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Combination circuit of multilevel inverter, matrix converter, and H-bridge

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ABSTRACT

In this study, a new integrated circuit design called H-bridge multilevel inverter matrix converter (HMIMC), which combines a multilevel inverter (MI), a matrix converter (MC), and an H-bridge circuit, is developed. It aims to generate a high number of output voltage levels that reduce the component count (CC). The MI step is used to control the positive voltage source, where the output of MI is connected to the input of MC. The MC is used to share the positive input voltage due to output phases, depending on the requirements. Afterward, the H-bridge circuit is used in each phase to select the positive or negative output voltage. The main contribution of this design is that the MI does not need to be repeated thrice to produce a three-phase output voltage. A seven-level (7L) and thirteen-level (13L) of proposed circuit is presented, followed by a new algorithm operation that is used for suitable switching control. Afterward, MATLAB simulation is used to check the operation process, output signals of voltage and current, and total harmonic distortion (THD) results. Then hardware circuit of the proposed system is implemented to verify the design. Lastly, a brief comparison in terms of CC is conducted.

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1. INTRODUCTION

In the first generation of multilevel inverters (MIs), the main challenges include how to connect power electronics with high-power applications and how to decrease total harmonic distortion (THD). At that time, four traditional MIs were designed: diode clamped MI [1], flying capacitor MI [2], cascaded MI [3], and generalized MI [4]. At the same time, four common switching algorithms were found: space vector control [5], selective harmonics elimination [6], [7] as low switching frequency. Space vector pulse width modulation (PWM) [8], [9], and sinusoidal PWM as high frequency control [10].

Afterward, many optimized design systems have been developed to decrease component count (CC), switching frequency, and power losses. While others are focused on increasing the number of output voltage levels, several MI designs that decrease CC without using an H-bridge circuit (e.g., T-type inverters (TTIs) [11]-[13], cascaded bipolar switched cells (CBSCs) [14], and packed-U cell topology [15]-[19] have been studied. In addition, several designs with an H-bridge circuit (e.g., cascaded half bridge-based multilevel DC-link inverter (MLDCL) [20], switched series/parallel sources (SSPS) MI [21], series-connected switched sources (SCSS) MI [22], [23], multilevel module (MLM) [24], reversing voltage (RV) MI [25] and two switches enabled level generation (2SELG) MI [26] have been studied to reduce the CC [26]. MI operation has several methods, and some of them use low switching frequency operations (e.g., equal phase (EP), half EP,

half height, feedforward, nearest level control (NLC), and nearest vector control (NVC) methods) [27], [28]. Others use high switching frequency (e.g., space vector modulation (SVM) and PWM).

Matrix converters (MCs) are widely used in industrial applications as an AC-AC converter. MCs have two types: direct and indirect. Indirect MCs use dual converters; the first is an AC-to-DC converter, and the second is a DC-to-AC converter. Thus, a DC link is required. Direct MCs are traditional MCs that contains three-by-three switches. Overall, nine bidirectional switches are used, and the main application of this type of MC is to drive the electrical motors. The traditional algorithm operation of MCs (e.g., SVM and Venturin modulation [29]) have been studied. Then, recent MC algorithms, such as hysteresis band, direct torque control, model predictive control, and sliding mode control have been studied [30].

However, many converters use multilevel and matrix design and structures as a features to support the conversion operation, previous studies have supported MCs with multilevel features inside their designs, such as stacked MC [31], sparse MC [32], hexagonal MC (hexverter) [33], and matrix interleaved converter [34]. The hybrid design of multilevel and matrix structure designs, such as multimodular [35]-[37], cascaded [38], and flying capacitor MIs [39], have been presented. In terms of indirect MCs, several studies have used MIs on DC-to-AC side (e.g., neutral point clamped MI [40], and T-type MI [41]). By contrast, inside direct MCs are MI connection (e.g., multilevel MC [42] and a new design of MC to generate a five-level (multilevel) output voltage [43].

In this study, a new connection between MI, direct MC and H-bridge circuit (HMIMC) is linked in series, as shown in Figure 1. The proposed system is designed to reduce the CC. The proposed HMIMC uses a novel algorithm operation called voltage selection algorithm (VSA) to provide a simple and suitable operation. MATLAB simulation is used to check the appropriateness of the circuit and its operation. lastly, a new CC equation of the proposed circuit is found and compared with top recent MIs that focus on reducing the CC switches.

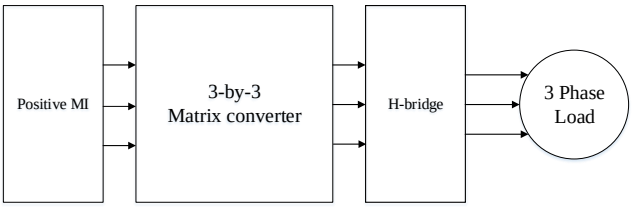

Figure 1. Schematic of the proposed circuit

2. OVERVIEW OF HMIMC

The proposed circuit HMIMC has three main steps; positive MI step, MC step, and H-bridge step. A seven-level (7L) HMIMC example is shown in Figure 2. The MI has three different voltage supplies, and each one has 100 V connected in series. Moreover, six isolated gate bipolar transistor (IGBT) switches are needed in this example, and two switches are needed for each voltage supply. Three different output voltages of MI are connected to the input of the MC. The traditional three-by-three MC is used; in MCs, three input voltages are received, and three output voltages are produced. The MC has nine switches; the operation of the MC switches is presented in the next section. Afterward, the output of the MC is connected to the H-bridge circuit to keep the output voltage positive or negative based on the requirement. Each phase needs four IGBT switches for the H-bridge circuit, that is, a total of twelve IGBT switches are required.

3. THE PRINCIPAL OPERATION OF HMIMC

The operation of HMIMC starts by generating all the voltages in MI from 0 V to 300 V within a 100 V level shift. If the HMIMC in Figure 2 is used, then 300 V is produced from the MI when S5 is 0 and S6 is1; at 200 V, S5 is 1 and S6 is 0. To generate 200 V and 100 V in the second leg of MC, S4 is 1 and S3 is 0, and for 100 V S4 is 0 and S3 is 1. To generate 100 V in the third leg of MC, switches S1 and S2 are (0,1) respectively, as shown in Table 1.

Afterward, the MC step is performed, the MC has three-by-three switches, and is operated and controlled using a three-by-three mathematical matrix. The nine switches of the MC are S11, S12, and S13 for the first column; S21, S22, and S23 for the second column; S31, S32, and S33 for the third column, in (1).

$$MC = \begin{bmatrix} S11 & S12 & S13 \\ S21 & S22 & S23 \\ S31 & S32 & S33 \end{bmatrix} \quad (1)$$

Lastly, the H-bridge step is used to set the negative and positive voltages of each phase, where the negative voltage uses the opposite operation of the positive trigger. When the positive voltage is needed, S1 and S4 are turned on at H-bridge circuit, and S2 and S3 are turned off. The operation of the H-bridge can be used in phases A, B, and C.

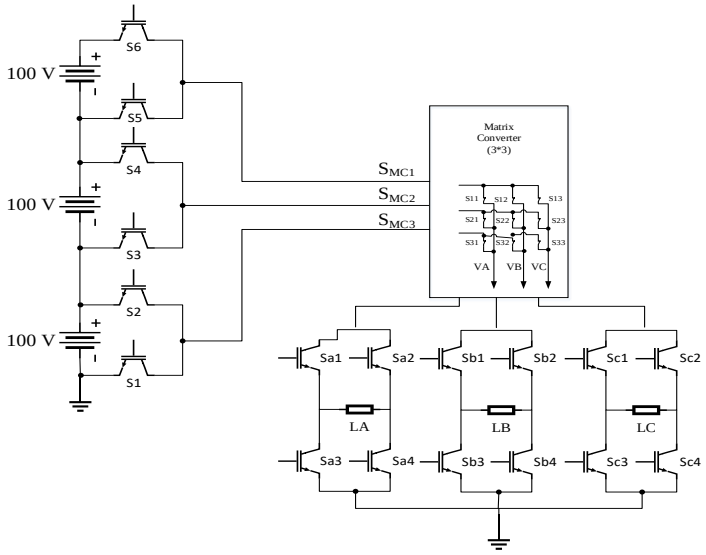

Figure 2. 7L HMIMC circuit

Table 1. Valid switching states of 7L HMIMC

#	V	MI						H-bridge (phase A)				H-bridge (phase B)				H-bridge (phase C)			
		S1	S2	S3	S4	S5	S6	Sa1	Sa2	Sa3	Sa4	Sb1	Sb2	Sb3	Sb4	Sc1	Sc2	Sc3	Sc4
1	300	X	X	X	X	0	1	1	0	0	1	1	0	0	1	1	0	0	1
2	200	X	X	0	1	1	0	1	0	0	1	1	0	0	1	1	0	0	1
3	100	0	1	1	0	X	X	1	0	0	1	1	0	0	1	1	0	0	1
4	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
5	-100	0	1	1	0	X	X	0	1	1	0	0	1	1	0	0	1	1	0
6	-200	X	X	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
7	-300	X	X	X	X	0	1	0	1	1	0	0	1	1	0	0	1	1	0

4. VOLTAGE SELECTION ALGORITHM

After the operation of the proposed circuit using MI, MC, and H-bridge circuits are presented. A new topology called VSA is found to simplify the overall operation. In this algorithm, the voltage is classified into groups with three different voltages. In our example of 7L HMIMC, three different VS groups (VS1, VS2, and VS3) are needed, as shown in Table 2. Each group has three different voltages. VS1 has 300, -100, and -100 V; VS2 has 200, -200, and 0 V; and VS3 has 100, -300, and 100 V. SMC1 is the first input of the MC and received voltages from MI either 200 or 300 in positive and either -200 V or -300 V in negative after included the H-bridge affections. Similarly, SMC2 received voltages of ±100 V or ±200 V, and SMC3 either 0 V or ±100 V.

For example, if a half period sequence of phase A is needed to generate from 300 V to -300 V, then the 300 V and 200 V are selected from VS1 and VS2, respectively, by connecting SMC1 and SMC2 to phase A respectively. Then, SMC3 is connected to phase A, and the following voltages are generated; 100, 0 and -100 V from VS3, VS2, and VS1. Lastly, -200 V and -300 V are generated when phase A is connected to SMC2 and SMC1 respectively, as shown in Figure 3.

Table 2. Voltage selection algorithm groups

VS groups	Voltage values (V)		
	S_{MC1}	S_{MC2}	S_{MC3}
VS1	±300	±100	±100
VS2	±200	±200	0
VS3	±200	±300	±100

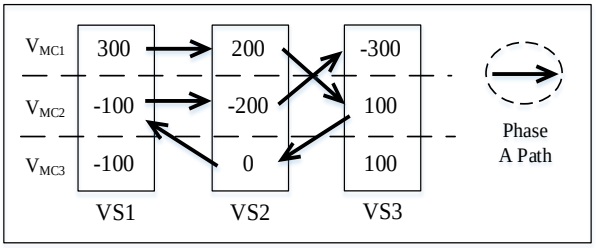

Figure 3. Operation path of the half cycle

When VS1 is used to generate 300 V to phase A, phase B and phase C have -100 V generated from the same VS group. In addition, when phase A uses 200 V, phase B has -200 V, and phase C has 0 V. Consequently, the operation of the VS is either forward (VSf) from VS1 to VS3 or backward (VSb) from VS3 to VS1. The (2) and (3) presents the above process.

$$VS_f = \begin{bmatrix} \text{VS1} \\ \text{VS2} \\ VS3 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \quad (2)$$

$$VS_b = \begin{bmatrix} \text{VS1} \\ \text{VS2} \\ \text{VS3} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 \\ 0 & 1 & 0 \\ 1 & 0 & 0 \end{bmatrix} \quad (3)$$

The operation of VS groups should be synchronized with the MC operation. The MC has six different state-matrix moods (M) known as M1, M2, M3, M4, M5, and M6 as shown in (4)-(9).

$$M1 = \begin{bmatrix} 0 & 0 & 1 \\ 0 & 1 & 0 \\ 1 & 0 & 0 \end{bmatrix} \quad (4)$$

$$M2 = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \quad (5)$$

$$M3 = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & 1 \\ 0 & 1 & 0 \end{bmatrix} \quad (6)$$

$$M4 = \begin{bmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \quad (7)$$

$$M5 = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix} \quad (8)$$

$$M6 = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 0 & 0 \end{bmatrix} \quad (9)$$

Where 1 means the switch is turned on and 0 is turned off.

To summarize the operation of HMIMC, Figure 4. Shows the overall operation of the HMIMC flow process. The input voltages of MC (SMC1, SMC2, SMC3) are changed by each step. At each step one VS groups is selected (VS1, VS2, VS3). The MC has six different state-matrix moods (M1, M2, M3, M4, M5, M6) synchronized with the voltage selection groups to generate the three phase output voltages.

The main advantage of using the VS algorithm is it can make the operation of the MI, MC, and H-bridge steps uniform. The VS algorithm can be optimized by using another common pervious operation technique, which is presented before.

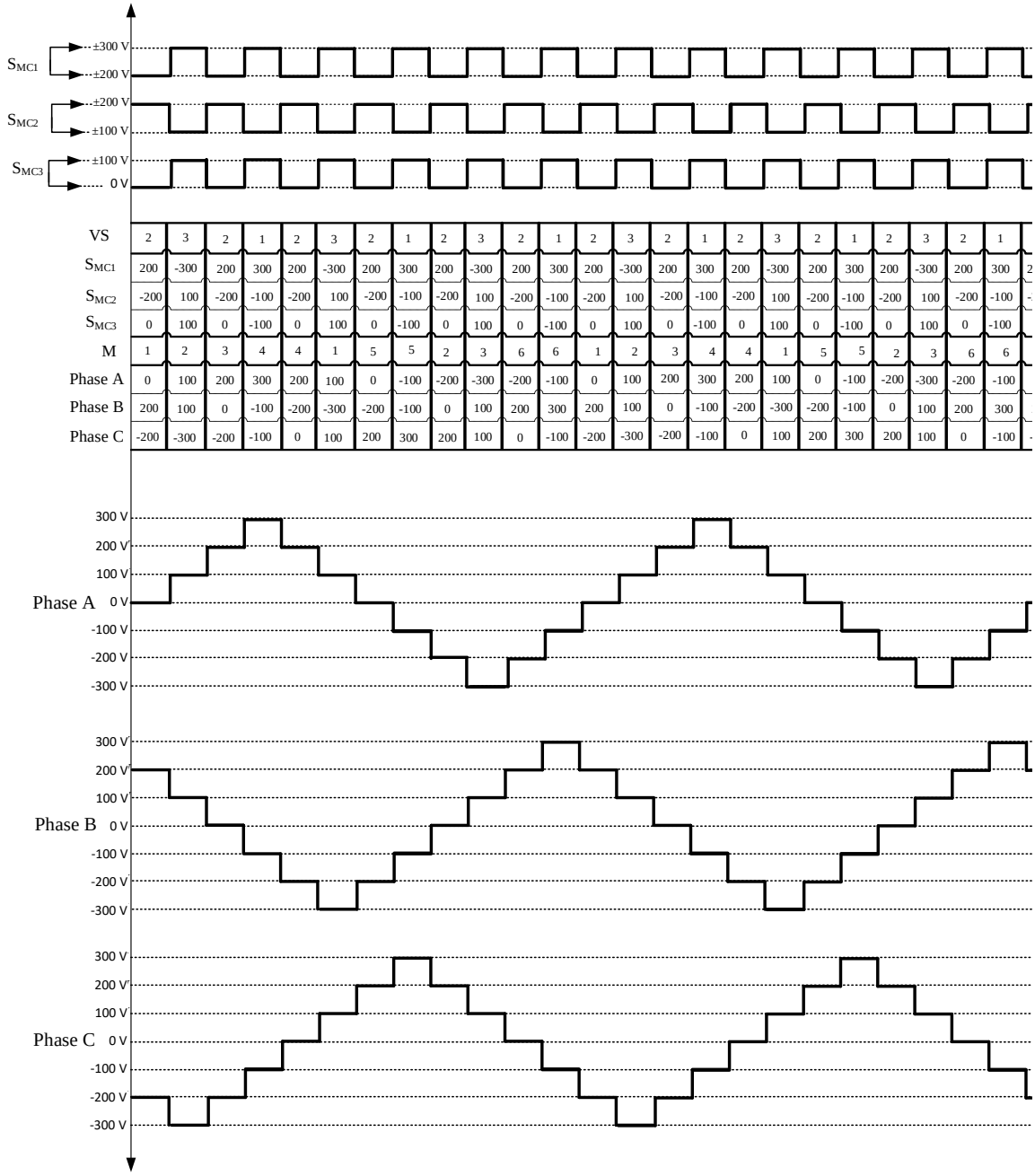

Figure 4. Overall operation of HMIMC

5. GENERAL FORM OF HMIMC

The general form of HMIMC to generate higher number of voltage level is presented in this section. As previously illustrated, HMIMC has three main steps; MI, MC, and H-bridge circuit. In the general form of HMIMC, the number of switches of the MC and H-bridge circuit is not increased; MC uses nine switches, and the H-bridge circuit uses twelve switches. The MI step varies when the number of HMIMC level varies; the relation of the number of levels of HMIMC and the number switches of MI steps is shown in Table 3.

The MI, MC, and H-bridge circuits use the common IGBT switch. The IGBT switch can be classified into unidirectional (UDS) and bidirectional (BDS) switch. UDSs use a single switch, whereas BDSs use two connected UDSs, as shown in Figure 5. A common-emitter BDS is shown in Figure 5(a), a common-collector BDS is shown in Figure 5(b), and a reverse UDS is shown in Figure 5(c) used two UDS. If the diode bridge BDS is used, only a single UDS is used, as shown in Figure 5(d).

Table 3. Equation of the HMIMC component count

HMIMC	No. of switches	Switch type
MI	$3(\left(\frac{n_{levels}-1}{6}\right)+1)$	# Unidirectional switch
MC	9	# Unidirectional switch
H-bridge	12	# Unidirectional switch

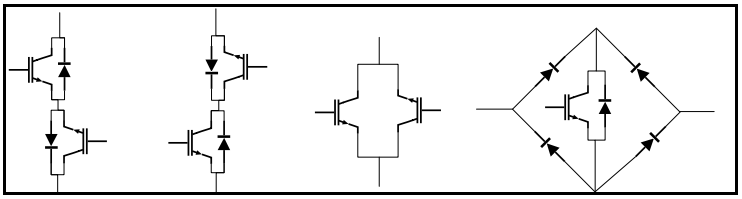

Figure 5. Types of bidirectional switch using IGBT [40]: (a) common-emitter BDS, (b) common-collector BDS, (c) reverse UDS, and (d) diode bridge BDS

6. RESULTS

MATLAB Simulink is used to validate the proposed HMIMC circuit design operated by the VSA operation. In the Simscape/power systems toolbox library, the IGBT with freewheeling diode, voltage power supply, and load is selected. The IGBT switch has two operation mode: turned on when the gate has a value of 1 and turned off when its value is 0.

However, a simple hardware design of the proposed circuit is implemented. The IGBT (IRG4BC30PF) is used and controlled by an Arduino Mega Microcontroller. The IGBT uses a TLP250 gate driver, and the Arduino Mega uses a BC337 transistor to switch the gate driver and decrease the current absorbed by the microcontroller, as shown in Figures 6 and 7.

The proposed VSA operation is used by simulation and practice. MI operations have different types, as previously mentioned. The VSA is used to simplify the previous type of operation when acting in the HMIMC design. In this study, the VSA involved by the EP operation is presented. Afterward, the VSA involved by NLC is presented in the subsequent section.

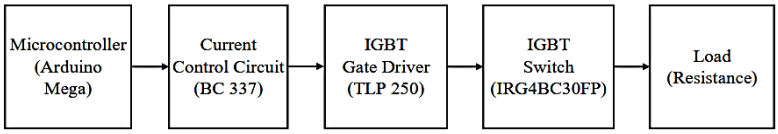

Figure 6. Schematic of the IGBT controlled by Arduino Mega

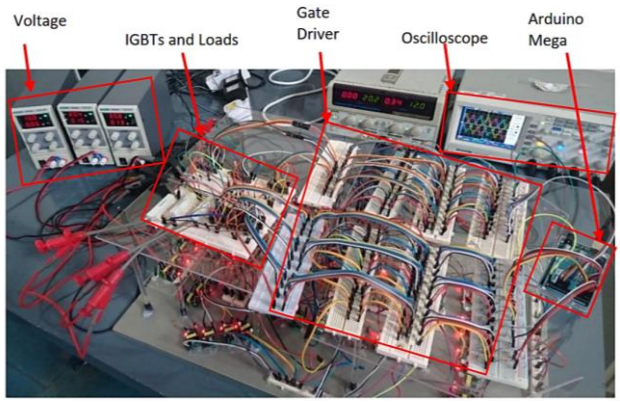

Figure 7. Practical implementation of 7L HMIMC

6.1. Equal phase with voltage selection algorithm

In the EP method, the single period is divided equally into the available number of levels, and then it generates a triangular output voltage signal, as shown in Figure 8. Three voltage sources are used; each one

has 100 V, and then a 300 V in positive and 300 V in negative can be generated. Overall, a 600 V peak-to-peak output voltage can be produced.

Three-phase of 100 ohms load is connected to 7L HMIMC. The current generated by the circuit is presented in Figure 9. The generated signal of current is same of voltage divided by resistive load, and the system operated at 50 Hz. Afterward, the switching frequency operation increased seven times to use nearest level control (NLC). Further details about the operation HMIMC using VSA and NLC are presented in the following section.

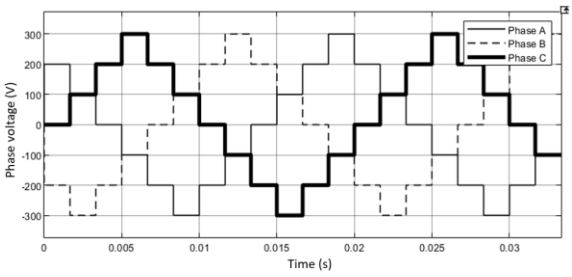

Figure 8. Voltage output signal of 7L HMIMC

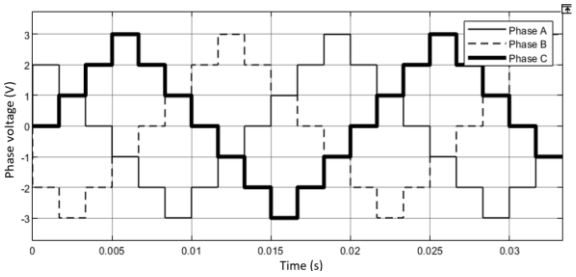

Figure 9. Current output signal of 7L HMIMC

6.2. Nearest level control with voltage selection algorithm

In the NLC the switching frequency should be increased; in this study, the switching frequency is increased seven times, that is, from 50 Hz to 350 Hz, which is still classified as low switching frequency. In the NLC, the output voltage be more sinusoidal will that could be reduce the THD. That purify on the output signal comes when the error of pure sine wave voltage is compared with proposed output voltage signal. However, as known the slope of pure sinusoidal at zero is higher than the slope at peak voltage. Increase the slope value, caused to decrease the time delay depends on the number of levels and levels value.

At 350 Hz, the same voltage level (7L) and same voltage value of 50 Hz are used, the sample time (ST) varies depending on the voltage value. The sample time and voltage value are found using MATLAB Simulink, as shown in Figure 10. The ST of 300 V is 15 ST; at 200 V, it is 7 ST; at 100 V it is 4 ST; and at 0 V it is 5 ST. The ST of 0 V is higher than 10V because the 0V ST is used in positive and negative time. In one period, only two STs of 0 V are used, totally 10 ST is used. On the other hand, the ST of 10 V is used four time: two in positive and two in negative. Overall, 16 ST is used for 10 V, which is higher than 0 V. On this basis, the number of STs at one period is 84 ST.

The 300 V ST is used two times in one period, once in positive another in negative. The three-phase operation of 7L HMIMC using NLC and VSA is shown in Table 4, where each phase is shifted by 28 ST. The state matrix of VSA using NLC is different from VSA using EP; here in some steps, two output phases are powered by a single voltage source. This case is accepted where no short circuit has happened, the new six state-matrix are used as (10)-(15).

$$M7 = \begin{bmatrix} 1 & 1 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix} \quad (10)$$

$$M8 = \begin{bmatrix} 1 & 0 & 1 \\ 0 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \quad (11)$$

$$M9 = \begin{bmatrix} 0 & 1 & 1 \\ 0 & 0 & 0 \\ 1 & 0 & 0 \end{bmatrix} \quad (12)$$

$$M10 = \begin{bmatrix} 0 & 0 & 1 \\ 1 & 1 & 0 \\ 0 & 0 & 0 \end{bmatrix} \quad (13)$$

$$M11 = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 1 \\ 0 & 0 & 0 \end{bmatrix} \quad (14)$$

$$M12 = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 1 \\ 0 & 0 & 0 \end{bmatrix} \quad (15)$$

The 84 ST of VSA using NLC is shown in Table 4, and each step the number of step and the value of the output voltage of three-phase is presented. The state-matrix (M) is also included. The same color of operation in Figure 9 is used in Table 4. The output voltage of VSA using NLC is presented in Figure 11. An output voltage that is more sinusoidal will that decrease the THD. The output current of 7L HMIMC using VSA and NLC is presented in Figure 12, where the load is R equal to 100 ohms.

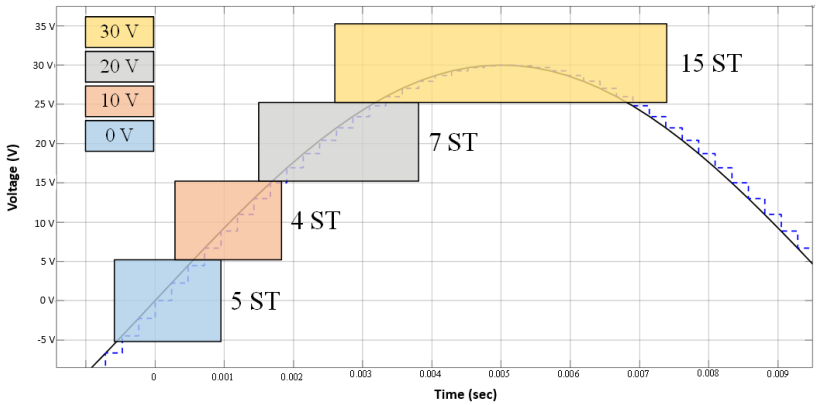

Figure 10. Sample time of 7L HMIMC using the VSA and NLC

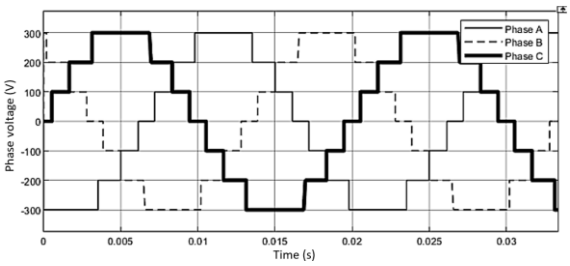

Figure 11. Output voltage of 7L HMIMC NLC

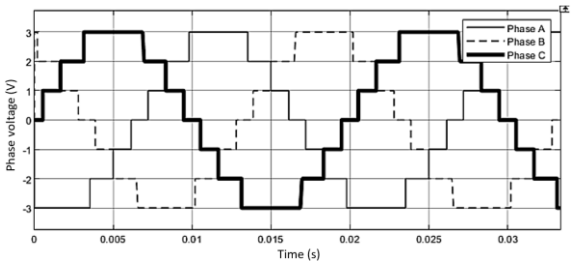

Figure 12. Output current of 7L HMIMC using NLC

Table 4. Generating the values of NLC and VSA of one period

Step	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
Phase A	0	0	0	0	0	100	100	100	100	200	200	200	200	200	200	200	300	300	300	300	300
Phase B	-200	-200	-300	-300	-300	-300	-300	-300	-300	-300	-300	-300	-300	-300	-300	-300	-300	-200	-200	-200	-200
Phase C	300	300	300	200	200	200	200	200	200	200	100	100	100	100	0	0	0	0	0	-100	-100
M	5	5	9	6	6	6	6	6	6	11	1	1	1	1	1	1	7	2	2	2	2

Step	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42
Phase A	300	300	300	300	300	300	300	300	300	300	200	200	200	200	200	200	200	100	100	100	100
Phase B	-200	-200	-200	-100	-100	-100	-100	0	0	0	0	0	100	100	100	100	200	200	200	200	200
Phase C	-100	-100	-200	-200	-200	-200	-200	-200	-200	-300	-300	-300	-300	-300	-300	-300	-300	-300	-300	-300	-300
M	2	2	12	3	3	3	3	3	3	8	4	4	4	4	4	4	10	5	5	5	5

Step	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
Phase A	0	0	0	0	0	-100	-100	-100	-100	-200	-200	-200	-200	-200	-200	-200	-300	-300	-300	-300	-300
Phase B	200	200	300	300	300	300	300	300	300	300	300	300	300	300	300	300	300	200	200	200	200
Phase C	-300	-300	-300	-200	-200	-200	-200	-200	-200	-200	-100	-100	-100	-100	0	0	0	0	0	100	100
M	5	5	9	6	6	6	6	6	6	11	1	1	1	1	1	1	7	2	2	2	2

Step	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84
Phase A	-300	-300	-300	-300	-300	-300	-300	-300	-300	-300	-200	-200	-200	-200	-200	-200	-200	-100	-100	-100	-100
Phase B	200	200	200	100	100	100	100	0	0	0	0	0	-100	-100	-100	-100	-200	-200	-200	-200	-200
Phase C	100	100	200	200	200	200	200	200	200	300	300	300	300	300	300	300	300	300	300	300	300
M	2	2	12	3	3	3	3	3	3	8	4	4	4	4	4	4	10	5	5	5	5

7. CASE STUDY

Further study is conducted on the proposed circuit HMIMC. This paper introduces three additional experiments; upgrade the HMIMC to thirteen-levels (13L) levels, use VSA, and NLC on 13L HMIMC, changing load parameter, and THD results.

7.1. Upgrade the number of levels

As other multilevel inverter topology, the proposed HMIMC levels can be increased. A 13L HMIMC is prepared where only the positive MI should be increased. In positive MI seven IGBT switches were used, switch 1 (S1) is for grounding the loads as shown in Figure 13. All the positive MI signals are grouped and linked to MC then to H-bridge circuit. The output voltage signal of 13L HMIMC is presented on Figure 14, and the output current signal of 13L HMIMC at R load of 100 ohm is presented on Figure 15. The symmetrical between the voltage and current signal is demonstrated with different value of signal depending on the resistive values.

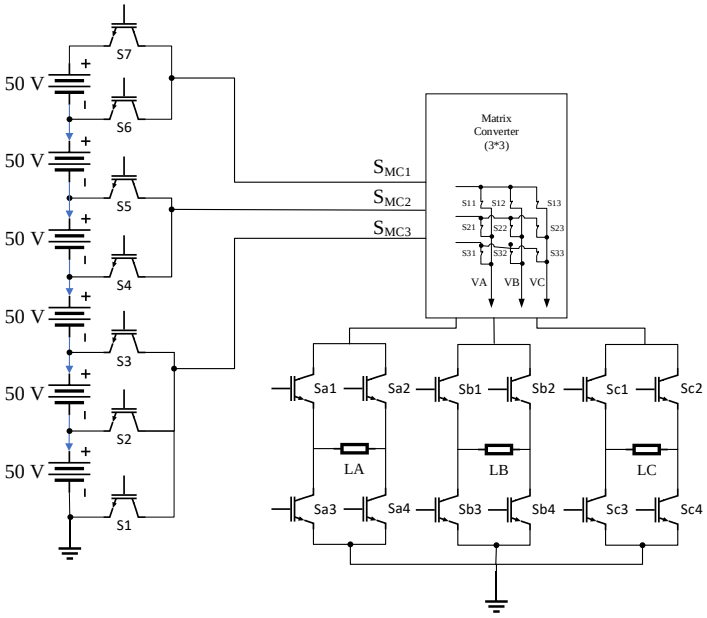

Figure 13. Proposed circuit of 13L HMIMC

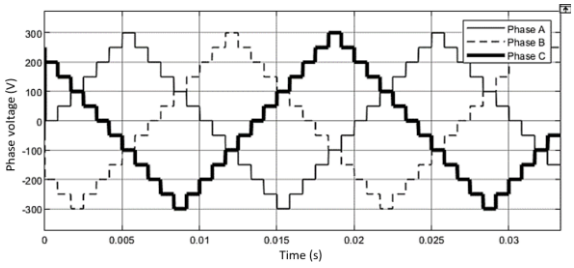

Figure 14. Output voltage of 13L HMIMC VSA

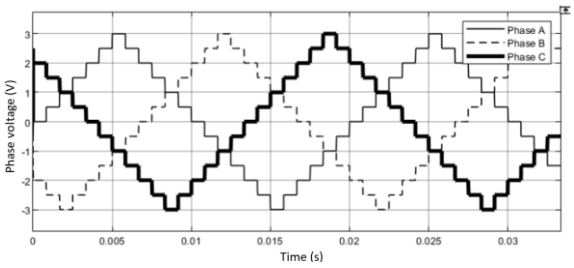

Figure 15. Output current of 13L HMIMC VSA

7.2. Use VSA and NLC on 13L HMIMC case study

In this section, the results of operation the 13L HMIMC using VSA and NLC are presented. The output signal of voltage and current is presented in Figures 16 and 17 respectively. The sequences of one period of 13L HMIMC using NLC and VSA are presented in Table 5. The sample time and voltage value are found. The ST of 300 V is 21 ST; at 250 V, it is 9 ST; at 200 V, it is 6 ST; at 150 V, it is 5 ST; at 100 V, it is 5 ST; at 50 V it is 4 ST; and at 0 V it is 5 ST. Still the 0V has the lowest number of sample time, where the 5 ST of 0 V is used in positive and negative side as presented before.

As illustrated in Table 5, the three phases: phase A, phase B, and phase C are presented. After one period of phase A, starting from 0V to 300, then from 300 to -300 V, finishing from -300 to 0 V. Phases B and C are synchronized with phase A and shifted by 56 ST. It is noteworthy that the 150 V ST of any two phases

are situated within the same ST region and are positioned midway of ±300 V ST region. In one period, two of 5 STs of 0 V and 21 STs of 300 V are used, totally 52 ST are used in 0V and 300 V. On the other hand, the ST of 50 V, 100 V, 150 V, 200 V, and 250 V are used four times: two in positive and two in negative. Based to each ST as mentioned before, the number of STs at one period is 168 ST.

Table 5. The values of NLC and the VSA of one period at 13L HMIMC

Step	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
Phase A	0	0	0	0	0	50	50	50	50	100	100	100	100	100	150	150	150	150	150	200	200
Phase B	-250	-250	-250	-250	-250	-250	-300	-300	-300	-300	-300	-300	-300	-300	-300	-300	-300	-300	-300	-300	-300
Phase C	250	250	250	250	250	250	250	250	200	200	200	200	200	200	150	150	150	150	150	100	100

Step	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42
Phase A	200	200	200	200	250	250	250	250	250	250	250	250	250	300	300	300	300	300	300	300	300
Phase B	-300	-300	-300	-300	-300	-300	-250	-250	-250	-250	-250	-250	-250	-250	-250	-200	-200	-200	-200	-200	-200
Phase C	100	100	100	50	50	50	50	0	0	0	0	0	-50	-50	-50	-50	-100	-100	-100	-100	-100

Step	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
Phase A	300	300	300	300	300	300	300	300	300	300	300	300	300	250	250	250	250	250	250	250	250
Phase B	-150	-150	-150	-150	-150	-100	-100	-100	-100	-100	-50	-50	-50	-50	0	0	0	0	0	50	50
Phase C	-150	-150	-150	-150	-150	-200	-200	-200	-200	-200	-200	-250	-250	-250	-250	-250	-250	-250	-250	-250	-300

Step	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84
Phase A	250	200	200	200	200	200	200	150	150	150	150	150	100	100	100	100	100	50	50	50	50
Phase B	50	50	100	100	100	100	100	150	150	150	150	150	200	200	200	200	200	200	250	250	250
Phase C	-300	-300	-300	-300	-300	-300	-300	-300	-300	-300	-300	-300	-300	-300	-300	-300	-300	-300	-300	-300	-250

Step	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105
Phase A	0	0	0	0	0	-50	-50	-50	-50	-100	-100	-100	-100	-100	-150	-150	-150	-150	-150	-200	-200
Phase B	250	250	250	250	250	250	300	300	300	300	300	300	300	300	300	300	300	300	300	300	300
Phase C	-250	-250	-250	-250	-250	-250	-250	-250	-200	-200	-200	-200	-200	-200	-150	-150	-150	-150	-150	-100	-100

Step	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126
Phase A	-200	-200	-200	-200	-250	-250	-250	-250	-250	-250	-250	-250	-250	-300	-300	-300	-300	-300	-300	-300	-300
Phase B	300	300	300	300	300	300	250	250	250	250	250	250	250	250	250	200	200	200	200	200	200
Phase C	-100	-100	-100	-50	-50	-50	-50	0	0	0	0	0	50	50	50	50	100	100	100	100	100

Step	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147
Phase A	-300	-300	-300	-300	-300	-300	-300	-300	-300	-300	-300	-300	-300	-250	-250	-250	-250	-250	-250	-250	-250
Phase B	150	150	150	150	150	100	100	100	100	100	50	50	50	50	0	0	0	0	0	-50	-50
Phase C	150	150	150	150	150	200	200	200	200	200	200	250	250	250	250	250	250	250	250	250	300

Step	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168
Phase A	-250	-200	-200	-200	-200	-200	-200	-150	-150	-150	-150	-150	-100	-100	-100	-100	-100	-50	-50	-50	-50
Phase B	-50	-50	-100	-100	-100	-100	-100	-150	-150	-150	-150	-150	-200	-200	-200	-200	-200	-200	-250	-250	-250
Phase C	300	300	300	300	300	300	300	300	300	300	300	300	300	300	300	300	300	300	300	300	250

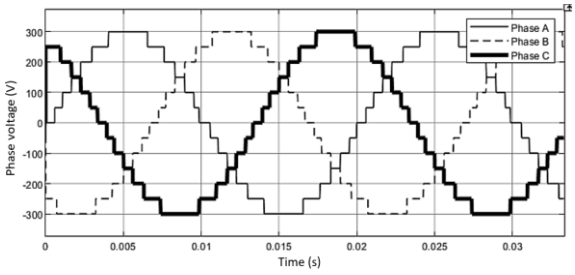

Figure 16. Output voltage of R load 13L HMIMC

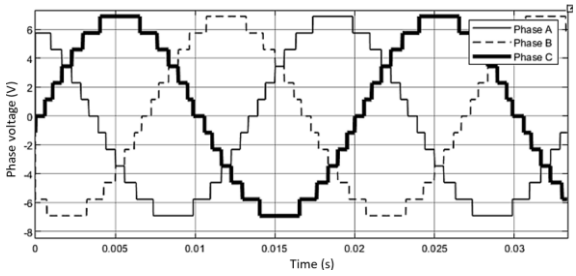

Figure 17. Output current of R load 13L HMIMC

7.3. Changing load

In this section, the load of 13L HMIMC is changed from resistive load (R) to resistive and capacitive load (RC). At RC case study the values of loads R= 100 ohm and C = 1000 uF. The current and the voltage results of RC load are presented in Figures 18 and 19.

The current and voltage signal of 13L HMIMC using VSA and NLC after load changed to RC are shown in Figures 20 and 21 respectively. In addition, the results RC load after the resistive value is changed to half is presented in Figures 22 and 23. The voltage is not affected by changing the resistive load, while the current is doubled. The maximum current at 100 ohms is 3 A, where at 50 ohms is 6 A for each phase of three phases.

7.4. THD results

In this section, the results of THD of the proposed circuit HMIMC is presented. The THD of 7L and 13L HMIMC using VSA are presented in Table 6 by 21.77% and 15.25%. The NLC operation decrease the THD in 7L to reach 12.23% and in 13L to 6.5%. The harmonics of 13L HMIMC are presented in Figure 24, the magnitude of fifth and seventh harmonic order are 0.53% and 0.51% of fundamental value respectively.

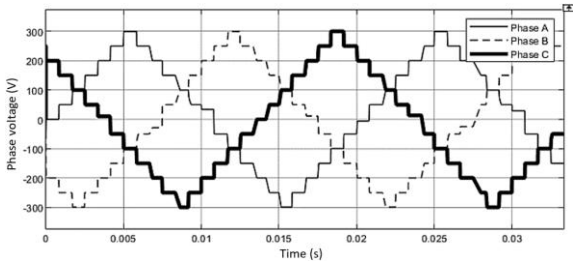

Figure 18. Output voltage of RC load 13L HMIMC

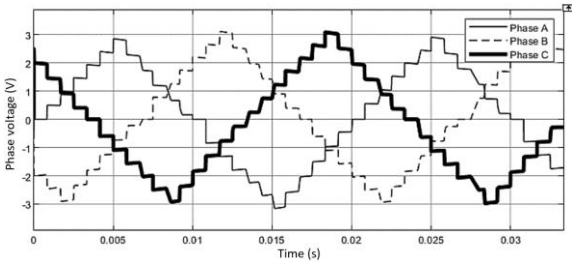

Figure 19. Output current of RC load 13L HMIMC

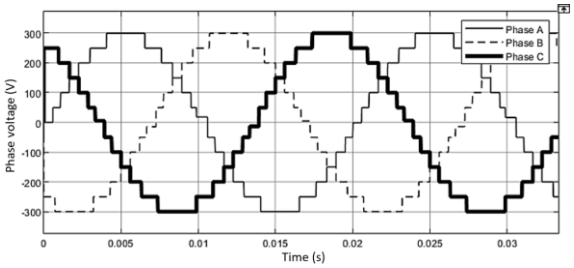

Figure 20. Output voltage of RC 13L HMIMC NLC

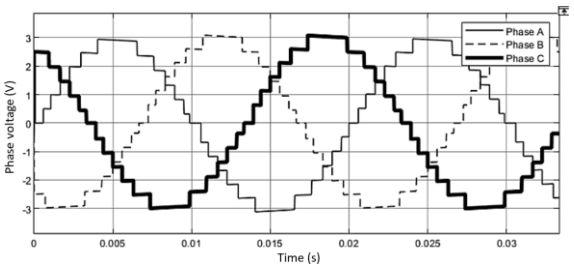

Figure 21. Output current of RC 13L HMIMC NLC

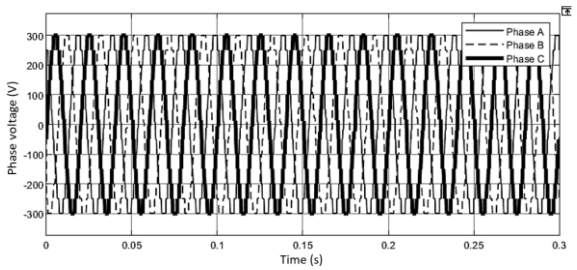

Figure 22. Output voltage of varies R load 13L

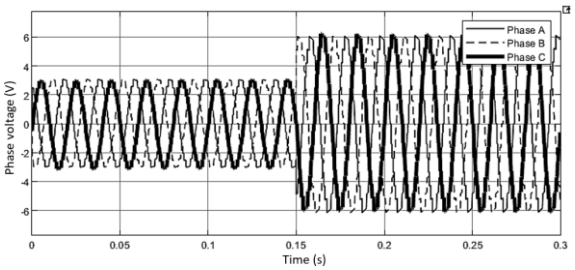

Figure 23. Output current of varies R load 13L HMIMC

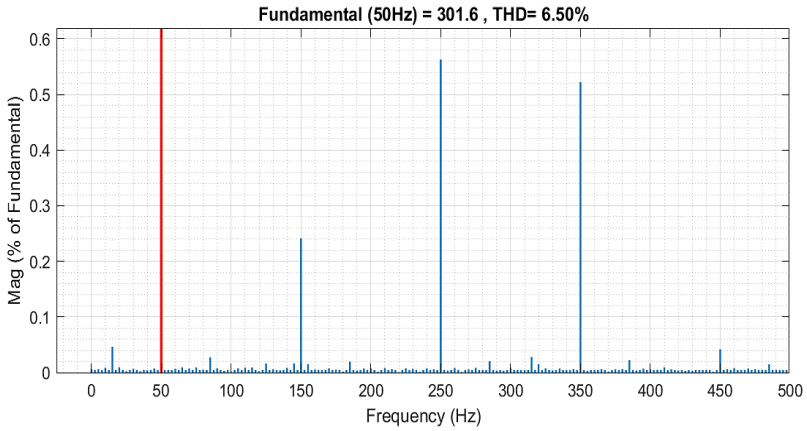

Figure 24. THD of the 13L HMIMC using VSA and NLC

Table 6. THD of the HMIMC

Circuit	Level	Operation	Frequency	THD
HMIMC	7L	VSA	Low	21.77%
HMIMC	7L	VSA and NLC	Low	12.23%
HMIMC	13L	VSA	Low	15.25%
HMIMC	13L	VSA and NLC	Low	6.5%

8. DISCUSSION AND COMPARISON

The relation between the number of CC with respect to the number of levels can be presented by the equation shown in Table 7. The traditional MIs such as DCMI, FCMI, and CMI have the same CC equations; 6(n_levels-1), and only use UDS. The number of switches of UDS and BDS can be equal if diode bridge BDS is used. Otherwise, each BDS equal two UDS. In this study, the comparison has two scenarios: i) when the UDS equals one BDS and ii) when the UDS equals two BDS. The equations of recent designs that reduce MI CC (e.g., TTI, CBSC, MLDCL, SSPS, SCSS, MLM, RV, and 2SELG) are also given in Table 7.

8.1. When BDS equal one UDS

A brief comparison between the proposed circuit HMIMC and a previous study of MI is presented in Table 8. The number of levels selected is 7, 13, 19, and 25. The traditional MI (TrMI) has the maximum number of CC in all levels. CBSC, MLM and 2SELG have the lowest CC at 7L by 24 switches, where the proposed circuit has only 21 switches. At thirteen levels (13L), the proposed HMIMC has the lowest MI CC with 30 switches, whereas the MLM and 2SELG have three more switches, that is, 33.

The repetition of single-phase three times increases the CC, especially if a high number of levels is generated. Solving the three-time-repetition (TTR) could be the best method to reduce the CC. The percentage reduce of CC at 7L is 12.5%; at 13L, it is 9.1%; at 19L, it is 21.4%; and at 25L, it is 29.4%. The percentage of reduction in the proposed circuit increases when the number of voltage level is increased.

Table 7. Previous MI equation that counts the component [23]

No	Topology	Ref.	Unidirectional switch	Bidirectional switch
1	TrMI	[1]-[3]	$2 * 3(n_{levels} - 1)$	0
5	TTI	[11]-[13]	12	$3(n_{levels} - 1)$
6	CBSC	[14]	0	$3(n_{levels} + 1)$
7	MLDCL	[20], [21]	$3(n_{levels} + 3)$	0
8	SSPS	[22]	$(3(3n_{levels} - 1))/2$	0
9	SCSS	[23], [24]	$3(n_{levels} + 3)$	0
10	MLM	[25]	12	$(3(n_{levels} + 1))/2$
11	RV	[26]	$3(n_{levels} + 3)$	0
12	2SELG	[27]	24	$(3(n_{levels} - 7))/2$

8.1. When BDS equal two UDS

The HMIMC uses only a UDS, where the proposed circuit could increase the gap of the CC results. The results are presented in Table 9, where the percentage reduction at 7L is 12.5%; at 13L, it is 28.5%; at 19L, it is 45%; and at 25L, it is 53.8%. Moreover, at a high number of voltage levels, the reduction percentage increases. In this scenario, the traditional MI does not have the maximum number of CC compared with recent MI designs.

Table 8. Comparison results of CC when BDS equals one UDS

MI types No. levels	TrMI	TTI	CBSC	MLDCL, SCSS, RV	SSPS	MLM	2SELG	HMIMC	Reduce %
7	36	30	24	30	30	24	24	21	12.5%
13	72	48	42	48	57	33	33	30	9.1%
19	108	66	60	66	84	42	42	33	21.4%
25	144	84	78	84	111	51	51	36	29.4%

*Only at 7L the CC of HMIMC is calculated without using the equation, because the voltage source is linked directly to the MC step, where no need to count the MI step switches.

Table 9. Comparison results of CC when BDS equals two UDS

MI types No. levels	TrMI	TTI	CBSC	MLDCL, SCSS, RV	SSPS	MLM	2SELG	HMIMC	Reduce %
7	36	48	48	30	30	36	24	21	12.5%
13	72	84	84	48	57	54	42	30	28.5%
19	108	120	120	66	84	72	60	33	45%
25	144	156	156	84	111	90	78	36	53.8%

9. CONCLUSION

The proposed circuit HMIMC is designed and controlled to reduce the CC. The HMIMC needs three steps: MI, MC, and H-bridge. In HMIMC control, the operation of MI and H-bridge is performed by using the VSA to generate different groups that have a selected voltage. Then, the MC should synchronize its operation with the VS operation to operate the three-phase output voltage. 7L and 13L of HMIMC are used and operated by VSA and NLC. To simplify the operation and synchronize MI, MC, and H-bridge, the VSA is demonstrate.

Case study of 7L and 13L with changing load parameter and value is presented. THD of 7L and 13L using VSA and NLC is obtained, where the lowest value of THD at low frequency operation has 6.5%. Lastly, the proposed circuit is compared with traditional and recent MIs that focus on CC reduction. Excellent results are found at a high number of levels and satisfactory results is found at a low number of levels. Future studies on the proposed circuit should consider the reduction of THD to be less than 5%, whether by using high switching frequency or increasing the output voltage levels.

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AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

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C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

The authors confirm that the data supporting the findings of this study are available within the article.

REFERENCES

[1] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Transactions on Industry Applications*, vol. IA-17, no. 5, pp. 518–523, 1981, doi: 10.1109/TIA.1981.4503992.
[2] T. A. Meynard and H. Foch, "Multi-level conversion: High voltage choppers and voltage-source inverters," *PESC Record - IEEE Annual Power Electronics Specialists Conference*, pp. 397–403, 1992, doi: 10.1109/PESC.1992.254717.
[3] I. R. H. Baker and L. H. Bannister, "United States Patent (19)," 1975.
[4] F. Z. Peng, "A generalized multilevel inverter topology with self voltage balancing," *IEEE Transactions on Industry Applications*, vol. 37, no. 2, pp. 611–618, 2001, doi: 10.1109/28.913728.
[5] Q. Cheng, C. Wang, X. You, Z. Chen, and Z. Dong, "Voltage-balancing control in stacked multicell converter based on single space-vector modulation," *IEEE Transactions on Power Electronics*, vol. 37, no. 1, pp. 344–353, 2022, doi: 10.1109/TPEL.2021.3098843.
[6] C. Wang, Q. Zhang, W. Yu, and K. Yang, "A comprehensive review of solving selective harmonic elimination problem with algebraic algorithms," *IEEE Transactions on Power Electronics*, vol. 39, no. 1, pp. 850–868, 2024, doi: 10.1109/TPEL.2023.3327280.

[7] I. Ibanez-Hidalgo *et al.*, "Real time selective harmonic control—PWM based on artificial neural networks," *IEEE Transactions on Power Electronics*, vol. 39, no. 1, pp. 768–783, Jan. 2024, doi: 10.1109/TPEL.2023.3322500.

[8] S. Raju and N. Mohan, "Switching optimized modulation for direct three-level matrix converter," *IEEE Transactions on Power Electronics*, vol. 39, no. 3, pp. 3313–3328, 2024, doi: 10.1109/TPEL.2023.3339480.

[9] J. Yin *et al.*, "An improved indirect pulsewidth modulation technique for modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 39, no. 1, pp. 733–743, 2024, doi: 10.1109/TPEL.2023.3321759.

[10] R. José, L. Jih-Sheng, and P. Fangzheng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 2, pp. 724–738, 2002.

[11] G. M. Martins, J. A. Pomilio, S. Buso, and G. Spiazzi, "Three-phase low-frequency commutation inverter for renewable energy systems," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 5, pp. 1522–1528, 2006, doi: 10.1109/TIE.2006.882023.

[12] G. Ceglia, V. Guzmán, C. Sánchez, F. Ibáñez, J. Walter, and M. I. Giménez, "A new simplified multilevel inverter topology for DC-AC conversion," *IEEE Transactions on Power Electronics*, vol. 21, no. 5, pp. 1311–1319, 2006, doi: 10.1109/TPEL.2006.880303.

[13] N. A. Rahim, K. Chaniago, and J. Selvaraj, "Single-phase seven-level grid-connected inverter for photovoltaic system," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 6, pp. 2435–2443, 2011, doi: 10.1109/TIE.2010.2064278.

[14] E. Babaei, "A cascade multilevel converter topology with reduced number of switches," *IEEE Transactions on Power Electronics*, vol. 23, no. 6, pp. 2657–2664, 2008, doi: 10.1109/TPEL.2008.2005192.

[15] Y. Ounejjar, K. Al-Haddad, and L. A. Grégoire, "Packed U cells multilevel converter topology: Theoretical study and experimental validation," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 4, pp. 1294–1306, 2011, doi: 10.1109/TIE.2010.2050412.

[16] Y. Ounejjar and K. Al-Haddad, "A novel high energetic efficiency multilevel topology with reduced impact on supply network," *IECON Proceedings (Industrial Electronics Conference)*, pp. 489–494, 2008, doi: 10.1109/IECON.2008.4758002.

[17] Y. Ounejjar and K. Al-Haddad, "Multilevel hysteresis controller of the novel seven-level packed U cells converter," *SPEEDAM 2010 - International Symposium on Power Electronics, Electrical Drives, Automation and Motion*, pp. 186–191, 2010, doi: 10.1109/SPEEDAM.2010.5542178.

[18] Y. Ounejjar, K. Al-Haddad, and L. A. Grégoire, "Novel three phase seven level PWM converter," *2009 IEEE Electrical Power and Energy Conference, EPEC 2009*, 2009, doi: 10.1109/EPEC.2009.5420867.

[19] Y. Ounejjar and K. Al-Haddad, "A new high power efficiency cascaded U cells multilevel converter," *IEEE International Symposium on Industrial Electronics*, pp. 483–488, 2009, doi: 10.1109/ISIE.2009.5214290.

[20] G. J. Su, "Multilevel DC-link inverter," *IEEE Transactions on Industry Applications*, vol. 41, no. 3, pp. 848–854, 2005, doi: 10.1109/TIA.2005.847306.

[21] Y. Hinago and H. Koizumi, "A single-phase multilevel inverter using switched series/parallel DC voltage sources," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2643–2650, 2010, doi: 10.1109/TIE.2009.2030204.

[22] W. K. Choi and F. S. Kang, "H-bridge based multilevel inverter using PWM switching function," *INTELEC, International Telecommunications Energy Conference (Proceedings)*, 2009, doi: 10.1109/INTLEC.2009.5351886.

[23] S. H. Lee and F. S. Kang, "A new structure of H-bridge multilevel inverter," in *Proceedings KIPE Conference*, 2008, pp. 388–390,

[24] J. Ebrahimi, E. Babaei, and G. B. Gharehpetian, "A new multilevel converter topology with reduced number of power electronic components," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 2, pp. 655–667, 2012, doi: 10.1109/TIE.2011.2151813.

[25] H. Nademi, A. Das, R. Burgos, and L. E. Norum, "A new circuit performance of modular multilevel inverter suitable for photovoltaic conversion plants," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 2, pp. 393–404, 2016, doi: 10.1109/JESTPE.2015.2509599.

[26] M. F. Kangarlu and E. Babaei, "A generalized cascaded multilevel inverter using series connection of submultilevel inverters," *IEEE Transactions on Power Electronics*, vol. 28, no. 2, pp. 625–636, 2013, doi: 10.1109/TPEL.2012.2203339.

[27] K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu, and S. Jain, "Multilevel inverter topologies with reduced device count: A review," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 135–151, Jan. 2016, doi: 10.1109/TPEL.2015.2405012.

[28] N. Prabaharan and K. Palanisamy, "A comprehensive review on reduced switch multilevel inverter topologies, modulation techniques and applications," *Renewable and Sustainable Energy Reviews*, vol. 76, pp. 1248–1282, 2017, doi: 10.1016/j.rser.2017.03.121.

[29] A. M. Al-Mahrouk, N. F. Mailah, M. A. Mohd Radzi, and M. K. Hassan, "Systematic review of multilevel and matrix usage in power electronics: Circuit Types, System Taxonomy, Applications and Recommendations," *International Review of Electrical Engineering (IREE)*, vol. 15, no. 2, p. 108, Apr. 2020, doi: 10.15866/iree.v15i2.17479.

[30] P. W. Wheeler, J. Rodríguez, J. C. Clare, L. Empringham, and A. Weinstein, "Matrix converters: A technology review," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 2, pp. 276–288, 2002, doi: 10.1109/41.993260.

[31] J. Zhang, L. Li, and D. G. Dorrell, "Control and applications of direct matrix converters: A review," *Chinese Journal of Electrical Engineering*, vol. 4, no. 2, pp. 18–27, 2018, doi: 10.23919/CJEE.2018.8409346.

[32] S. M. Mousavi Sangdehi, S. Hamidifar, and N. C. Kar, "A novel bidirectional DC/AC stacked matrix converter design for electrified vehicle applications," *IEEE Transactions on Vehicular Technology*, vol. 63, no. 7, pp. 3038–3050, 2014, doi: 10.1109/TVT.2014.2325740.

[33] N. Taib, B. Metidji, and T. Rekioua, "Performance and efficiency control enhancement of wind power generation system based on DFIG using three-level sparse matrix converter," *International Journal of Electrical Power and Energy Systems*, vol. 53, no. 1, pp. 287–296, 2013, doi: 10.1016/j.ijepes.2013.05.019.

[34] L. Baruschka and A. Mertens, "A new three-phase AC/AC modular multilevel converter with six branches in hexagonal configuration," *IEEE Transactions on Industry Applications*, vol. 49, no. 3, pp. 1400–1410, 2013, doi: 10.1109/TIA.2013.2252593.

[35] Y. Hu, R. Zeng, W. Cao, J. Zhang, and S. J. Finney, "Design of a Modular, High Step-Up Ratio DC-DC Converter for HVDC Applications Integrating Offshore Wind Power," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 4, pp. 2190–2202, 2016, doi: 10.1109/TIE.2015.2510975.

[36] J. Wang, B. Wu, D. Xu, and N. R. Zargari, "Indirect space-vector-based modulation techniques for high-power multimodular matrix Converters," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 8, pp. 3060–3071, 2013, doi: 10.1109/TIE.2012.2200215.

[37] S. Liu, X. Wang, Y. Meng, P. Sun, H. Luo, and B. Wang, "A decoupled control strategy of modular multilevel matrix converter for fractional frequency transmission system," *IEEE Transactions on Power Delivery*, vol. 32, no. 4, pp. 2111–2121, 2017, doi: 10.1109/TPWRD.2016.2646384.

[38] J. Wang, B. Wu, D. Xu, and N. R. Zargari, "Phase-shifting-transformer-fed multimodular matrix converter operated by a new modulation strategy," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 10, pp. 4329–4338, 2013, doi: 10.1109/TIE.2012.2217714.

[39] S. Thamizharasan, J. Baskaran, and S. Ramkumar, "A new cascaded multilevel inverter topology with voltage sources arranged in matrix structure," *Journal of Electrical Engineering and Technology*, vol. 10, no. 4, pp. 1552–1557, 2015, doi: 10.5370/JEET.2015.10.4.1552.
[40] O. Bouhali, B. Francois, and N. Rizoug, "Equivalent matrix structure modelling and control of a three-phase flying capacitor multilevel inverter," *IET Power Electronics*, vol. 7, no. 7, pp. 1787–1796, 2014, doi: 10.1049/iet-pel.2013.0414.
[41] H. Wang *et al.*, "Topology and modulation scheme of a three-level third-harmonic injection indirect matrix converter," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 10, pp. 7612–7622, 2017, doi: 10.1109/TIE.2017.2694386.
[42] L. Wang *et al.*, "A three-level T-type indirect matrix converter based on the third-harmonic injection technique," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 2, pp. 841–853, 2017, doi: 10.1109/JESTPE.2017.2666418.
[43] M. Diaz *et al.*, "Control of wind energy conversion systems based on the modular multilevel matrix converter," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 8799–8810, 2017, doi: 10.1109/TIE.2017.2733467.

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