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Development of numerical model-based photovoltaic emulator for half-cut cell PV panel with multiple peaks output characteristics curve emulation capability

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ABSTRACT

This study introduces a photovoltaic (PV) emulator focusing on a developed numerical model specifically for half-cut cell PV panels under partial shading conditions (PSCs), addressing a gap in research focused on full-cell models. The emulator uses a DC-DC buck converter and PI control to accurately replicate half-cut cell PV panel characteristics. A cost-effective hardware prototype validated the model's effectiveness in emulating multi-peak PV behavior under dynamic PSCs with up to three peaks and user-defined shading. This flexible and affordable platform enables efficient testing of maximum power point tracking (MPPT) algorithms and grid integration for PV systems using increasingly prevalent half-cut cell technology. Simulation results show high accuracy, with MAPE in power as low as 0.175% under uniform irradiance conditions and less than 0.302% under multi-peaks PSCs. Hardware validation confirms reliability with low MAPE in the power of 0.499% under uniform conditions and below 0.614% multi-peak PSCs, demonstrating the developed half-cut cell PV panel numerical model's accuracy in reproducing dynamic shading effects for renewable energy research.

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1. INTRODUCTION

The progressive development of solar photovoltaic technology has been evident. Despite the increasing maturity of solar technology, optimizing the yield of solar generation remains a critical area for ongoing improvement and innovation. One of the most notable advancements in solar technology in recent years is the adoption of half-cut cell technology, which has been widely implemented across the solar industry [1]. This is because half-cut cells can enhance the cell-to-module (CTM) power ratio and reduce the cost of PV panels [2]. Besides, a key advantage of half-cut cell PV panels over traditional full-cell PV panels is the enhanced energy performance of half-cut cell PV panels under partial shading conditions (PSCs) [3]. A study indicates that half-cut cell PV panels outperform full-cell PV panels under PSCs, achieving an increased energy yield ranging from 11.3% to 20.7% [4]. Thus, half-cut cell PV panels dominate the global market, accounting for over 90% of the market share as of 2023 [5].

Optimal energy generation in solar photovoltaic (PV) systems is significantly dependent on the inclusion of maximum power point tracking (MPPT) technology in the associated solar inverter [6]. Bypass

diodes are integrated into PV panels to mitigate the potential for hotspot formation under PSCs [7]. Due to the activation of a bypass diode in a partially shaded PV panel, the electrical behavior is modified, leading to the development of multiple peaks in P-V characteristics. Accurately tracking the maximum power point of a PV panel under complex shading conditions presents considerable difficulty for MPPT algorithms, ultimately impacting the efficiency of solar energy generation. A primary obstacle in testing MPPT algorithms lies in the requirement for a real PV panel, as the fluctuating nature of solar energy makes it difficult to establish consistent and controlled conditions for effective feasibility assessment. To facilitate the research and testing of MPPT algorithms, the development of a PV emulator is crucial. A key feature of such emulators is their capability to simulate the electrical characteristics of PV panels under any user-defined environmental scenario.

The fundamental components of a PV emulator include a DC-DC converter and an integrated PV model operating within a closed-loop control system. The PV model can be developed through methodologies such as numerical model, look-up tables (LUTs), piecewise linear functions, or neural network approaches. Numerical modeling techniques are widely adopted in the development of PV models, primarily attributed to their robustness, traceability, accuracy, and flexibility. The single diode equivalent circuit model represents a particularly common numerical approach, largely due to its inherent simplicity [8]-[17]. However, a significant drawback of employing complex numerical models is their potentially high computational burden. While the LUT method is also frequently employed, it presents significant drawbacks, including a substantial memory requirement for the microcontroller and a lack of inherent flexibility [18], [19]. Its accuracy requires large data storage and lacks adaptability, needing new datasets for each panel and changing conditions. By employing a curve-fitting procedure, the piecewise linear method represents the output characteristic curve of a PV panel through a series of discrete linear segments [20], [21]. While the accuracy of the piecewise linear method improves with an increased number of segments, its practical flexibility is limited by the need for the entire PV output characteristic, rather than readily accessible datasheet values. The neural network methodology is not as frequently employed in PV emulator development due to its dependence on training data obtained from existing datasets [22]. While the hardware implementation of a PV model employing a physical diode offers a direct representation [23], it suffers from significant efficiency losses attributed to diode thermal issues, requiring active cooling to mitigate performance degradation.

A power converter with a PV model embedded in its closed-loop control architecture serves as the power source for a PV emulator intended for real-world applications. The DC-DC buck converter topology is the most employed power converter architecture in the development of PV emulators [11], [13]-[15], [24]-[27]. The DC-DC buck converter is widely used in PV emulator development for its circuit and control simplicity, requiring fewer components. Additionally, it can effectively emulate a broad spectrum of PV output characteristics, provided the input voltage exceeds the PV panel's open-circuit voltage. While [12] utilizes a SEPIC converter with backstepping control, its system design complexity exceeds that of the buck converter due to the incorporation of additional LC elements. Despite its benefits in terms of footprint, isolation, and power extensibility [28], the Single-Mode Power Supply (SMPS) converter implementation is more complex and involves higher costs. Despite the integration of AC/DC supplies and inverters in complete systems, MPPT algorithm testing often requires only a DC-DC converter, as these algorithms are frequently developed using a DC-DC boost converter [29]-[31].

The result [8], emulation of polycrystalline PV panels and amorphous PV panel are carried out. Three modelling techniques are explored for three types of solar cell technologies, namely Amorphous, CdTe and Mono-Si [28]. However, these technologies utilize full-cell technology in the study. While prior full-cell PV emulators achieve multi-peak PV curves, the half-cut cell PV panel features a distinct topology, which is twice the number of sub-strings compared to a conventional panel of the same size. This fundamental change dictates that the equivalent single diode model equations and the resulting multi-peak characteristics under PSCs are inherently different and cannot be accurately replicated by simple rescaling of a full-cell model. The proposed model is novel because it is derived from first principles of this specific electrical architecture, ensuring high fidelity for this modern technology. The current literature, as highlighted by the summary of emulator studies in Table 1, reveals a critical technical gap, which is the absence of a comprehensive PV emulator model validated for the unique, multi-peak output characteristics of the increasingly prevalent half-cut cell technology under complex partial shading. To the best of the authors' knowledge, no prior emulator has validated a numerical model specifically for half-cut cell panels under PSCs.

This paper presents a half-cut cell-based PV emulator designed to emulate the multi-peaked output characteristics of half-cut cell PV panels under PSCs. Utilizing a simplified yet accurate single-diode model, a DC-DC buck converter with an integrated numerical PV model in its closed-loop control with a conventional PI controller ensures robust and rapid response. The major contributions of this paper are presented below:

- Development of a highly accurate numerical model specifically designed to emulate the complex and multi-peak P-V characteristics of half-cut cell PV panels under PSCs.
- Simulation of different shading patterns to shift the maximum power peak to various locations on the P-V curve.
- Design and hardware validation of the model through a cost-effective and high-fidelity PV emulator prototype using the rapid control prototyping TI LAUNCHXL-F28379D microcontroller and PI controller.

By providing a high-fidelity platform for reproducing dynamic shading effects, this work significantly facilitates the rigorous testing of MPPT algorithms and grid integration strategies for PV systems utilizing the increasingly prevalent half-cut cell technology.

Table 1. Summary of recent studies for PV emulators with partial shading emulation ability

Reference	Type of PV model implementation method	PSCs emulation implementation method	Hardware prototype	Solar cell cutting technology
[11] (2020)	Numerical model	-	Buck converter	Full cell
[12] (2020)	Numerical model	-	SEPIC	Full cell
[19] (2020)	Look-up table	Look-up table	Buck converter	Full cell
[28] (2022)	Numerical model / Look-up table	-	SMPS	Full cell
[25] (2022)	Numerical model	Partial shading adjuster	Buck converter	Full cell
Current work	Numerical model	Proposed half-cut cell numerical model	Buck converter	Half-cut cell

2. METHOD

2.1. PV cell reference current equation

The equivalent electrical model of a PV cell, as illustrated in Figure 1, consists of a parallel combination of a current source and a p-n junction diode, connected in series with a resistance. To reduce computational complexity while maintaining acceptable accuracy, the shunt resistance component is neglected in this model [32]. The photocurrent induced by solar irradiance is represented by the current source, and the semiconductor junction properties of the PV cell are modeled by the p-n diode. Power losses within the PV cell are represented by the series resistance (R_{se}) in the equivalent circuit. Applying Kirchhoff's current law to the PV cell equivalent circuit model yields the PV cell reference current (I_{PV}) equation, as presented in (1).

$$I_{PV} = I_{ph} - I_d \left(exp\left(\frac{V_o + (I_o \times R_{se})}{vt}\right) - 1 \right) \quad (1)$$

Where I_{ph} is the photocurrent; I_d is the diode reverse saturation current; V_o is the output voltage; I_o is the output current and vt is the thermal voltage. The photocurrent is represented by (2):

$$I_{ph} = (I_{sc} + \alpha_i (T_{pvc@deg} - T_{STC})) \times \left(\frac{G}{G_{STC}}\right) \quad (2)$$

where G is irradiance in W/m^2; G_{STC} is the irradiance at standard testing conditions; α_i is the temperature coefficient of short-circuit current; $T_{pvc@deg}$ is the operating temperature of the PV cell in degrees Celsius; and T_{STC} at 25 °C. The operating temperature influences the semiconductor properties of the PV cell. This temperature dependence is represented by the thermal voltage (vt), as defined in (3):

$$vt = \frac{A \times k \times T_{pvc@K} \times N_{cs}}{q} \quad (3)$$

where A is the diode ideality factor; k is the Boltzmann constant (1.38 x 10^{-23}); T_{pvc} is the PV cell temperature in Kelvin; N_{cs} is the number of PV cells connected in series; and q is the electron charge (1.6×10^{-19}). To provide sufficient voltage and current, PV panels are generally assembled from numerous PV cells in series-parallel arrangements. The thermal voltage of the panel increases with the number of cells connected in series. By combining (1) and (3) and rearranging the equation, the output voltage of the PV panel can then be represented as (4).

$$V_o = \frac{N_{cs} A k T_{pvc}}{q} \times \ln\left(\frac{I_{ph} - I_o}{I_d}\right) + 1 \quad (4)$$

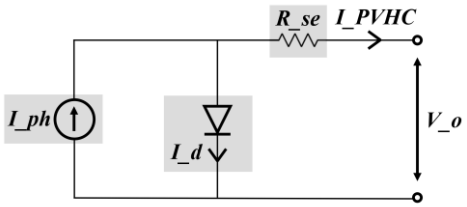


Figure 1. Single diode solar cell model with series resistance

At open circuit conditions, the output current, I_o is zero, and the open circuit voltage, V_{oc} can be derived as (5).

$$V_{oc} = \frac{N_{cs}AkT_{pvc}}{q} \times \ln\left(\frac{I_{ph}}{I_d}\right) + 1 \quad (5)$$

Besides, according to [32], the diode reverse saturation current can be calculated as (6).

$$I_d = \frac{I_{sc@stc} + \alpha_i\,(T_{pvc@deg} - T_{STC})}{exp\left(\frac{q\left(V_{oc@stc} + \beta_v\,(T_{pvc@deg} - T_{STC})\right)}{N_{cs}AkT_{pvc}}\right) - 1} \quad (6)$$

where $V_{oc@stc}$ and $I_{sc@stc}$ are the open circuit voltage and short circuit current at standard test condition (STC – 1000 W/m^2 and 25 °C). PV panel datasheets commonly provide parameters such as V_{oc}, I_{sc}, N_{cs}, α_i, and β_v can be easily obtained from the PV module datasheet. However, R_{se}, and A are usually not provided. To determine these parameters, this research utilized the System Advisor Model provided by NREL which was implemented through the PV Array block within MATLAB Simulink. library. The JA Solar JAM60S01-300/PR PV panel serves as the basis for this study, with its electrical characteristics defined by the parameters in Table 2.

Table 2. Electrical parameters of JA Solar JAM60S01-300/PR from datasheet

Parameter	Value
Diode ideality factor, A	0.94929
Temperature coefficient of short-circuit current, α_i	0.036
Temperature coefficient of open-circuit voltage, β_v	-0.281
Number of cells in series, N_{cs}	60
Open-circuit voltage, V_{oc}	39.85 V
Short-circuit current, I_{sc}	9.75 A
Series resistance, R_{se}	0.33719 Ω

While bypass diodes effectively reduce hotspots in partially shaded PV panels, their activation results in P-V curves exhibiting multi-peaks characteristic with the number of peaks directly corresponding to the number of activated diodes. The architecture of standard PV panels generally includes three bypass diodes as shown in Figure 2, partitioning the PV panel into three cell strings. Shading of an individual cell string activates one of the bypass diodes, consequently yielding a P-V curve with a maximum of three peaks. Under uniform irradiance, the current output of a PV panel with N_{ug} numbers of cell string at the same irradiance level can be calculated as (7).

$$I_{PV} = I_{ph} - I_d\left[exp\left(\frac{q(V + N_{ug}R_{se}I_o)}{N_{ug}N_{cs}AkT_{pvc}}\right) - 1\right] \quad (7)$$

2.2. Half-cut cell PV panels numerical modelling

A half-cut cell PV panel contains twice the number of cells compared to a full cell PV panel, as each cell is bisected. These halves the current of each PV cell, while maintaining the PV cell voltage, resulting in a greater number of cell strings in the half-cut cell PV panel. Similar to a standard full-cell PV panel, the half-cut cell PV panels typically integrate three bypass diodes, dividing the PV panel into three cell strings connected in series. However, each cell string is further divided into two parallel cell strings by each bypass

diode, as illustrated in Figure 2. Thus, the half-cut cell PV panels have a total of six cell strings. Nonetheless, the P-V curves of half-cut cell PV panels still exhibit a maximum of three peaks. Figure 2 depicts the parallel connection of individual bypass diodes to two cell strings. The bypass diodes activate when the respective cell strings experience shading and reduce irradiance. The forward voltage threshold for bypass diode activation is 0.6 V.

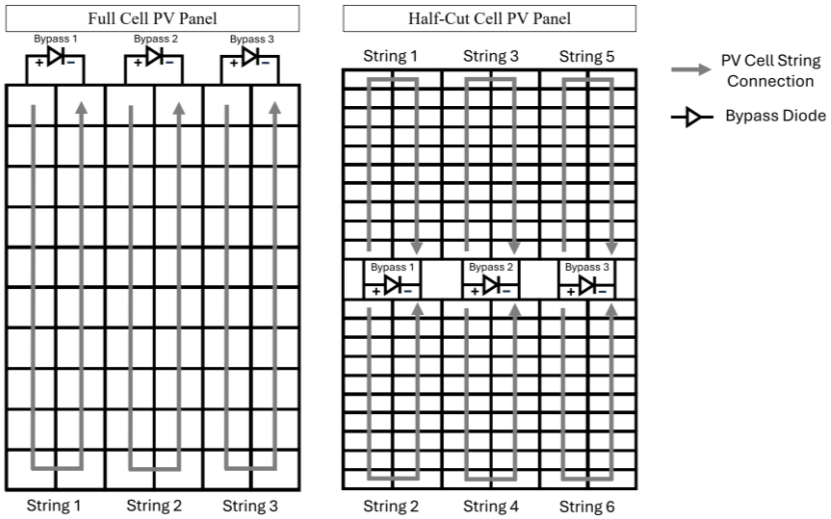


Figure 2. Comparison of full-cell and half-cut cell structures showing parallel sub-string connections

The half-cut PV cell reference current of the parallel connection of bypass diodes across paired cell strings can be derived as (8).

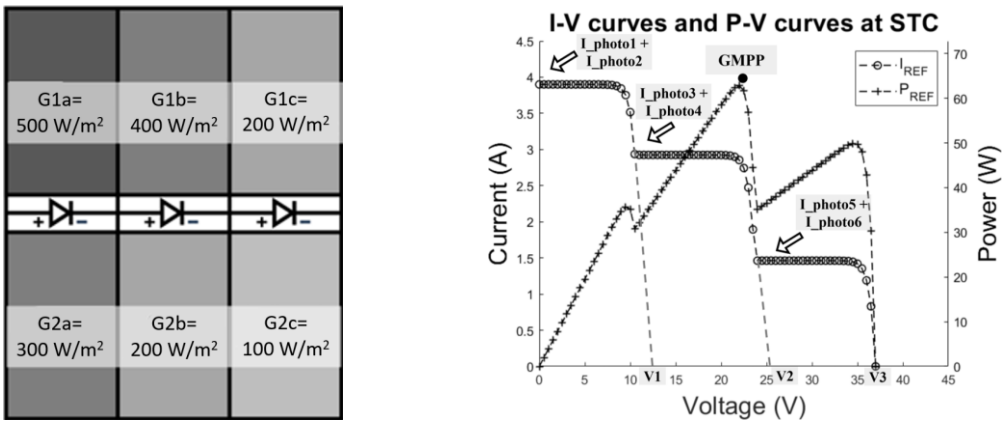
$$I_{PVHC} = \left[I_{ph1} - I_d\left(exp\left(\frac{q(V_o+(I_o \times R_{se}))}{N_{ug}N_{cs}AkT_{pvc}}\right)-1\right)\right] + \left[I_{ph2} - I_d\left(exp\left(\frac{q(V_o+(I_o \times R_{se}))}{N_{ug}N_{cs}AkT_{pvc}}\right)-1\right)\right] \quad (8)$$

Where, I_{ph1} is the photocurrent of cell string 1 connecting to a bypass diode, and I_{ph2} is the photocurrent of cell string 2 connecting to the same bypass diode. If two cell strings sharing a bypass diode experience non-uniform irradiance, the resulting variation in their photocurrents, I_{ph1} and I_{ph2} will vary according to (2). As the PV panel comprises three cell strings connected in series, the V_{oc}, $N_{cs,}$ and R_{se} values provided in Table 2 require division by three for implementation in (8).

Figure 3(a) shows the irradiance distributions applied to the parallel cell strings of each bypass diode, where two specific irradiance distributions are considered: G1 = [500 400 200]; G2 = [300 200 100] W/m². The temperature of all PV panels, $T_{pvc@deg}$ is set at 25 °C. Based on the irradiance distributions illustrated in Figure 3(a), the resulting multi-step I–V curves and multi-peak P–V curves are presented in Figure 3(b). The staircase-like I-V curve is attributed to the bypass diodes activating at different current thresholds dictated by the irradiance levels. By applying (2), I_{ph} at corresponding to different irradiance can be resolved into distinct values, denoted as I_{ph1} to I_{ph6}. The open circuit voltage for each cell string under different irradiance levels, $V_{oc\_irr\_n}$, is calculated using (5) and (6). Given that each bypass diode is connected across two cell strings, two distinct open-circuit voltages will develop when these strings experience different irradiance levels. However, only the minimum of these two voltages is selected. The labelled V_1 to V_3 can be calculated as (9).

$$V_L = \left[\sum_{n=1}^{L} V_{oc\_irr\_min\_n}\right] - (N_{bd} - L)(V_{fd}) \quad (9)$$

Where N_{bd} is the total number of bypass diodes, and V_{fd} is the forward voltage of the bypass diode. This equation is critical as it represents the total open-circuit voltage, which is the sum of the minimum individual open-circuit voltages across each bypass diode where connected cell strings receive different irradiance levels.



(a) (b)

Figure 3. Output characteristics of a Half-cut Cell PV panel under PSCs: (a) half-cut cell PV panel with two specific irradiance distributions for each bypass diode; and (b) multi-step I-V curve and multi-peak P-V curve of the half-cut cell PV panel under PSC, confirming bypass diode activation under PSCs

The proposed PV panel numerical model is detailed in the following three distinct, modularized algorithm stages to enhance clarity and address complexity concerns. The model's numerical procedure is to solve the single diode model and compute the PV panel characteristics curve. Algorithm Stage 1 initializes the parameters and sets up the single diode model. This foundational procedure calculates the necessary electrical parameters from the environmental and reference data and initializes the arrays required for the full IV curve generation. This stage involves the computation of the I_{ph} and V_{oc} for each cell string, considering potential irradiance non-uniformity. The model takes irradiance arrays (G1 and G2) and a temperature array $T_{pvc@deg}$ as inputs for each cell string. For cell strings connected to the same bypass diode, one string receives irradiance G1, while the other receives G2. The photocurrent I_{ph1_irr} is computed based on irradiance level G1, and I_{ph2_irr} is computed based on G2. The open-circuit voltages derived from I_{ph1_irr} and I_{ph2_irr} are compared, and the smaller of the two is stored for the computation of I_{PVHC} for the parallel cell strings. This comparison is important to the half-cut architecture, as finding the limiting voltage of the parallel sub-strings defines the specific inflection points where bypass diodes will activate, setting the foundation for the multi-peak profile.

Algorithm stage 1. Establishes the baseline parameters for the unique parallel sub-string structure

Procedure:	Initialize Cell Parameters
Inputs:	Irradiance 1, *G1*, Irradiance 2, *G2* and temperature arrays, T
Constant:	A, $I_{sc@stc}$, $V_{oc@stc}$, α_i, β_v, N_{cs}, R_{se}, T_{stc}, V_{fd}, k, q, N_{bd}
Declare arrays:	I_d, I_{ph1_irr}, I_{ph2_irr}, V_{oc_irr1}, V_{oc_irr2}, I_{PVHC}, I_{max}
Output:	I_{max}, the maximum current of all I-V curves for each voltage
Logic flow:	1. Calculate parameters for each cell string based on input G1, G2, and $T_{pvc@deg}$, using (5), (6), and (8) 2. Store in their respective values in I_d, I_{ph1_irr}, I_{ph2_irr}, V_{oc_irr1}, V_{oc_irr2} 3. Compare $V_{oc\_irr1}(i)$ and $V_{oc\_irrw}(i)$, and store the smaller value between them as $V_{oc\_irr\_min}$. 4. Initialize declared arrays I_{PVHC} and I_{max}.

Algorithm stage 2 handles the computational grouping of adjacent strings with identical irradiance conditions to reduce redundant calculation and defines the current calculation logic for a specific voltage step. Upon computation of the parameters for each PV panel mentioned in algorithm stage 1, they are stored for subsequent use in I-V curve generation in algorithm stage 2. The core computation for determining the current of the cell strings in the numerical model is performed in algorithm stage 2 and step 3. At each discrete voltage step, the numerical model computes the cell strings' output current by iterating over a voltage range from 1 V to the sum of individual cell string open-circuit voltages. The total I_{PVHC} is the sum of the computed photocurrents, I_{ph1_irr} and I_{ph2_irr}. The algorithmic process for computing the output current utilizes three conditional branches to handle different scenarios. These branches serve as the core mechanism for multi-peak emulation, mathematically replicating the physical activation of bypass diodes to create distinct current steps when shaded sub-strings exceed their voltage limits. For scenario 3(a), when the instantaneous voltage, V surpasses the summed open-circuit voltages of the initial i cell strings, the output current is

assigned to a value of zero. This models the activation of lower-irradiance strings above their voltage limit, excluding their current from I_{max}. While scenario 3(b) checks if the voltage is less than the sum of the open-circuit voltages of all cell strings excluding the N_{ug} grouped strings (where N_{ug} equals 1 for a distinct irradiance i-th string), the current is set to the photocurrent of the i-th cell string. This simulates the low-voltage operation of PV panels, where the output current is mainly dictated by the lower irradiance of the i-th panel. As for scenario 3(c), the output current calculation for voltages beyond the defined conditions is contingent on the uniformity of irradiance across the cell strings. Under uniform irradiance ($N_{ug} = N_{bd}$) across the cell strings, the output current is calculated according to (8). While under non-uniform irradiance across the cell strings, the parameters of individual cell strings are modified to accurately model the irradiance effects. These modifications ensured I-V curves closely match the ideal I-V curves. (10)-(12) are important for computing the output current at each voltage increment:

$$I_{PVHC} = I_{ph} - I_d \left[exp\left(\frac{q\left(V_{mod} + f_{mod} N_{ug} R_{se} I_o\right)}{N_{ug} N_{cs} A k T_{pvc}} \right) - 1 \right] \quad (10)$$

where,

$$V_{mod} = V - \left[\sum_{n=1}^{i-N_{ug}} V_{oc\_irr\_min\ \_n} \right] + (N_{bd} - i)(V_{fd}) \quad (11)$$

$$f_{mod} = \begin{cases} 1 & for\ i = 1 \\ (i)\left(1 + \frac{N_{bd}}{12}\right) & for\ i > 1 \end{cases} \quad (12)$$

where V_{mod} is the modified voltage that accounts for voltage drops across the activated bypass diodes and V_{oc} of the first (i-N_{ug}) cell string of the PV panel; f_{mod} is the modification factor that corrects for varying R_{se} of the operating cell string and the neglected shunt resistance, R_{sh} in the single-diode model. The iterative process also assesses if the I_o of the i-th cell string drops below the photocurrent of the (i+1)-th cell string in the sequence. In such instances, the loop is terminated prior to completion to optimize computational efficiency.

Algorithm stage 2. Computes the individual "steps" of the curve based on bypass diode logic

Procedure:	Calculate IV curves
Inputs:	i (Current panel index), V (Voltage step), N_{ug} (Number of identical adjacent strings), all arrays from Algorithm 1.
Output:	I_{PVHC} (i,V) (Current contribution of the i-th cell string group at voltage V)
Logic Flow:	1. Check if voltage is too high: If V > sum ($V_{oc\_diff\_min}$(1:i)), set I_{PVHC} (i,V) = 0. 2. Check low voltage region: Else if V = 1 or V < sum ($V_{oc\_diff\_min}$(1:i-N_{ug})), set I_{PVHC} (i,V) = I_{ph1_irr}(i) + I_{ph2_irr}(i) 3. Final current calculation at operating region: ELSE a. Uniform condition: If uniform (N_{ug} = N_{bd}), set I_{PVHC} (i,V) according to (8). b. Non-uniform condition: If non-uniform, set I_{PVHC}(i,V) according to (10), (11), and (12). c. Optimization check: If i < N_{bd} and I_{PVHC}(i,V) < I_{ph1_irr}(i) + I_{ph2_irr}(i), break the loop. 4. Return I_{PVHC}(i,V).

Algorithm stage 3 executes the irradiance grouping check, then iterates through voltage steps, and finally performs current matching to determine the maximum current for each voltage step. This stage involves initializing N_{ug} to 1, with N_{ug} denoting the count of adjacent cell strings receiving identical total irradiance. The total irradiance of successive cell strings is compared. If identical, the N_g counter is incremented, grouping these strings to optimize computational efficiency. Algorithm stage 3 step 6: select the maximum current for each voltage point from algorithm stage 2 step 3. This process yields the maximum current array, which the model returns as the I-V curve for the half-cut cell PV panel under given conditions, effectively constructing the final multi-peak curve by dynamically selecting the dominant current path at every voltage step.

Algorithm stage 3. Aggregates the segments to form the final multi-peak curve

Procedure:	Calculate the maximum current by comparing all the I-V curves
Inputs:	N_{bd}, all arrays from Algorithm 1, G1, G2.
Output:	I_{max} (maximum current array/final I-V curve)
Logic Flow:	1. Outer Loop (PV String Grouping Iteration): FOR each PV panel string from 1 to N_{bd}. 2. Initialize grouping: N_{ug} = 1. 3. Irradiance Grouping Check: FOR count equals i to (N_{bd} -1), if G1(i) + G2(i) = G1(count +1)

+ G2(count +1), increment N_{ug}.
4. Skip the for loop if having PV panels with identical irradiance: Increment i by $N_{ug} - 1$,
5. Inner Loop (Voltage Step Iteration): FOR each voltage step V from 1 to sum ($V_{oc\_diff\_min}$):
   a. Call Algorithm 2 to determine $I_{PVHC}(i,V)$.
6. Maximum current selection: After both loops, FOR each voltage V, set $I_{max}(V) = \max(I_{PVHC}(:,V))$
7. Return I_{max}

The three modularized algorithm stages enable accurate simulation of half-cut cell PV panel behavior under non-uniform irradiance. The use of N_{ug} optimizes computation by grouping identical strings. Furthermore, V_{mod} and f_{mod} ensure accurate I-V curves emulation for cell string groups under different irradiance.

2.3. PV emulator simulation in MATLAB/Simulink

To emulate the I-V characteristics of typically high-voltage half-cut cell PV panels, a PV emulator utilizes a DC-DC buck converter to step down the output voltage to the desired operating range. The buck converter controls the equivalent resistance via a feedback loop, aligning the output current with the reference current computed by the numerical model for accurate I-V replication under varying conditions. The buck converter consists of an inductor, a Schottky diode, a capacitor, and a MOSFET, where the MOSFET functions as the fast-switching element controlled by a gate driver. The accuracy of the PV emulator depends on component design. Determining the critical inductance, L, and output capacitance, C_{out} used equations that were derived by modifying the formulas described in (13) and (14) [33].

$$L > \frac{(1-d_{min})R_{load}}{2f} \tag{13}$$

$$C_{out} > \frac{1-d_{min}}{8\gamma L f^2} \tag{14}$$

Where load resistance, R_{load} is determined based on (15).

$$R_{load} = \frac{V_{MPP\,(min)}}{I_{MPP\,(min)}} \tag{15}$$

Where $V_{MPP(min)}$ and $I_{MPP(min)}$ are the maximum power point voltage (28.02 V) and current (0.737 A) of the PV panel under the condition of uniform irradiance of 100 W/m^2 and temperature of 25 °C, respectively. Considering the need for reduced inductor size, compatibility with the TI microcontroller's frequency limitations, and aiming for continuous current mode operation with minimized ripple, the buck converter specifications and design constraints were established as summarized in Table 3.

Table 3. Specifications and control parameters of the PV emulator

Parameter	Value
Switching frequency, f	20 kHz
Inductance, L	2 mH
Output capacitance, C_{out}	47 µF
Minimum duty cycle, d_{min}	0.05
Target output voltage ripple, γ	1%

The PV emulator model was implemented within the MATLAB/Simulink environment, utilizing a built-in buck converter model in the Simulink library, as shown in Figure 4. The half-cut cell PV panel numerical model is integrated into the buck converter's closed-loop control, which utilizes a PI controller, as depicted in Figure 4, to compute duty cycle, D, for MOSFET switching. The deliberately selected standard PI controller serves to validate the proposed model, demonstrating its ability to be accurately emulated without reliance on complex, high-computational-load control schemes. The PV panel numerical model is developed in the MATLAB/Simulink environment using a MATLAB function block based on the three modularized algorithm stages of the proposed half-cut cell PV panel numerical model. The reference current derivation is based on the buck converter's output voltage. This integrated control enables the PV panel's output characteristic emulation across various operating points. PI controller design requires consideration of system dynamics, non-linearities, and desired response time. Proper tuning enhances robustness, stability, and responsiveness for accurate tracking of the PV panel's operating point. The PI controller coefficient is set to 0.13 for the proportional coefficient and 40 for the integral coefficient for simulation in MATLAB/Simulink.

The MATLAB/Simulink simulation was configured with a fixed-step solver and a step size of 1 µs. This configuration ensures compatibility in comparison with the hardware results, as the microcontroller operates exclusively in fixed-step mode. Irradiance inputs are configured via the constant blocks G1 and G2 as depicted in Figure 4. The numerical model requires these values in an array format, where each array element specifies the irradiance for a section of the half-cut cell PV panel, as shown in Figure 3.

A signal builder block was employed to vary the load condition, enabling the generation of the full IV characteristic curve. The dynamic response of the PV emulator was evaluated by subjecting the system to a sudden step change in the operating setpoint as presented in Figure 5. The system exhibits excellent transient behaviour, with output voltage and current successfully reaching steady state with minimal overshoot and a settling time of less than 10 ms. This high-speed dynamic performance serves to validate the entire architecture.

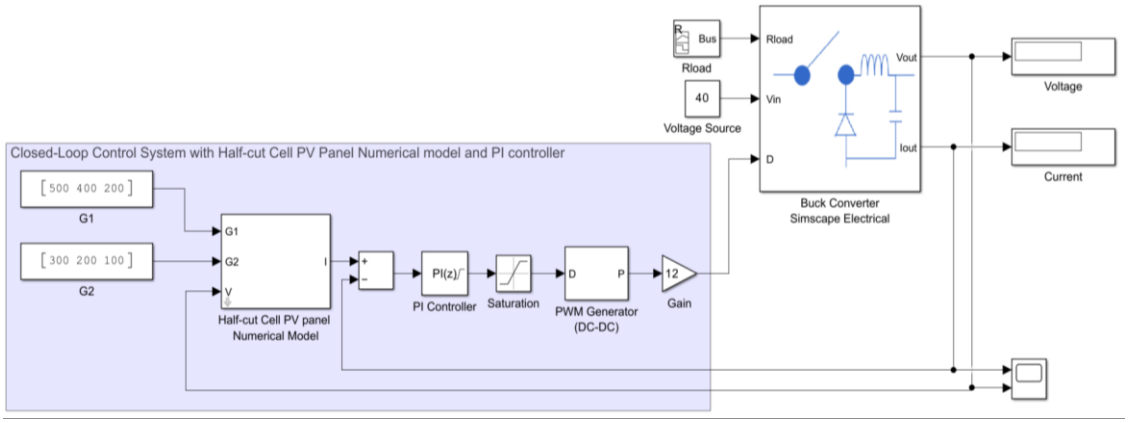


Figure 4. PV emulator simulation model in MATLAB/Simulink with integrated half-cut PV panel numerical model within the closed-loop control system

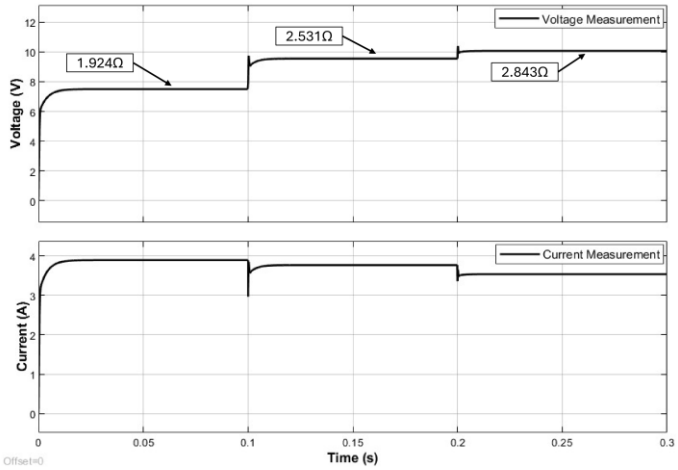


Figure 5. Dynamic response of PV emulator with PSC showing < 10 ms settling time under step change in the operating setpoint changing from 1.924 Ω to 2.531 Ω and to 2.843 Ω

To further assess the viability of the proposed half-cut cell numerical model for real-time applications, the computational burden imposed by the model was quantified via high-resolution timing in the MATLAB simulation environment. The computational load was measured by isolating the time required for the microcontroller to execute the core numerical calculation (Algorithms Stage 1 to 3) to determine a single IV characteristic point. The results confirm an exceptionally low computational load where the model requires only around 5.2 µs to complete one full calculation cycle. The rapid dynamic response and low computational overhead of the novel half-cut cell numerical model confirm that its complexity does not impede real-time execution.

2.4. Hardware implementation

The PV emulator hardware implementation consists of a current-controlled buck converter circuit and a PV emulator controller, as shown in Figure 6. Appropriate component rating selection is critical for the buck converter circuit. Voltage ratings must be higher than the DC source voltage and the PV panel open-circuit voltage, and current ratings must surpass the PV panel short-circuit current. The LC filter of the buck converter utilized a toroidal inductor and an electrolytic capacitor.

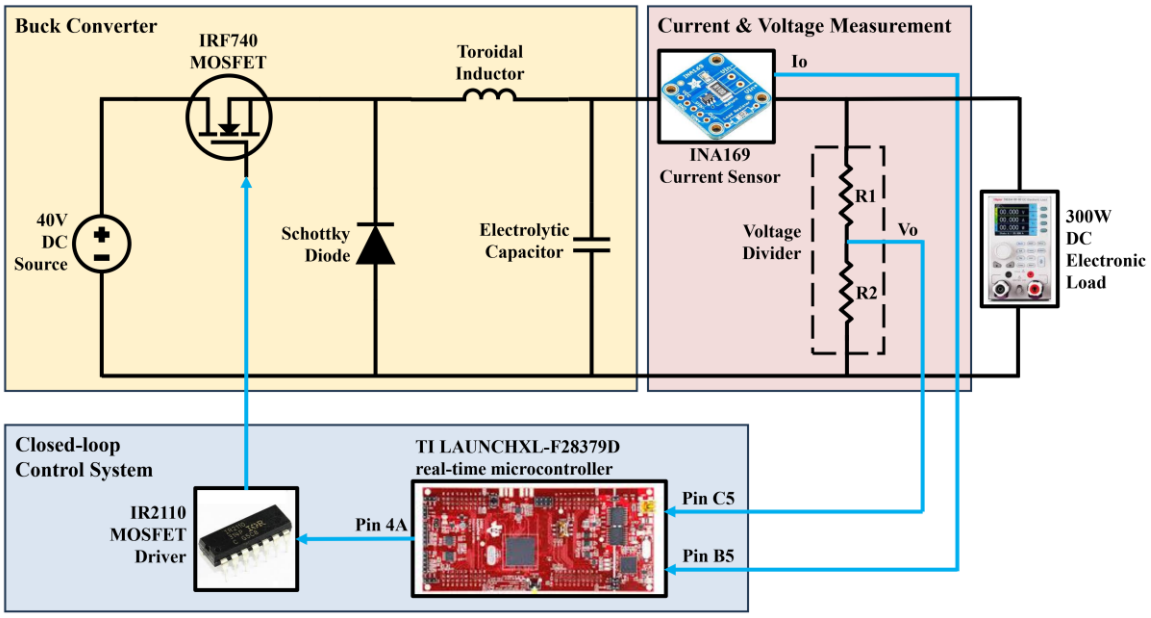


Figure 6. Overview of PV emulator hardware implementation

A MOSFET driver is required to interface the MOSFET (IRF740) gate with the TI LAUNCHXL-F28379D microcontroller. The real-time microcontroller's output signal has insufficient drive strength for the MOSFET, given the buck converter's high input voltage. The IR2110 MOSFET driver is used in this implementation along with a bootstrap circuit for driving the high-side MOSFET [34]. The PV emulator controller utilizes a current sensor and a voltage divider network for current and voltage sensing, respectively. An electronic load with adjustable power dissipation can accommodate the PV emulator's resistance operating point. The PV emulator controller model for the TI LAUNCHXL-F28379D real-time microcontroller was developed in MATLAB/Simulink. Two ADC input pins and one PWM output pin are assigned. Output voltage and current signals from the buck converter circuit are received by the real-time microcontroller's ADC input. To match the microcontroller's 3.3 V maximum analog input and the 12-bit ADC's 4096 resolution, received values are scaled by 3.3/4095. A resistive voltage divider network reduces the buck converter's output voltage to a level compatible with the microcontroller's analog input range. The INA219 DC current sensor was selected for its accuracy and straightforward integration. The duty cycle computed by the PI controller is a normalized value between 0 and 1. Since the real-time microcontroller's ePWM block requires the duty cycle as a percentage, the PI controller's output is scaled by a factor of 100.

The experimental setup of the PV emulator hardware is depicted in Figure 7. The experimental hardware includes a DC-DC buck converter circuit with current sensor and voltage sensing resistive networks, and a TI LAUNCHXL-F28379D real-time microcontroller implementing the PV emulator controller model. The resistive voltage divider composed of R_1 (12 kΩ) and R_2 (1 kΩ) was used to scale the output voltage down to the ADC limit. A 1 ms time step was configured for the real-time microcontroller. The laboratory power supply was used as the DC source, and a 300 W electronic load served as the variable load. Two laboratory power supply units were utilized to achieve a total supply voltage of 40 V, which exceeds the open-circuit voltage of the half-cut cell PV panel specified in Table 2. The electronic load was configured to current-controlled mode to set the load conditions according to the simulation results, thereby enabling direct comparison. The controller model was deployed to the real-time microcontroller using MATLAB/Simulink. The output voltage and current of the PV emulator were monitored via the electronic load display to generate PV characteristic curves under specified load conditions. The PI controller's

proportional and integral coefficients were set to 0.05 and 10, respectively, for hardware validation. The lower PI coefficient values were sufficient to achieve the desired dynamic response, given the real-time operational characteristics of the microcontroller and hardware.

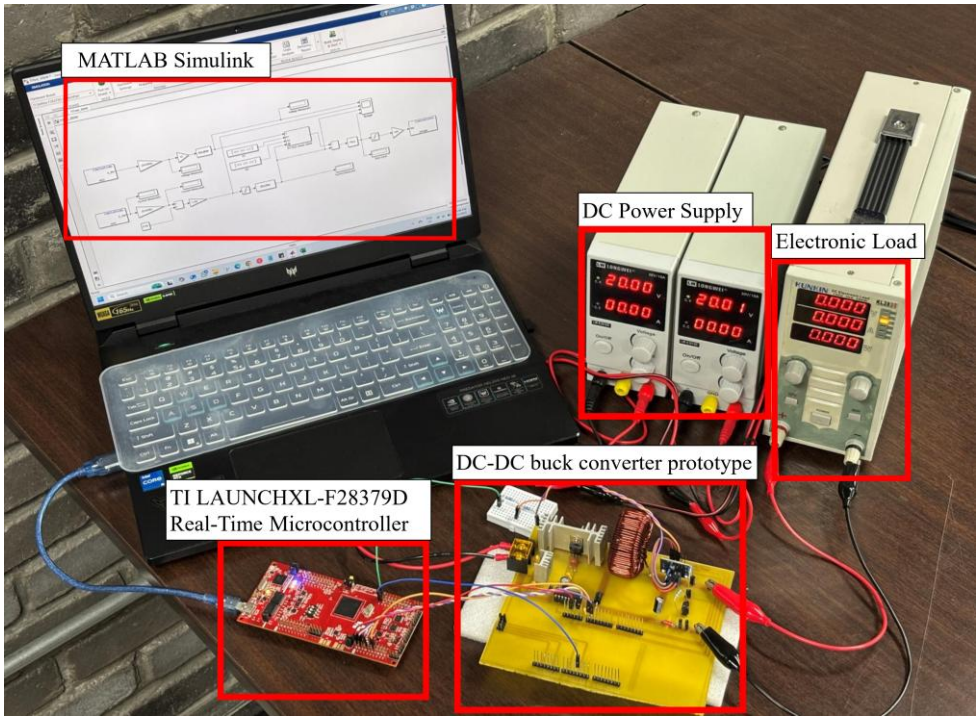


Figure 7. PV emulator hardware prototype setup

3. RESULTS AND DISCUSSION

The characteristic curves obtained from the developed half-cut cell PV panel numerical model through simulation in MATLAB/Simulink provide the primary reference for evaluating the curves generated by the proposed PV emulator. This methodology establishes a three-stage validation hierarchy where the PV panel model simulation serves as a theoretical reference and is first used to confirm the accuracy of the PV emulator simulation developed in MATLAB/Simulink. Both are then used to validate the PV emulator hardware prototype results for real-time validation. The half-cut cell PV panel numerical model was tested with various irradiance input arrays to simulate I-V and P-V characteristic curves under both uniform irradiance (all cell strings of the PV panel received 500W/m^2 irradiance) and PSCs, resulting in multi-peak as presented in Figure 8. The partial shading conditions (PSC1, PSC2, PSC3, and PSC4) are designed to simulate the effects of uneven heavy soiling, resulting in random irradiance distributions across the PV panels. The GMPP is located on the low voltage side (LVS) for PSC1, in the middle of the multi-peak curve for PSC2, on the high voltage side (HVS) for PSC3, and PSC4 exhibits similar GMPP and LMPP. The characteristic curves obtained from the half-cut cell PV panel numerical model through simulation in MATLAB/Simulink provide a reference for evaluating the curves generated by the proposed PV emulator. PSCs exhibiting up to three peaks present a significant challenge for evaluating the proposed PV emulator's feasibility in accurately emulating multi-peak P-V characteristic curves.

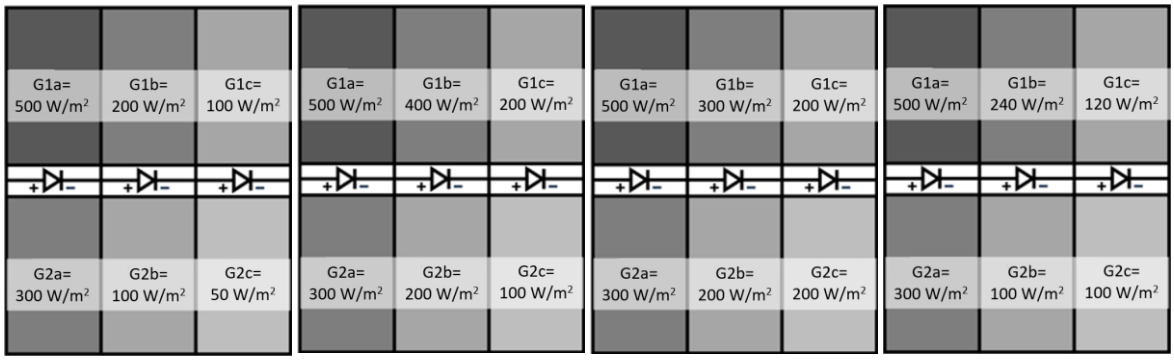
3.1. Performance evaluation of the proposed PV emulator

To evaluate the PV emulator's accuracy, the mean absolute percentage error (MAPE) was employed as a performance metric, calculated as (16).

$$MAPE = \frac{\sum_{V=1}^{V_{oc}} \frac{|P_{ref}(V) - P_{sim}(V)|}{P_{ref}(V)}}{V_{oc}} \times 100\% \quad (16)$$

Figure 9 presents a comparative analysis between the reference half-cut cell PV panel numerical model, the Simulink simulation results, and the hardware verification results of the proposed PV emulator. Simulink

simulation is conducted under uniform irradiance and four PSCs with multi-peak, namely, PSC1, PSC2, PSC3, and PSC4, to assess the PV emulator's performance in accurately reproducing I-V and P-V characteristic curves through simulation. Furthermore, hardware prototyping was conducted to validate the functionality and system characteristics of the proposed PV emulator, aiming to verify its practical applicability and assess its accuracy in replicating the I-V and P-V characteristic curves. The PV emulator, which employs the half-cut cell PV panel numerical model, is validated against these multi-peak test cases.



(a) (b) (c) (d)

Figure 8. Multi-peak test cases with GMPP location shifts under uneven soiling PSCs: (a) PSC1 (GMPP at LVS), (b) PSC2 (GMPP at middle), (c) PSC3 (GMPP at HVS), and (d) PSC4 (similar LMPP and GMPP)

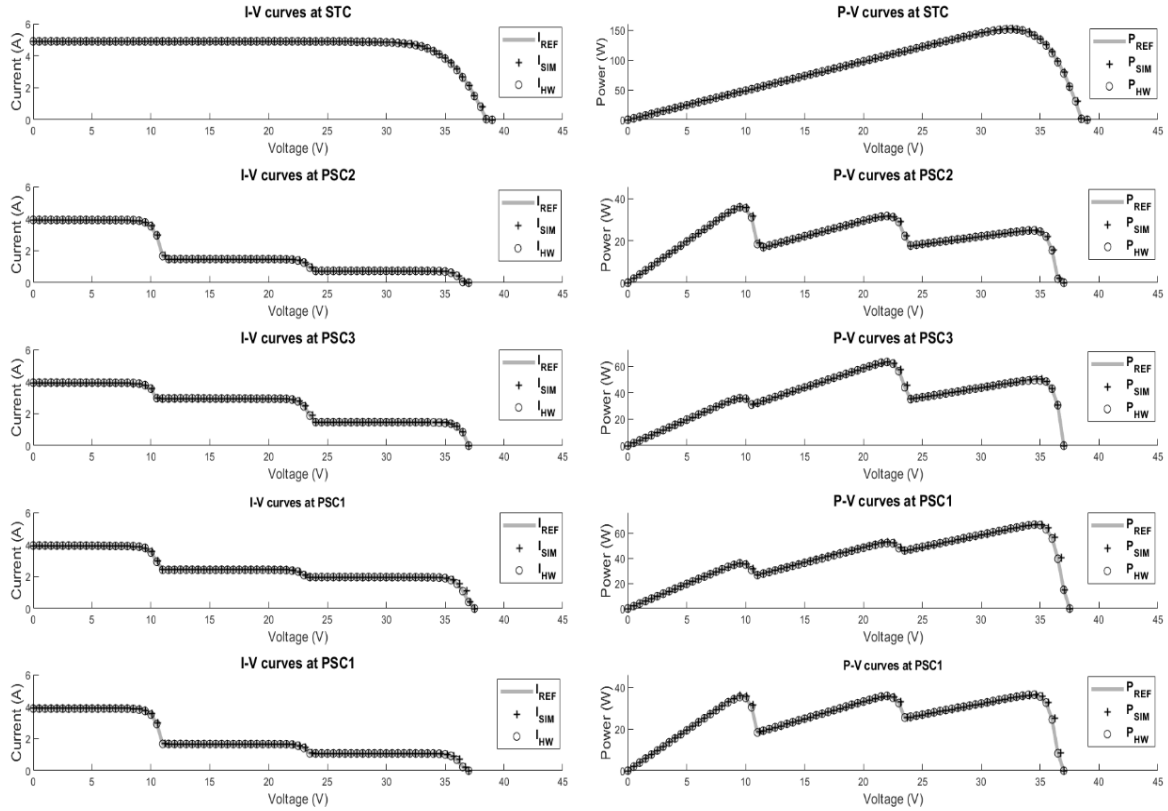


Figure 9. Performance evaluation confirming the accuracy of the proposed PV emulator under MATLAB/Simulink simulation and hardware validation against the reference numerical model

Table 4 summarizes the power performance metrics, MAPE for the conducted test cases. Under uniform irradiance conditions, the recorded power error is 0.175% for the simulation and 0.499% for the hardware prototype. The low error values suggest that the PV emulator accurately replicates the I-V curve

profile, with only minor discrepancies observed in the power calculation. In the scenarios of the four PSC test cases, the error levels consistently stayed within acceptable limits. Specifically, the power error for Simulink simulation is 0.262% for PSC1, 0.226% for PSC2, 0.223% for PSC3, and 0.302% for PSC4. As for the hardware prototype, the power error is 0.597% for PSC1, 0.555% for PSC2, 0.584% for PSC3, and 0.614% for PSC4. Consistently elevated MAPE values were observed in the hardware prototype compared to Simulink simulations. This difference indicates reasonable hardware performance, considering real-world limitations like component operating efficiency and signal noise. These results directly address the technical gap highlighted previously regarding the absence of validated models for half-cut cell technology. By achieving low error rates (<0.62%) while accurately emulating the unique multi-peak behavior of the half-cut topology, the proposed emulator fulfills the study's primary contribution of providing a high-fidelity platform for modern PV system research.

The achieved hardware MAPE of less than 0.62% is highly competitive with existing full-cell PV emulators, which typically exhibit comparable error ranges [11], [25]. Moreover, unlike look-up table (LUT) based approaches that suffer from quantization errors and limited flexibility [19], this numerical model ensures continuous and precise tracking of the unique multi-peak characteristics inherent to half-cut cells without resolution limits. The ability to reliably reproduce these complex shading scenarios in a controlled laboratory environment significantly accelerates MPPT algorithm development. It eliminates the dependency on unpredictable weather conditions and the logistical challenges of large-scale field testing, providing a standard platform for benchmarking algorithm performance against the specific challenges posed by half-cut cell technology.

Despite the low computational overhead of 5.2 μs for a single panel, it is important to note that the iterative nature of the numerical model demands more processing cycles than simple analytical equations. Thus, scaling this specific approach to emulate large-scale PV arrays may linearly increase the computational burden, potentially requiring high-performance processors or distributed control architectures for real-time execution.

Table 4. Summary of performance metrics for MATLAB/Simulink simulation and hardware prototype, confirming the accuracy of the proposed PV emulator

Test Cases	MAPE for Simulink simulation (%)	MAPE for hardware prototype (%)
Uniform	0.175	0.499
PSC1	0.262	0.597
PSC2	0.226	0.555
PSC3	0.223	0.584
PSC4	0.302	0.614

4. CONCLUSION

This study developed and validated a numerical model-based PV emulator tailored for half-cut cell PV panels, addressing the critical challenge of accurate emulation under partial shading conditions. The proposed numerical model accounts for the unique electrical configuration and performance attributes inherent to half-cut cell technology, which are increasingly prevalent in modern PV systems due to their enhanced efficiency and shading tolerance. By integrating a numerical model of the half-cut cell PV panel with a PI-controlled DC-DC buck converter, the proposed emulator accurately reproduces multi-peak P-V curves, showcasing its ability to effectively mimic panel behavior under diverse shading conditions. Simulation and experimental results confirm that the integration of a half-cut cell PV panel numerical model within a PI-controlled DC-DC buck converter accurately replicates the output behavior of such panels under diverse shading patterns, highlighting the PV emulator's practicality. This work successfully delivers three novel technical results: 1) a highly validated numerical model for the contemporary half-cut cell PV panel configuration; 2) a simplified PI-controlled DC-DC buck converter solution capable of real-time emulation of complex curves with up to three distinct peaks; and 3) a low-cost hardware platform that offers a flexible and high-accuracy alternative for MPPT algorithm testing and development under realistic PSCs. The performance evaluation demonstrated high accuracy, with MATLAB/Simulink simulations exhibiting an MAPE consistently below 0.302%. Furthermore, hardware verification confirmed the prototype’s fidelity under real-world conditions, maintaining a MAPE of less than 0.614% across all tested shading scenarios. Besides, Hardware verification results validate the appropriate sizing methodologies employed in the development of the prototype. As the PV industry increasingly standardizes half-cut cell technology to maximize energy yield, the availability of such validated emulation tools becomes critical for ensuring the reliability and efficiency of next-generation renewable energy systems. The PV emulator's robust and accurate capture of half-cut cell PV panel characteristics under partial shading conditions establishes it as a reliable tool for MPPT algorithm testing, thus accelerating the research and development of MPPT technologies. It is noted that this validation utilizes a specific commercial half-cut panel and a classical PI controller. Future research directions include scaling the proposed model to emulate large-

scale PV arrays, implementing advanced control strategies such as model predictive control (MPC) or artificial neural networks (ANN), and conducting uncertainty quantification to assess model robustness against parametric variations.

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AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

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C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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