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Interleaved buck converter using a floating dual series-capacitor topology

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ABSTRACT

Interleaved buck converters (IBC) are widely utilized in step-down voltage applications due to their excellent performance and straightforward design. However, conventional IBCs require individual current sensors and feedback control circuits to maintain phase current balance, resulting in increased cost and design complexity. In this paper, a novel floating dual series capacitor (FDSC) converter based on an interleaved floating structure is proposed. The most distinctive aspect of this proposed converter is its ability to naturally balance the four inductor currents without the need for any current sensors or feedback control. Furthermore, the proposed converter also exhibits lower voltage stress on switching devices and inductors, contributing to improved efficiency and a reduction in overall magnetic volume. To validate the performance characteristics of the proposed converter, a 1.3 kW prototype of the FDSC topology was developed and tested to indicate the analytical results and demonstrate stable current balance even under different operating conditions. The experimental validation highlights the topology's suitability for high step-down, compact, and efficient applications such as EV auxiliary power supply and voltage regulator modules.

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1. INTRODUCTION

Electric vehicles (EVs) have gained significant popularity in today's market. These vehicles typically operate using high-voltage battery packs, commonly at 400 V or even up to 800 V, to deliver the necessary power for propulsion. Despite this, low-voltage lead-acid batteries are still employed to supply energy to the vehicle's control and infotainment systems, primarily due to their proven reliability [1]. However, lead-acid batteries pose environmental hazards and are increasingly inadequate in meeting the rising energy demands of modern, feature-rich EV systems. As a result, extensive research is being conducted to develop power converters capable of stepping down high-voltage battery output directly to low-voltage levels, aiming to eliminate the need for traditional auxiliary batteries in electric vehicles [2], [3].

Step-down conversion using transformers is widely employed, especially in applications requiring electrical isolation or large voltage conversion ratios. Transformer-based topologies, such as flyback and forward converters, offer flexibility in design and are well-suited for high-voltage or isolated systems. However, in certain scenarios particularly when isolation is not required and the voltage step-down ratio is moderate direct step-down converters like the buck topology provide superior efficiency, reduced component

count, and lower cost [4]–[6]. As a result, direct conversion methods remain a favorable choice in compact, low-to-medium power applications.

The buck converter is a widely used non-isolated topology that efficiently steps down the input voltage to a lower output level. The presence of an output inductor in this topology ensures continuous output current, which is a critical feature in DC/DC converters. To enhance output power, interleaved buck converters (IBC) are widely used. IBC is constructed by combining conventional buck converters in parallel using interleaved switching [7]–[10]. The interleaving effect significantly reduces output current fluctuations. This enables a smaller L-C filter and faster dynamic response [11], [12]. However, even a slight mismatch in gate signals between buck converters can lead to unbalanced inductor currents in the IBC. These studies attempt to address the issue of current imbalance among inductors; however, they require additional current sensors and more complex control methods [13]–[16]. Buck converter achieves high efficiency when the output voltage is not significantly lower than the input voltage. However, as the voltage conversion ratio increases, the efficiency of the converter declines markedly. Moreover, all switches and diodes in the IBC must withstand the high input voltage, resulting in significant switching loss when operating at high frequencies [17]–[20]. Consequently, for applications demanding large voltage step-down ratios, alternative converter topologies with superior conversion capabilities are typically preferred.

The series capacitor (SC) converter as shown in Figure 1 and presented in [21], [22] offers solutions to the issues faced by the IBC. To begin with, the SC converter has twice the voltage gain while imposing lower voltage stress on the semiconductor devices. Specifically, the voltage stress on switch S_2, diodes D_1 and D_2 is only $V_{in}/2$. This is achieved because the capacitor C_1 is withstanding half of the input voltage, which is $V_{in}/2$. Secondly, due to the charge-discharge equilibrium of capacitor C_1, the current flowing through the two inductor L_1 and L_2 is inherently balanced. However, the aforementioned advantage is only realized when the duty cycle is less than 0.5 [23]. In fact, when the duty cycle exceeds 0.5, the voltage stress on the switching devices increases significantly, and the function of balancing inductor currents is lost [24], [25]. Chen *et al.* [26] attempted to enhance the performance of the conventional SC converter by proposing a multiphase SC configuration. However, the main drawback of this approach is that as the number of phases increases, the operating range becomes more restricted, since the maximum duty cycle is limited to 1/n, where n is the number of phases.

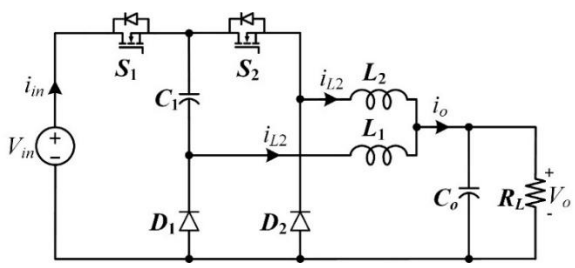

Figure 1. Series capacitor (SC) converter

Several studies have instead explored the interleaved floating (IF) structure [26]–[28], which connects two complementary cells of a converter in a floating-input, parallel-output manner. This configuration maintains current balance between phases while achieving a higher conversion ratio, without further narrowing the operating range of the converter. However, for successful interconnection, the configured connection must include both N-cell and P-cell types, as illustrated in Figure 2. Notably, these two converter types exhibit identical electrical characteristics. Forest *et al.* [29] sought to enhance the capacity by extending the IF structure to four phases. However, the phase currents were not inherently balanced, requiring additional current sensors and feedback loops.

In this paper, a floating dual series capacitor (FDSC) converter based on an interleaved floating structure is proposed, as illustrated in Figure 3. The converter is developed by integrating SC cells into an interleaved floating structure to achieve a higher conversion ratio and increase the output power. The proposed converter is engineered to maximize voltage gains and minimize voltage stress on the switching devices, resulting in reduced switching losses and improved efficiency, especially in high conversion ratio applications. Moreover, the proposed converter also has the current balancing feature that naturally equalizes the currents in the four inductors without requiring feedback control or sensing circuits.

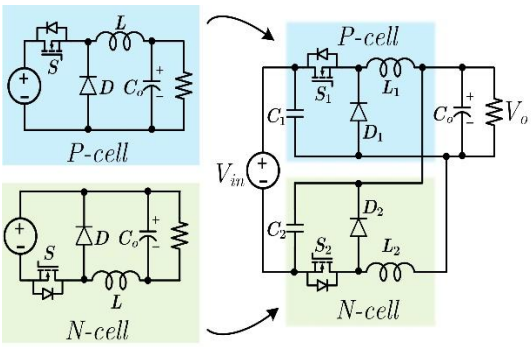

Figure 2. Interleaved floating (IF) structure

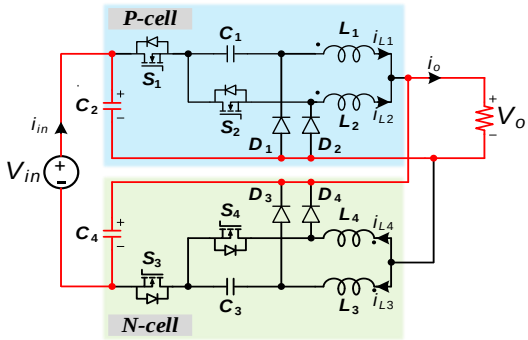

Figure 3. The proposed FDSC converter

2. OPERATION OF THE NOVEL CONVERTER

The proposed FDSC converter, shown in Figure 3, is built by connecting two SC converters called the P-cell and N-cell with floating inputs and parallel outputs. The four operating modes of the FDSC converter are illustrated in Figure 4 and their key waveforms are shown in Figure 5. As illustrated in Figure 5, both cells use the same gate driving signals, but with a 90° phase shift. As the voltage and current waveforms of the P-cell and N-cell are identical, only the representative waveforms of the P-cell are shown for clarity. Furthermore, due to the inherent limitations of the SC converter, the duty cycle of the FDSC is restricted to $D < 0.5$ in this study.

[Mode 0, Figure 4(a)]: All the switches are turned off while all the diodes are turned on. The current flows through the load by the loops L_1-V_o-D_1 and L_2-V_o-D_2. The two capacitors C_2 and C_4 are charged through the loop V_{in}-C_2-V_o-C_4. The instantaneous voltage across each inductor is equal to -V_o. Therefore, the inductor currents i_{L1} and i_{L2} decrease in this mode.

$$\begin{cases} V_{L1} = -V_o \\ V_{L2} = -V_o \end{cases} \tag{1}$$

[Mode 1, Figure 4(b)]: S_1 and D_2 are turned on while S_2 and D_1 are turned off. In this mode, capacitor C_1 is charged from C_2 with a current equal to i_{L1} flowing through the loop S_1-C_1-L_1-V_o-C_2. The inductor L_2 continues discharging through the loop L_2-V_o-D_2. In this mode, the voltage across L_1 is positive, while that across L_2 is negative. The inductor voltage can be expressed as:

$$\begin{cases} V_{L1} = V_{C2} - V_{C1} - V_o \\ V_{L2} = -V_o \end{cases} \tag{2}$$

[Mode 2, Figure 4(c)]: S_2 and D_1 are turned on while S_1 and D_2 are turned off. The capacitor C_1 discharges through the loop C_1-S_2-L_2-V_o-D_1, delivering a current equal to i_{L2}. The current of inductor L_1 circulates through the loop L_1-V_o-D_1. In contrast to Mode 1, the voltage across L_1 becomes negative while that across L_2 becomes positive, as shown (3).

$$\begin{cases} V_{L1} = -V_o \\ V_{L2} = V_{C1} - V_o \end{cases} \tag{3}$$

[Mode 3, Figure 4(d)]: All the diodes are turned off while all the switches are turned on. The current flows through the load by the loops L_1-V_o-C_2-S_1-C_1 and L_2-V_o-C_2-S_1-S_2. The two capacitors C_2 and C_4 are charged through the loop V_{in}-C_2-V_o-C_4. The inductor currents i_{L1} and i_{L2} increase in this mode. In this mode, the voltage across both inductors is positive. The inductor voltages can be expressed as:

$$\begin{cases} V_{L1} = V_{C2} - V_{C1} - V_o \\ V_{L2} = V_{C2} - V_o \end{cases} \tag{4}$$

In the FDSC converter, capacitor C_1 acts as an intermediate energy storage element: it stores energy by charging in series with inductor L_1 during Mode 1 and releases this energy to L_2 during Mode 2. Thus, the energy delivered to L_1 and L_2 is precisely the energy exchanged in capacitor C_1.

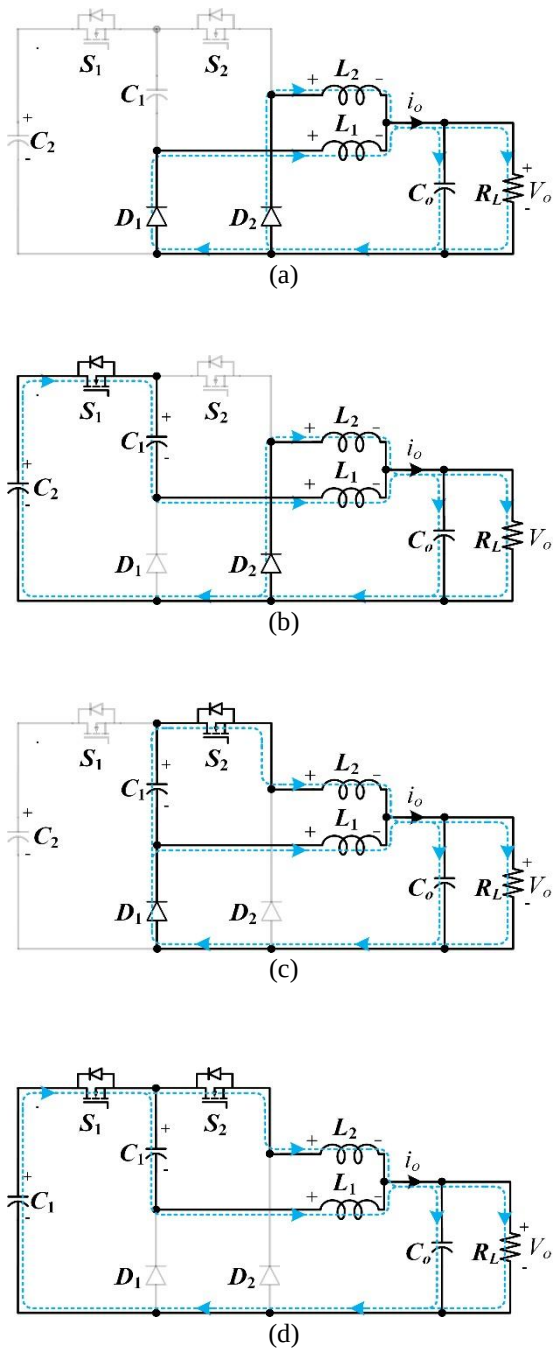

Figure 4. Operation modes of *the* P-cell SC converter*:* (a) mode 0, (b) mode 1, (c) mode 2, and (d) mode 3

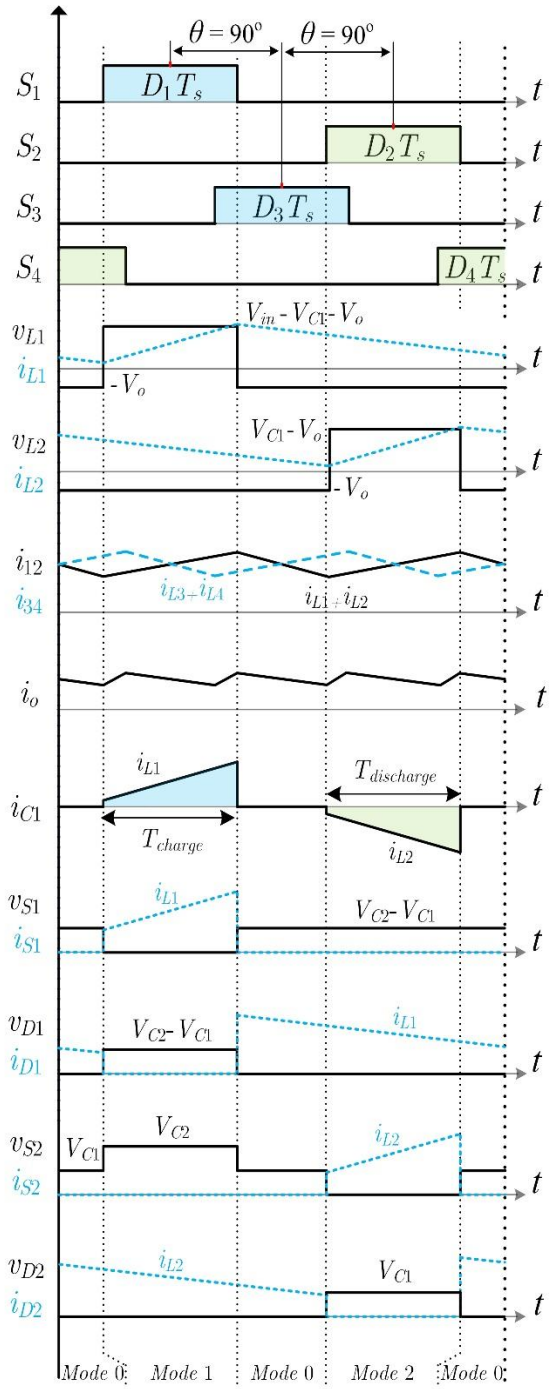

Figure 5. Key waveforms of the proposed converter

3. CHARACTERISTICS OF THE FDSC CONVERTER

3.1. Voltage gain

When $D < 0.5$, the durations of Mode 1 and Mode 2 are equal, each lasting DT_s. Mode 0 operates for (1-2D) T_s. The voltages of inductors L_1 and L_2, denoted as v_{L1} and v_{L2}, are illustrated in Figure 5. It can be observed that, within each switching cycle, the inductor voltage alternates between positive and negative intervals. According to the flux (volt–sec) balance condition, the average inductor voltage over one switching period must be zero. In other words, the area of the positive portion (voltage × time) must be equal to that of the negative portion. Therefore, the voltage across the two inductors can be expressed as (5).

$$\begin{cases} V_{L1_{Mode\,1}} DT_s = -V_{L1_{Mode\,0}}(1-2D)T_s - V_{L1_{Mode\,2}} DT_s \\ V_{L2_{Mode\,2}} DT_s = -V_{L2_{Mode\,0}}(1-2D)T_s - V_{L2_{Mode\,1}} DT_s \end{cases} \quad (5)$$

By substituting (1)–(4) into (5), the voltages across C_1 and C_2 are obtained.

$$\begin{cases} V_{C1} = \frac{V_o}{D} \\ V_{C2} = \frac{2V_o}{D} \end{cases} \qquad 0 < D \leq 0.5 \quad (6)$$

The voltage across C_1 is always half of that across C_2. Consequently, C_1 blocks half of the switch voltage during operation, thereby reducing voltage stress on the switching devices. Since the properties of the N-cell and P-cell SC are identical, the voltages across C_3 and C_4 correspond to those of C_1 and C_2, respectively. From the V_{in}–C_2–V_o–C_4 loop shown in Figure 3 (red loop), the output voltage of the proposed FDSC converter is obtained as (7).

$$V_o = V_{C2} + V_{C4} - V_{in} \quad (7)$$

Based on (6) and (7), and considering the symmetry between the P-cell and N-cell, it leads to $V_{C2} = V_{C4}$, $V_{C1} = V_{C3}$. The output voltage of the proposed converter can be expressed as (8).

$$V_o = \frac{DV_{in}}{(4-D)} \quad (8)$$

From (8), it is evident that the FDSC converter can step down a large input voltage to a much smaller output voltage with a very high conversion ratio, exceeding 7 times. In contrast, achieving the same ratio with a conventional buck converter would require an extremely small duty cycle. Figure 6 compares the voltage gain of the proposed converter with that of a conventional buck converter, showing that the FDSC consistently achieves a higher conversion ratio at the same duty cycle. It is also well known that the efficiency of step-down converters decreases significantly when the duty cycle becomes extremely low. By attaining a high conversion ratio without resorting to such low duty cycles, the proposed converter offers superior suitability for high step-down applications compared with conventional designs

3.2. Inductor current balancing

As shown in Figure 5, the charge and discharge time of the proposed converter are equal to DT_s. Following the charge balance condition for capacitor C_1, the charge and discharge areas of capacitor C_1 must be equal. Moreover, the capacitor C_1 is charged and discharged by i_{L1} and i_{L2}, respectively. Therefore, the average current of L_1 and L_2 are equal. It is similar for I_{L3} and I_{L4}.

As mentioned in Forest *et al.* [29], the two cells of the proposed converter are also naturally balanced by the special input floating output parallel structure. Thus, the four average inductor currents in the proposed converter are given by:

$$I_{L1} = I_{L2} = I_{L3} = I_{L4} = \frac{I_o + I_{in}}{4} \quad (9)$$

As indicated by (9), the converter inherently maintains balanced inductor current without requiring any supplementary sensors or control algorithms, thereby simplifying the system and ensuring power equilibrium.

3.3. Inductor current ripples of the proposed converter

From inductor current waveforms in Figure 5, the inductor current ripple of L_1 to L_4 can be given as (11).

$$\Delta i_{L1-4} = \frac{V_o}{Lf_{sw}}(1-D) \quad (11)$$

where: L is the inductance of inductors L_1–L_4. These inductors are normally selected with equal values to ensure optimal interleaving performance. f_{sw} is the switching frequency of the converter. To achieve the best interleaving effect, the phase currents of the converter must be equal in magnitude and evenly phase-shifted [30], [31]. In the case of the proposed FDSC converter, which operates with four phases, the phase shift between adjacent phases is 90°. The output current ripple of the proposed converter can be expressed as:

$$\Delta i_o = \begin{cases} \frac{(1-4D)V_o}{Lf_{sw}} & 0 < D \leq 0.25 \\ \frac{(1-2D)(4D-1)V_o}{2DLf_{sw}} & 0.25 < D \leq 0.5 \end{cases} \quad (12)$$

Figure 7 illustrates the output current ripple of the proposed converter in comparison with that of the four-phase interleaved buck converter (4P-IBC). Both converters are evaluated under identical conditions, including the same conversion ratio and inductor value. It is observed that the proposed converter exhibits a significantly lower output current ripple than the 4P-IBC. This improvement is attributed to the fact that the voltage across the inductor in the proposed topology is lower than that in a conventional 4P-IBC. Consequently, the FDSC converter allows for a reduction in both the inductance $L_{1\text{-}4}$ and the output capacitance C_o, thereby enhancing the dynamic response of the system.

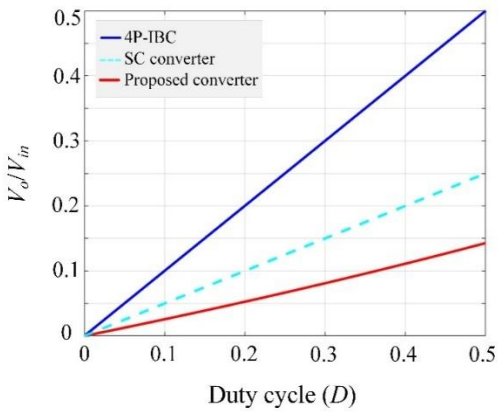

Figure 6. Voltage gain of the 4P-IBC, SC, and proposed converter

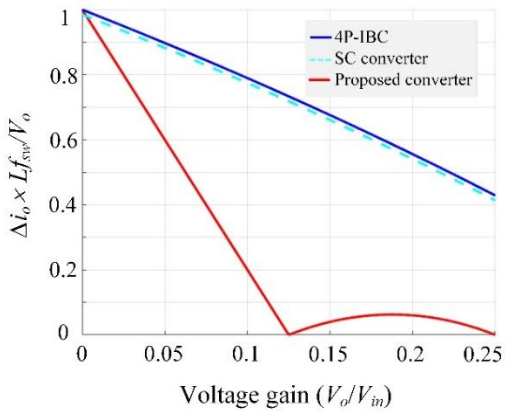

Figure 7. Output current ripple of the 4P-IBC, SC, and proposed converter

3.4. The converter characteristics

Table 1 provides a comprehensive comparison between the proposed FDSC and other converters, including the four-phase interleaved buck converter (4P-IBC), the series capacitor (SC) converter, and the coupled-inductor buck (CIB) converter. In terms of operating range, the proposed FDSC is restricted to duty cycles below 0.5, which is narrower than that of the other converters. Nevertheless, this limitation is offset by several remarkable advantages. Specifically, the FDSC exhibits the lowest voltage stress on semiconductor devices, ensuring improved efficiency. Moreover, it inherently achieves self-balancing of the output voltages across all four phases without requiring additional control circuits. Beyond that, the proposed topology attains the highest conversion ratio among the compared configurations, while simultaneously producing the smallest output voltage ripple, making it highly attractive for high step-down, high-efficiency applications.

Table 1. Comparison between the FDSC and other converters

Converters		FDSC (Proposed converter)	4P-IBC (**)	SC (**)	CIB (**)
Duty cycle (D)		$0 < D \leq 0.5$	$0 < D < 1$	$0 < D \leq 0.5$	$0 < D < 1$
Voltage stress (*)	S_1, S_3	$\frac{V_{in}}{(4-D)}$	V_{in}	$\frac{V_{in}}{2}$	V_{in}
	S_2, S_4	$\frac{2V_{in}}{(4-D)}$	V_{in}	V_{in}	V_{in}
	D_1, D_3	$\frac{V_{in}}{(4-D)}$	V_{in}	$\frac{V_{in}}{2}$	V_{in}
	D_2, D_4	$\frac{V_{in}}{(4-D)}$	V_{in}	$\frac{V_{in}}{2}$	V_{in}
Voltage gain $\left(\frac{V_o}{V_{in}}\right)$		$\frac{D}{(4-D)}$	D	$\frac{D}{2}$	D
Output current ripple (Δi_o)		Lowest	Medium	High	Low
Current balancing		Yes	No	Yes	No

*note: In both SC and CIB, only the devices S_1, S_2, D_1, and D_2 are present; **4P-IBC : Four phase interleaved buck converter; SC : Series capacitor converter; CIB : Coupled inductor buck converter

4. EXPERIMENTAL VERIFICATION

A 1.3 *k*W FDSC converter, as shown in Figure 8, was built and tested. The experimental results are shown in Figures 9–12 and the converter parameters are presented in Table 2. The converter was designed to work over a wide input voltage range (from 300 to 450 V) while the output voltage was controlled at 45 V. The gate signals of S_1 to S_4 are shifted by 90°.

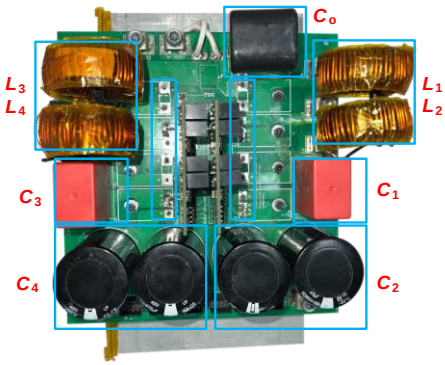

Figure 8. The prototype of FDSC converter

Table 2. Experimental parameters

Symbol	Value	Symbol	Value
V_{in}/V_o	300 – 450 *V*/45 *V*	C_1, C_3	4.4 μF
P_{out}	1.3 *kW*	C_2, C_4	100 μF
f_{sw}	55 *kHz*	L_1, L_2, L_3, L_4	250 μH
S_1–S_4	SCT3060AR	D_1–D_4	SCS320AM2

Figure 9 shows the experimental waveforms of inductor currents (i_{L1}, i_{L2}, i_{L3}, and i_{L4}) and semiconductor device voltages (v_{S1}, v_{D1}, v_{S2}, and v_{D2}) at (D = 0.45, V_{in} = 360 V, V_o = 45 V, and P_o=1.3 *kW*). The gate driving signals are shown in Figure 9(a). Owing to the self-balancing capability of the FDSC configuration, the phase currents remain balanced even without the use of sensors or feedback control. As illustrated in Figure 9(b), the four inductor currents are well balanced, with a ripple of approximately 25% (about 2 *A*). Furthermore, the interleaving effect of the four phases significantly reduces the output current ripple to about 0.5 *A*. This low ripple allows optimization of the phase inductor values and the output capacitor reactance during the design stage, thereby enhancing the dynamic response of the converter. Figure 9(c) also shows the voltage stresses of switches S_1 and S_2 are 100 V and 200 V, respectively. The voltage stresses of diodes D_1 and D_2, are 100 V. The same also applies to switches S_3, S_4 and diodes D_3, D_4, since the FDSC structure consists of symmetrical P-cell and N-cell configurations. Compared with the conventional 4P-IBC, in which the switching devices experience the full input voltage ($V_{in} \approx$ 360 V), the proposed converter significantly reduces the voltage stress on the switches. This reduction directly contributes to improved conversion efficiency.

An additional experiment was conducted to examine the effect of inductance mismatch, as shown in Figure 10. In this case, the inductor L_1 was deliberately reduced to 200 μH, compared to 250 μH for the remaining inductors. It can be seen that although the ripple of i_{L1} is larger than that of the other inductors, the average current values across all four inductors remain equal. This demonstrates that the current-balancing capability of the FDSC configuration is independent of the inductor values.

Another similar experiment was conducted, Figure 11, illustrating the waveforms of four currents in the FDSC circuit under conditions where the gate driving signal are intentionally mismatched. The gate signal for S_1 was deliberately altered (D_{S1} = 0.42 and D_{S2} = D_{S3} = D_{S4} = 0.45), the four inductor currents are still balanced. To clarifying a point of here that the inductor current balancing function does not mean all the inductor currents must be perfect equal, so it can be observed that the average values of the currents i_{L1} – i_{L4} show some deviation i_{L1} reaches 7.5 *A* while i_{L2}, i_{L3}, and i_{L4} are at 7 *A*. As long as the inductor currents are not "losing control" which could lead to degraded performance or potential damage to circuit components, a little mismatch in the inductor currents is still acceptable. It should also be noted that in practical applications, a duty cycle deviation of 0.03 is relatively significant.

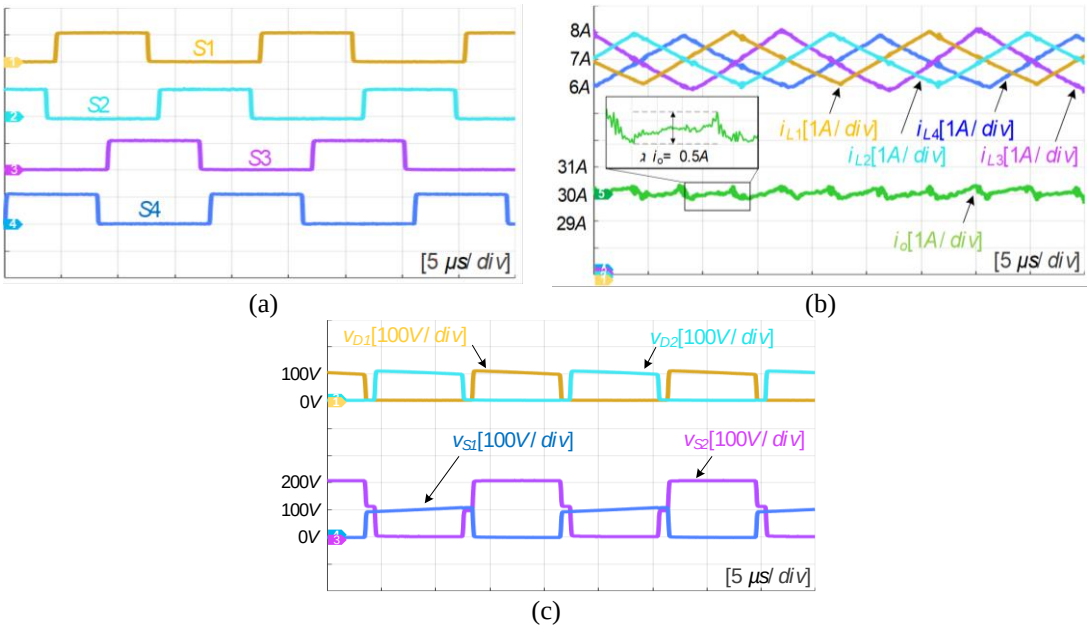

Figure 9. Experimental waveforms when D = 0.45, V_{in} = 360 V, V_o = 45 V, P_o = 1300 W: (a) gate signals, (b) inductor current and output current, and (c) diode voltage and switch voltage

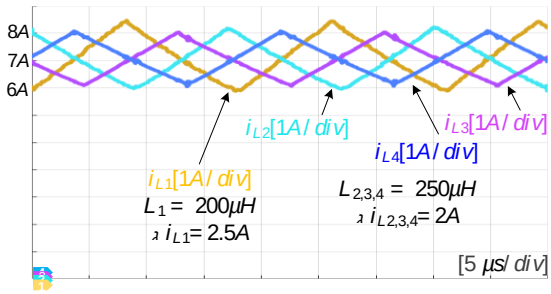

Figure 10. Experimental waveforms of the FDSC converter when have a mismatch of the inductance value (L_1 = 200 μH, L_2 = L_3 = L_4 = 250 μH)

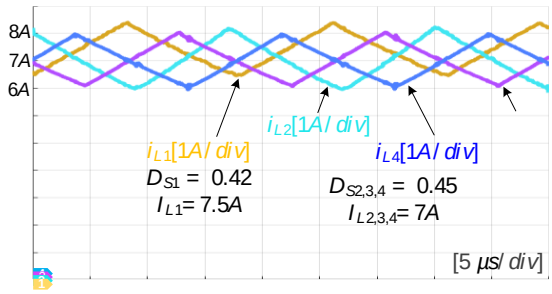

Figure 11. Experimental waveforms of the FDSC converter with a mismatch of the gate signal (D_{S1} = 0.42 and D_{S2} = D_{S3} = D_{S4} = 0.45)

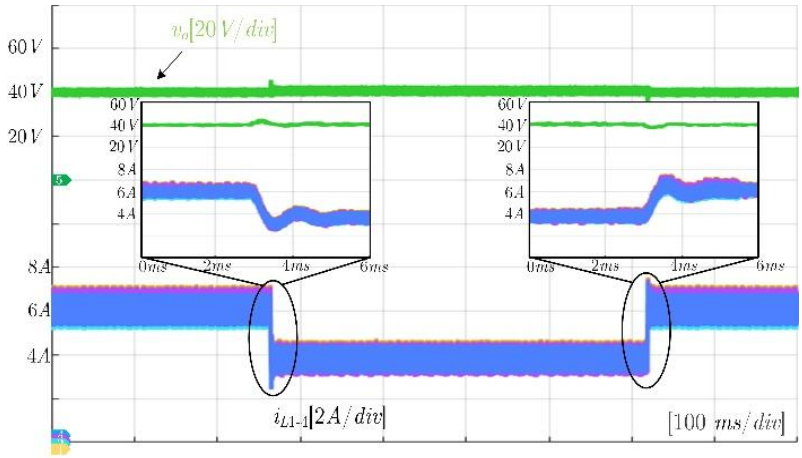

Figure 12. Dynamic response of the FDSC converter under step load

The dynamic response of the FDSC converter under step load conditions is presented in Figure 12. In this test, the load is varied between 70% (900 W) and 40% (500 W). Despite the absence of current feedback, the inductor currents i_{L1}–i_{L4} remain well balanced, with only a minor overshoot. The output voltage exhibits slight fluctuations, but without significant deviation. Notably, the converter requires only 1 ms to fully settle and restore steady operation.

Figure 13 presents the efficiency of the FDSC converter, validated through both simulation and experimental results. The proposed topology demonstrates excellent performance, achieving an efficiency greater than 97% at full load. As the simulation does not account for inductor losses and circuit conduction losses, its reported efficiency is slightly higher than that observed experimentally. Figure 14 further illustrates the loss distribution, indicating that the majority approximately 72% originates from the conduction losses of diodes D_1–D_4. This observation suggests that the efficiency could be further enhanced by replacing the diodes with active switches, similar to those employed in a synchronous buck converter.

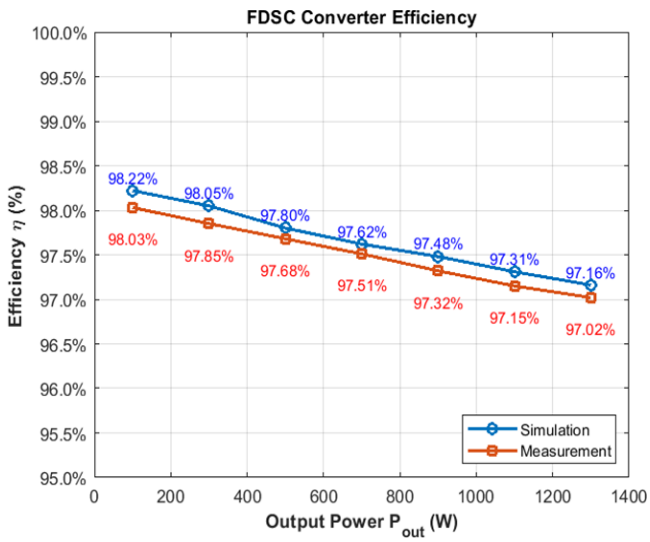

Figure 13. The efficiency of the proposed FDSC converter

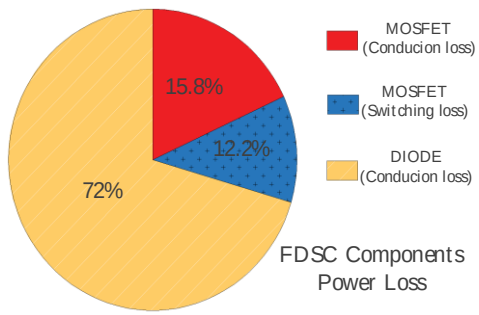

Figure 14. Power loss distribution of semiconductor devices in the FDSC converter

5. CONCLUSION

This paper proposed an FDSC converter for high conversion ratio DC–DC applications. Compared with the conventional 4P-IBC, the proposed converter achieves natural current balancing without additional sensing or control circuits, provides a higher voltage gain, and reduces voltage stress on semiconductor devices. These advantages make it suitable for applications such as EV auxiliary power supply and voltage regulator modules, where wide voltage ranges and high current capability are required. A detailed analysis was carried out and the experimental prototype at 1.3 *kW* validated the theoretical findings. Although the duty-cycle limitation still constrains the operating range, future work will focus on PWM scheme and design improvements to address this issue. In conclusion, the proposed FDSC converter demonstrates high efficiency, intrinsic current sharing, and practical feasibility, highlighting its potential for next-generation low-voltage, high-current power converter.

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AUTHOR CONTRIBUTIONS

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Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
Chan Viet Nguyen	✓	✓	✓	✓	✓	✓		✓	✓			✓	✓	
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C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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