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Comparison of phase disposition, phase opposition, and phase disposition with variable frequency PWM techniques for harmonic reduction in cascaded multilevel inverters

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ABSTRACT

Renewable energy penetration in distributed generation systems significantly impacts the power quality of the output. The stochastic nature of the inverters provides variable voltage and variable frequency outputs, which is an advantage when used with photovoltaic (PV) and grid integration to the distribution grid, and also in induction motor drives. A primary source of power quality issues is the harmonics generated by the inverters. Multilevel inverters are commonly employed to mitigate these harmonics and improve power quality. Among the various multilevel inverter topologies, the cascaded multilevel inverter (CMLI) has gained prominence due to its simple structure, ease of control, and reduced component requirements. This paper presents a comprehensive review of multilevel inverter topologies that have influenced the evolution of the CMLI structure, along with an investigation into the application of advanced pulse width modulation (PWM) strategies for performance enhancement. In particular, phase disposition (PD), phase opposition disposition (POD), and phase disposition with variable frequency (PD-VF) PWM techniques are implemented on cascaded h-bridge (CHB) multilevel inverters configured for five-level, seven-level, and nine-level operations. A comparative evaluation of total harmonic distortion (THD) is conducted for each inverter configuration, both with and without the inclusion of an LC output filter, to assess waveform quality and harmonic mitigation capability. Furthermore, the harmonic suppression effectiveness of PD, POD, and PD-VF modulation methods is systematically analyzed across different voltage levels. The study also demonstrates that varying the carrier frequency in PD-VF modulation significantly influences THD performance, offering enhanced flexibility and expanded control possibilities in multilevel inverter applications.

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1. INTRODUCTION

Power systems have adopted multilevel inverters to reduce the harmonics, usually in the renewable energy integration in the grid. Different topologies of multilevel inverters and different pulse width modulation techniques are developed in search of better performance in harmonic reduction. Cascaded Inverter is one of the most widely accepted multilevel inverter topologies with the advantage of reduced

components and simple design as compared to previous multilevel inverter topologies like diode clamped and flying capacitor multilevel inverters. The topological variation is researched simultaneously along with the pulse width modulation (PWM) methods. Phase disposition (PD) PWM method is applied on the neutral point clamped multilevel inverter to analyze the harmonics by measuring the total harmonic distortion (THD) [1]. The weighted THD of the high-frequency component of the inverter output is used for analyzing the performance of the inverter. A reduced switch topology of the cascaded multilevel inverter is used, and phase disposition pulse width modulation (PDPWM) is applied to analyze the effect of this PWM technique on the eleven-level cascaded multilevel inverter (MLI) [2]. The analysis is carried out for different switching frequencies. Two different operating frequencies are used to generate the carrier wave for the PDPWM implementation [3]. Unsymmetrical multilevel inverters, which involve two different levels of inverters, like three-level and 9-level combined, and also unequal direct current (DC) link voltages, are used for a better performance in harmonic reduction [4]. A five-level neutral point connected inverter is used for an induction motor drive to meet the IEEE 519 standards. Very low switching frequency-based MLI is used to get good stability in a dynamic environment in the variable speed drive [5]. An AC-DC converter connected to the multiwinding transformer connected to the multilevel inverter induction motor drive uses an 18-pulse AC-DC conversion stage [6]. To improve the dynamic response of the IMD 9-level cascaded multilevel inverter (CMLI) is used at the ternary winding. The reduction of the 5^{th} ,7^{th}, and 9^{th} harmonics are analyzed. In order to maintain the quality of the motor current all the time of operation, the choice of harmonic current generated by the inverter is controlled by modifying the operating frequency [7] using the hybrid inverter topology that combines the low voltage high frequency H-bridge cells to the high voltage quasi square wave inverter. To maintain the power quality in the medium voltage induction motor drive systems from both the drive side and the grid side a multiple pulse ac-dc converter and multilevel inverter with the H-bridge topology is simulated to eliminate the harmonics from the multiwinding transformer [8]. A similar topology with unequal voltages with the proportional ratio of 1:2:3 is developed to obtain a better THD, and power quality is discussed [9].

A novel level-shifted carrier-based PWM technique named third harmonic injected inverted sinusoidal carrier (PWM THI2SCPWM) is introduced in the induction motor drive, which mitigates the torque ripple [10]. Nine different output voltages are obtained from the photovoltaic (PV) panels and supplied to the three-phase multilevel inverter with a supercapacitor unit. Supercapacitors work for voltage balancing in the neutral point clamped inverter topology since no need for extra control is required, and no need for any circuit topological variation is needed [11]. Increase in junction temperature due to high frequency switching in the PV-fed grid with cascaded MLI is controlled using the switching scheme which employs a modified discontinuous standard mode signal [12]. Neutral point clamped topologies are adopted for their advantage of higher power density. A modified carrier discontinuous PWM (DPWM) method is used on the NPC T-type inverter to improve the THD and to manage capacitor voltages [13]. Different PWM techniques and topologies are discussed with improvements in performance in THD and power quality in the literature [14]–[25]. A novel advanced level shifted carrier-based bus clamping PWM is proposed that provides better THD reduction in the induction motor drive (IMD) [14]. As an improvement to the phase-shifted pulse width modulation techniques, the jittered carrier phase shifted sine pulse width modulation (JCPS-SPWM) method is introduced, which moves the lower-order harmonics to higher-order harmonics for both the voltage and current to obtain fewer harmonics [15]. Among the multilevel inverters, single-stage multiport inverters are a cost-effective variation that facilitates the connection of energy storage devices directly to an AC microgrid without intermediate converters. For a time-varying DC input, a novel asymmetric level-shifted pulse-width modulation technique is used, which facilitates better current control [16]. The input current harmonics from any three-phase power supply are controlled using the multi-pulse AC-DC converters in the rectifier stage of the IMD. An increase in the number of pulse numbers has decreased the input current harmonics fed to the inverter, thus safeguarding the input supply from harmonics [17]. A 27-level induction motor drive is fed using an 18-pulse rectifier to facilitate the inverter to be controlled using a lower switching frequency [18]. Similarly, a 36-pulse rectifier is used for a T-type inverter fed to the induction motor drive [19]. Advanced SVPWM methods are discussed in [20] and [21]. A survey of different PWM techniques on the neutral point clamped multilevel inverter (NPCMI) is carried out in [22]. A novel PWM technique called the rotating trapezoidal SPWM technique is introduced in the article [23], which showed THD improvement compared to other similar methods. Specific harmonic elimination using metaheuristic methods is used in [24] and [25].

This paper compares different PWM techniques like phase disposition, phase opposition, and phase disposition with different frequencies on 5, 7, and 9 level inverters. MATLAB-based simulation is developed on all three levels, and the harmonics reduction of all the levels is compared for all three PWM techniques. The THD obtained from all these different PWM techniques is tabulated, and the progressive performance of each method is discussed in the paper. Section 2 of the paper discusses the methodology of the three PWM

techniques, section 3 details the results and discussion on the results thus obtained from the MATLAB simulation, 0 followed by a conclusion and references.

2. CARRIER-BASED PWM TECHNIQUES IN CASCADED MULTILEVEL INVERTER

Sinusoidal pulse width modulation (SPWM) remains one of the most extensively utilized modulation techniques in multilevel inverter systems due to its simplicity and effective harmonic performance. This section evaluates three SPWM-based approaches: PD, phase opposition disposition (POD), and phase disposition with variable carrier frequency. Each technique is founded on the comparison between a high-frequency triangular carrier waveform and a sinusoidal reference signal, where the interaction between these signals determines the inverter switching pattern and overall output quality.

The interaction between the carrier and reference waveforms determines the switching pattern and, consequently, the output voltage waveform. In the phase disposition technique, multiple carrier signals are arranged in amplitude-stacked levels and are compared with the sinusoidal reference across different phase angles to generate the required PWM pulses. In the phase opposition method, the same procedure as the phase disposition is applied with the triangular wave, which is in phase opposition. The triangular waves with different frequencies are generated to be compared with the sinusoidal wave and the stepped amplitude variation, as the phase disposition method is applied to obtain the phase disposition with variable frequency (PD-VF) implementation. Five, seven, and nine-level inverters are used for cascaded MLI topology to get the THD comparison for different PWM techniques with different levels of the inverter. The topology of the cascaded multilevel inverter is depicted in Figure 1 as a nine-level inverter. It can be seen that in this three-phase inverter, each phase has 4 cells supplied with the DC supply. The individual cells that are connected in series to get the multilevel output are depicted in Figure 2. The controller for each phase of the inverter is developed using the above-said PWM generation.

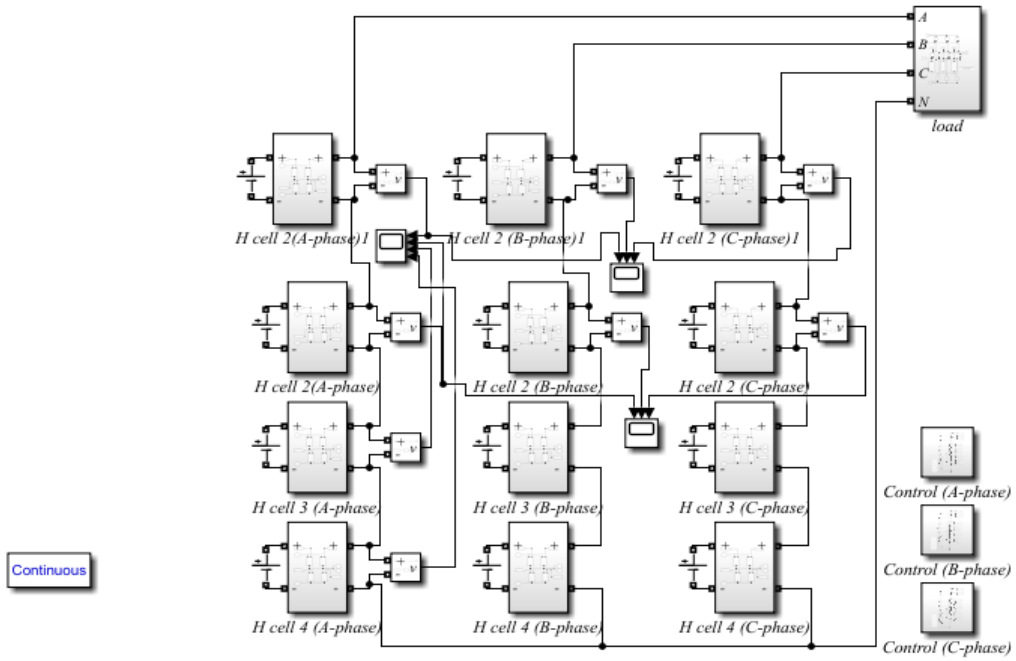

Figure 1. Nine-level inverter topologies

Inverters with different levels are compared to get a harmonics reduction comparison among the different topologies. A comparative analysis of THD is performed for the system with and without an LC filter to evaluate the effectiveness of passive filtering in multilevel inverter topologies. This comparison highlights the role of the LC filter in attenuating switching harmonics and improving the quality of the inverter output waveform. There is a common formula for the output voltage of the multilevel inverter for all three types of PWM techniques. If we consider N as the number of levels, the number of carrier waves generated is N-1. The carrier wave is denoted by $V_{c,i}$ where 'i' denotes the number between 1 to N-1 in the number of carrier waves. The modulating wave which is the reference sinusoidal wave, is compared with these triangular waves generated as the phase variation of the sinusoidal wave. The modulating wave is

defined as V_m and V_s is the DC source supplied to the multilevel inverter. The equation defining the multilevel inverter output voltage for the carrier wave modulation implementation is defined in (1).

$$V_{out}(t) = \sum_{i=1}^{N-1} \left[sgn\left(V_m(t) - V_{c,i}(t)\right) + 1 \right] . \frac{V_s}{2(N-1)} \quad (1)$$

The function sgn(x) denotes the signum function, which characterizes the polarity of the variable x. It returns a value of +1 when x is positive (x > 0), –1 when x is negative (x < 0), and 0 when x equals zero. The specification of the different levels of inverter and corresponding passive filter data is detailed in Table 1.

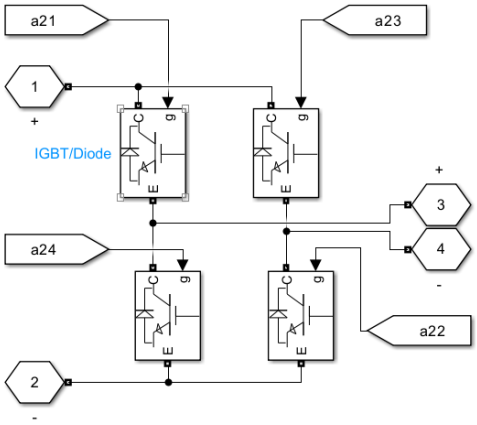

Figure 2. H-bridge topology in a cell

Table 1. Configuration details of 5-level, 7-level, and 9-level multilevel inverters

Inverter level	Specification	Value
Five-level	Switches per phase	8
	DC source voltage per bridge	100 V
	Load parameters	R = 100 Ω, L = 314 µH
Seven-level	Switches per phase	12
	DC source voltage per bridge	100 V
	Load parameters	R = 100 Ω, L = 314 µH
Nine-level	Switches per phase	16
	DC source voltage per bridge	100 V
	Load parameters	R = 100 Ω, L = 314 µH

3. RESULTS AND DISCUSSION

MATLAB-based simulation of different PWM techniques and different levels of multilevel inverters. The THD of the different PWMs with different levels is measured and tabulated. The modulation and carrier wave for the 5-level inverter for all three types of PWM techniques are depicted in Figures 3–5.

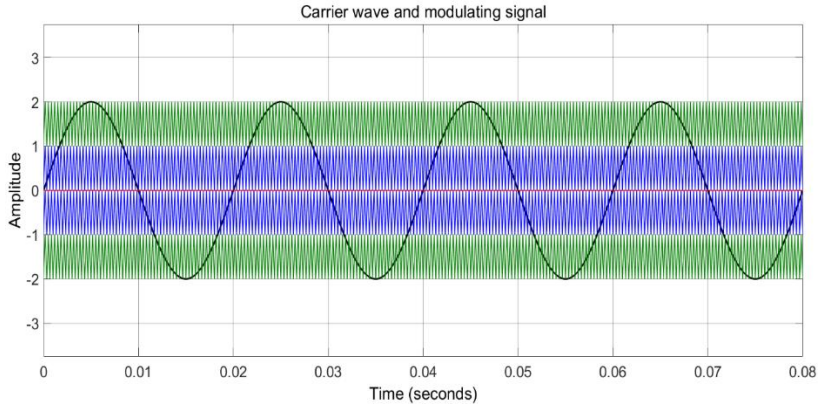

Figure 3. Modulation and carrier wave 5 level

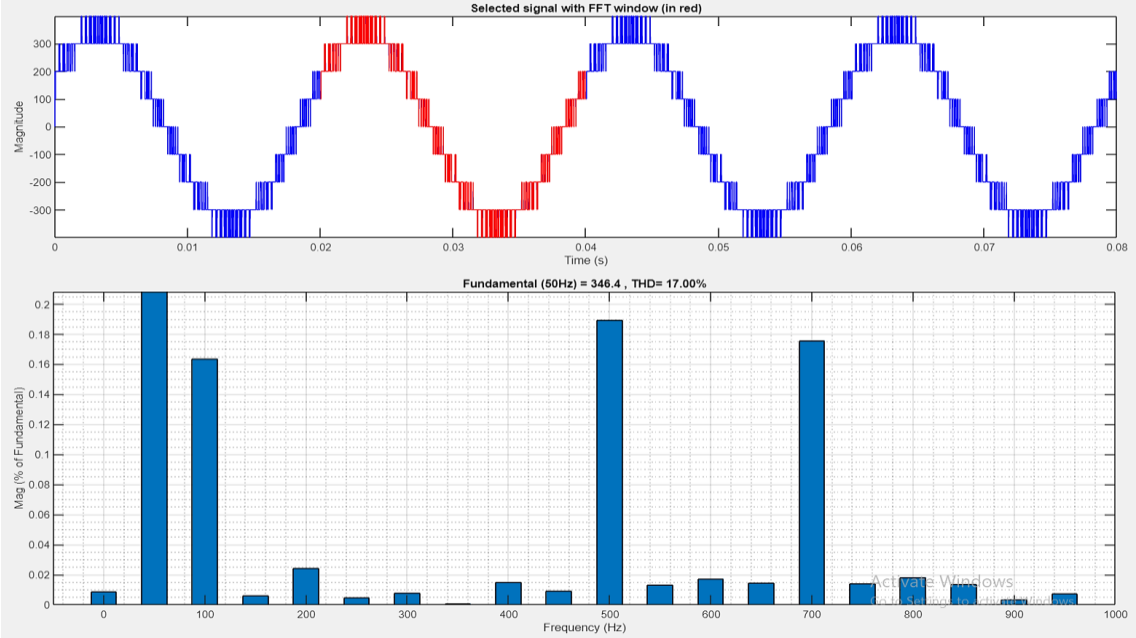

Figure 4. THD five level inverter

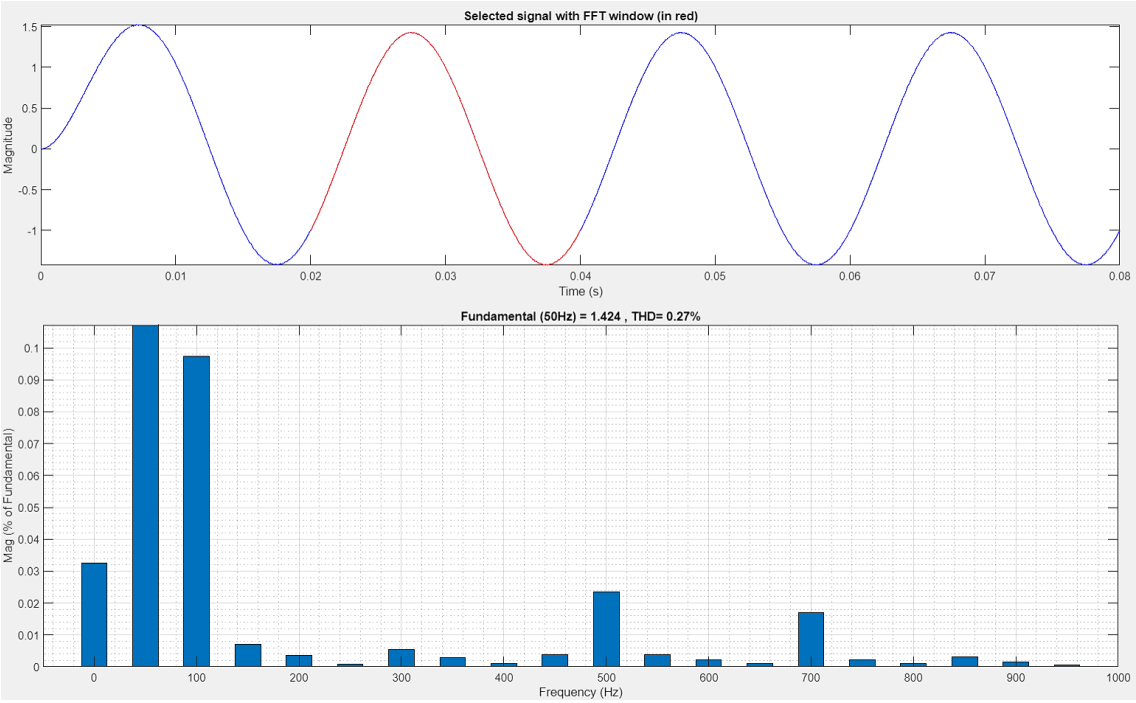

Figure 5. THD after LC filter

An LC filter is incorporated at the inverter output to attenuate high-frequency switching harmonics and smooth the output waveform toward a near-sinusoidal profile. The inclusion of the filter significantly reduces the THD compared to the unfiltered inverter output. The THD measured after the LC filtering stage is presented in Figure 5. Although the multilevel inverters are important in reducing the THD it cannot act alone. The passive filter, when acting alone, will not be able to fully reduce the harmonics either. The size of the passive filter is largely reduced when combined with the multilevel inverter. The use of an LC filter in the multilevel inverter output reduces the THD to a very acceptable level.

The seven-level inverter's output is as given in Figure 6 without the LC filter. An LC filter is connected at the inverter output to suppress high-frequency switching harmonics and shape the output voltage into a near-sinusoidal waveform. As a result, the THD is significantly reduced compared to the raw inverter output. The THD achieved after LC filtering in the seven-level inverter configuration is illustrated in Figure 7. Similar to the five-level output, the seven-level output is also applied with the LC filter to obtain the acceptable THD level, as shown in Figure 7.

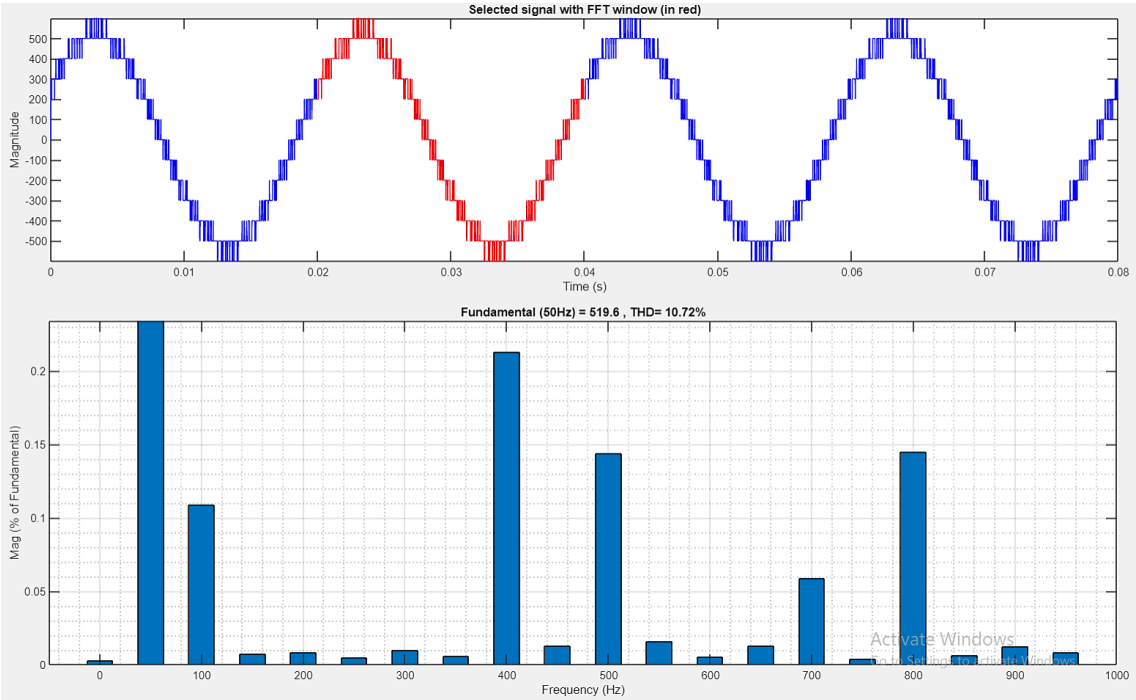

Figure 6. Seven-level THD

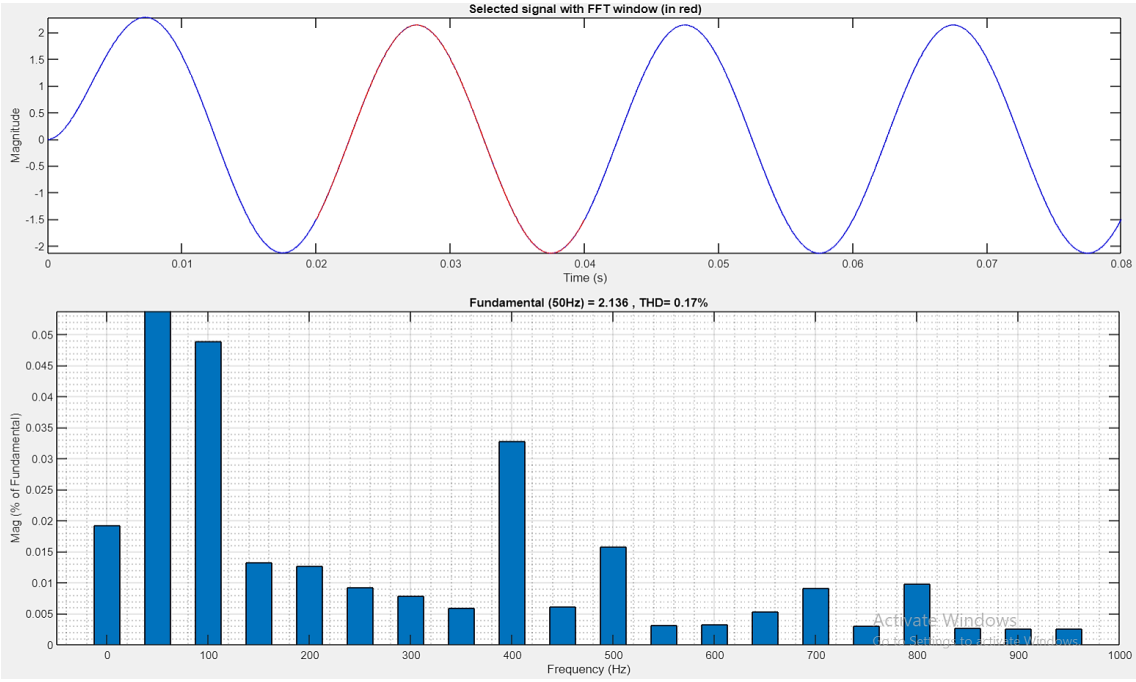

Figure 7. THD after the LC filter seven-level

To further improve the harmonic reduction, the number of levels in the multilevel inverter is increased to 9 levels and combined with the LC filter. The THD percentage is about 8.26% with a 9-level inverter and reduced to 0.15% with the LC filter, as shown in Figures 8 and 9, respectively. Although all the multilevel inverters are giving the THD within the IEEE 519 standards, the depiction of THD for each level is done to insist that there is an improvement in the THD for every increase in level.

An LC filter is implemented at the inverter output to mitigate switching harmonics and refine the voltage waveform toward a sinusoidal shape. This filtering stage results in a lower THD compared to the unfiltered inverter output. The THD obtained after applying the LC filter in the nine-level inverter configuration is shown in Figure 9. The phase disposition method, along with the LC filter, has performed better in reducing the harmonics with the increase in the number of levels.

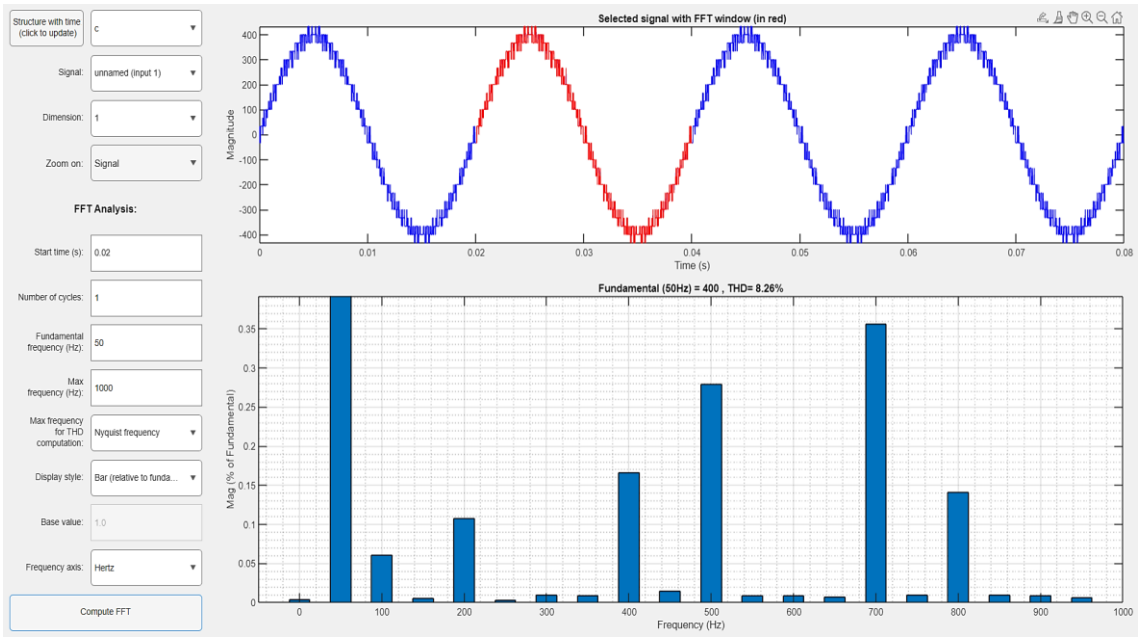

Figure 8. Nine-level THD

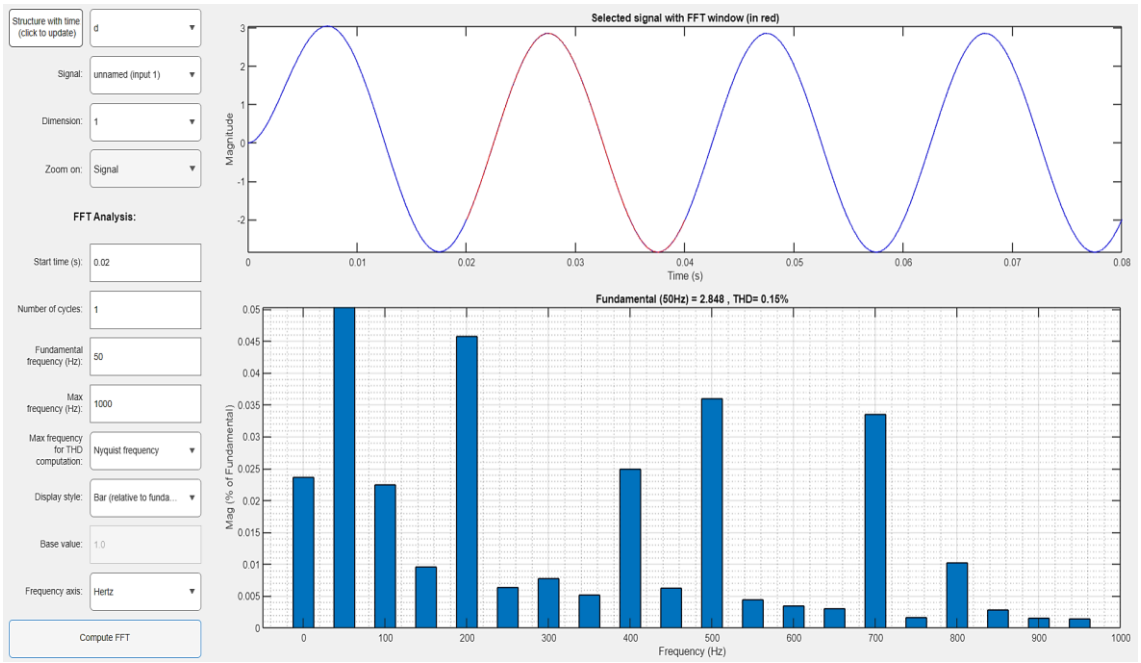

Figure 9. THD after LC filter nine-level

3.1. Phase opposition

Similar to the phase disposition method, phase opposition methods are also used extensively to reduce the harmonics in the power systems. For the comparative analysis with the phase disposition methods, the phase opposition methods are used, which use the same technique to generate the PWM as the phase disposition method, with the triangular waves in the opposite direction for comparison with the sinusoidal wave. The modulation and the carrier wave for PWM generation are as given in Figure 10.

THD of the 5-level inverter with the phase opposition PWM applied to the multilevel inverter is around 25.39%, and after the LC filter, the THD is reduced to 0.99%, as shown in Figures 11 and 12. The use of an LC filter is very effective in reducing the THD, and also, since a multilevel inverter is used, there is a reduction in the size of the passive filter. Thus, the THD when increasing the number of levels needs to be checked.

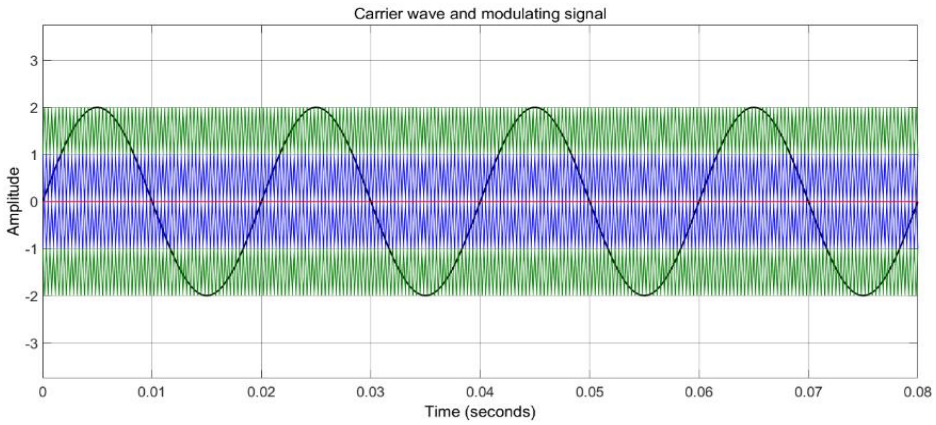

Figure 10. Modulation and carrier wave 5 level

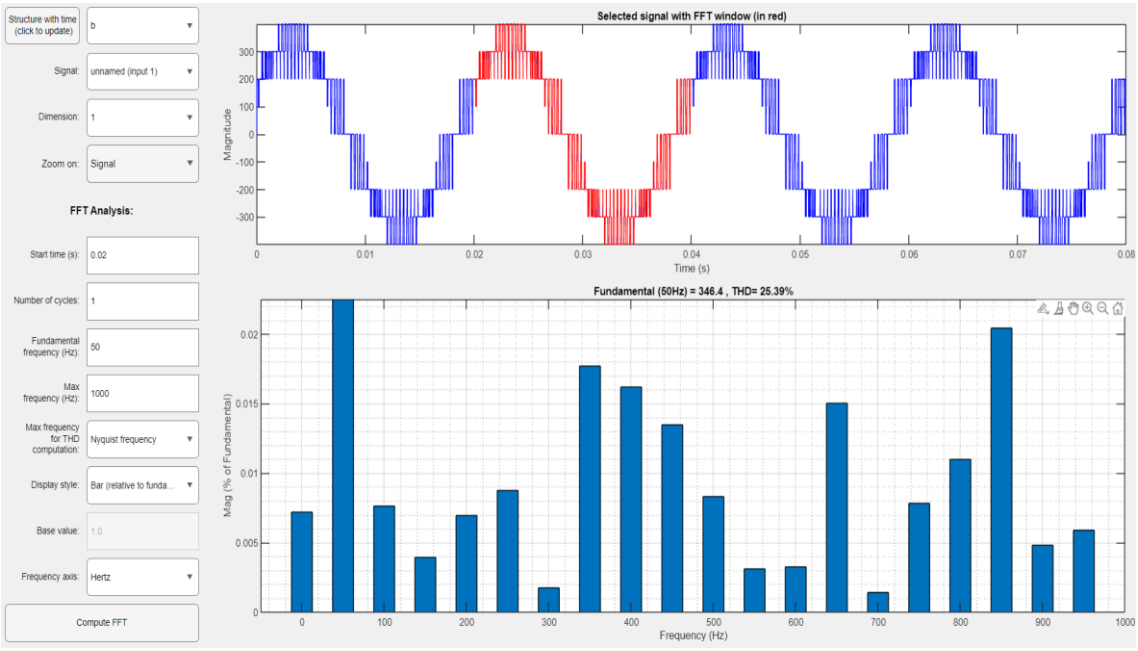

Figure 11. FFT 5 level

With the seven-level inverter in the LC filter, the THD has been brought down to 0.51%, which is nearly half of what was obtained in the 5-level inverter output. Thus, a further increase in the multilevel inverter level is checked to observe the THD obtained after the LC filter is applied at the multilevel inverter output. Figure 13 shows the harmonic level for the 7-level inverter without an LC filter, while Figure 14 shows the harmonic level for the 7-level inverter with an LC filter.

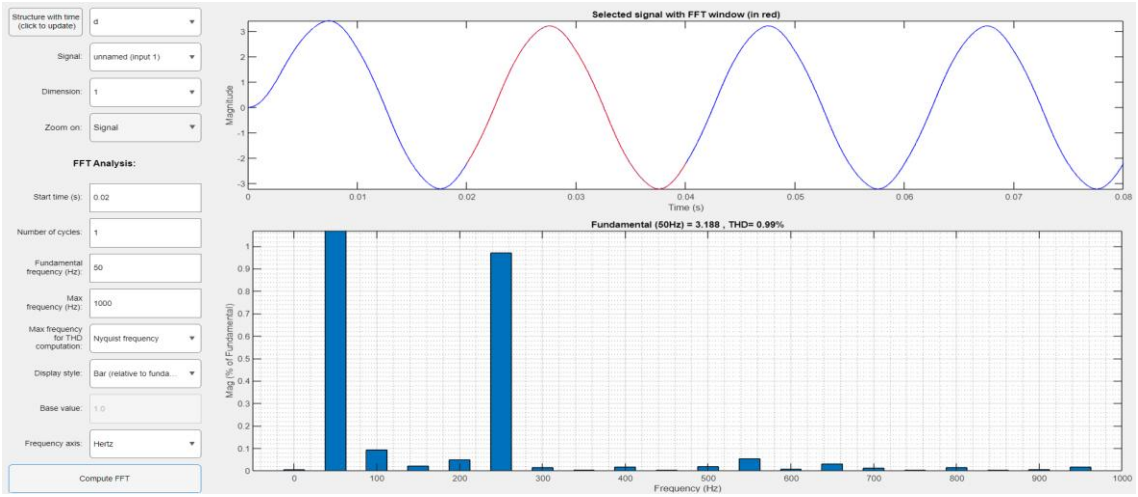

Figure 12. FFT 5 level with LC

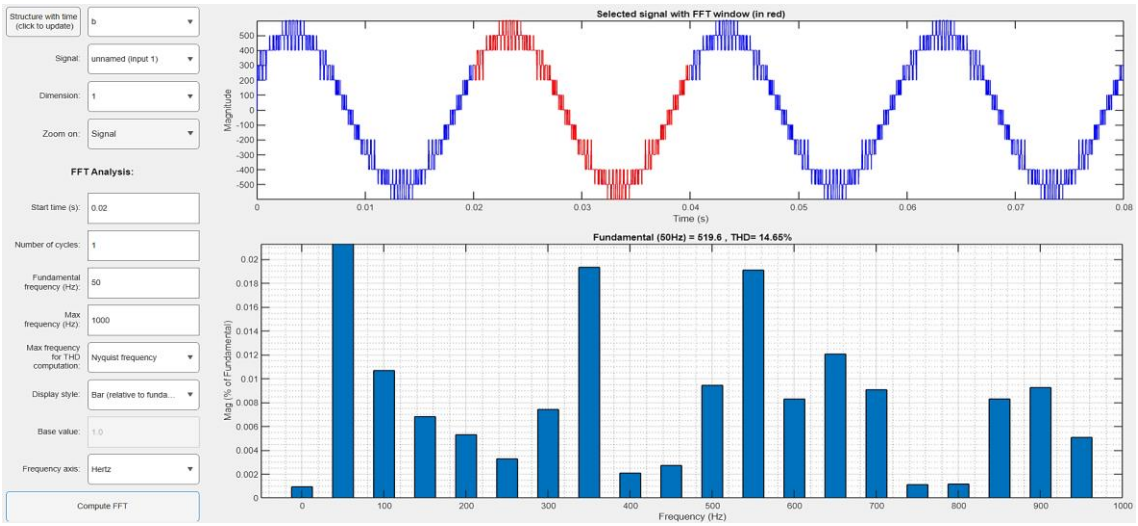

Figure 13. FFT 7 level

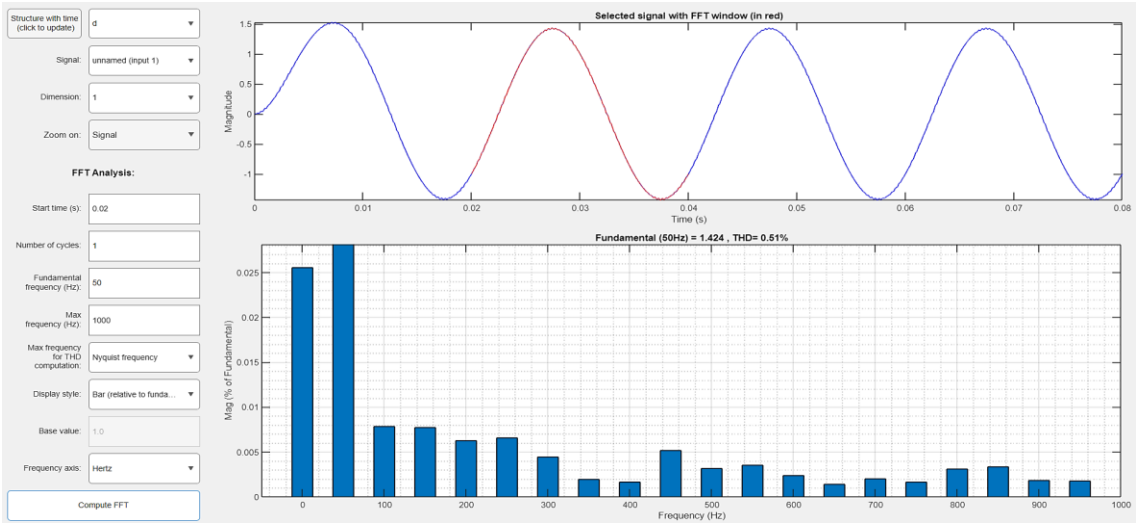

Figure 14. FFT 7 level with LC

With the nine-level inverter in the LC filter, the output has brought down the THD to 0.29%, which is nearly half of what was obtained in the 7-level inverter output. In both phase disposition and phase opposition methods, it is found that the nine-level inverter has performed better than its 5 and 7-level inverter topologies. The THD without the LC filter for a 9-level inverter is shown in Figure 15, and with the LC filter is given in Figure 16.

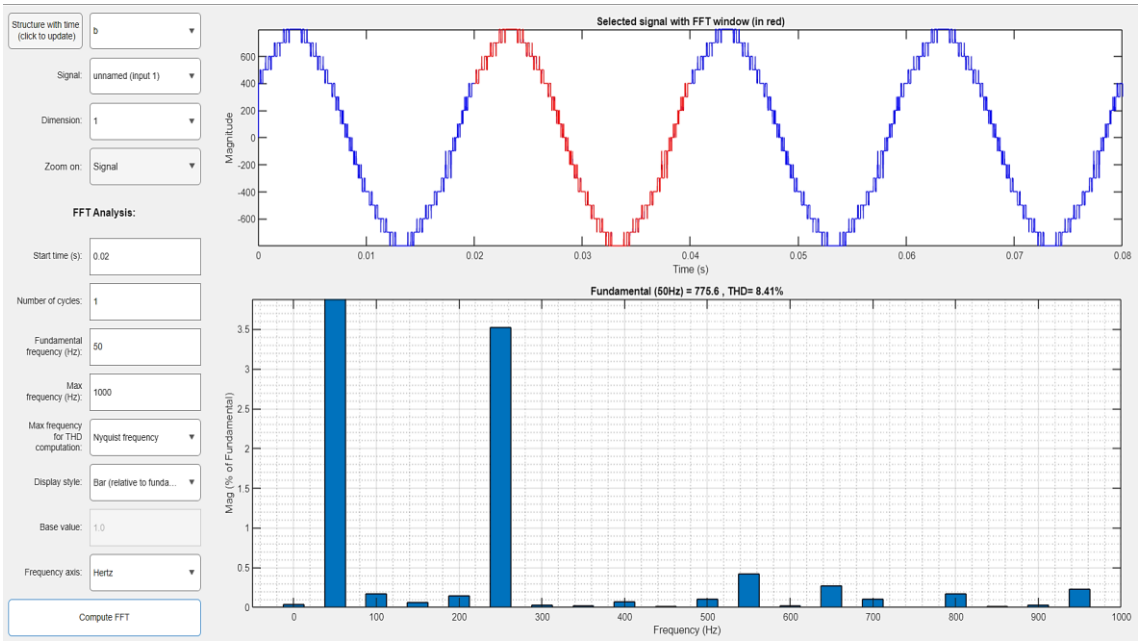

Figure 15. FFT 9 level

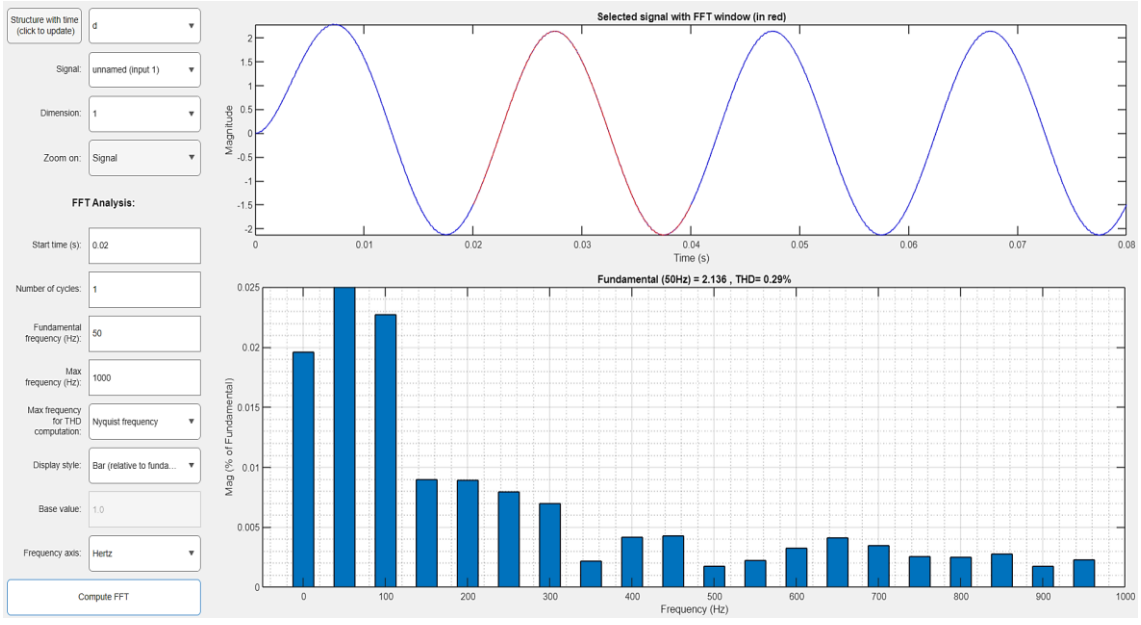

Figure 16. FFT 9 level with LC

3.2. Phase disposition with variable frequency

This method uses the same phase disposition method of generating the PWM, except that it introduces different frequencies of triangular waves to be compared with the sinusoidal wave. The comparison of 5, 7, and 9-level multilevel inverters is done in this section and compared with the other two

PWM techniques. THD improvement while using each PWM technique and each level in the multilevel inverter is compared. THD for the 5-level inverter with phase disposition with the variable frequency method is as given in Figure 17. After the LC filter is applied, the result is as given in Figure 18 with THD as low as 0.75%.

With the seven-level inverter in the LC filter, the output has been brought down to 0.32%, which is less than half of what was obtained in the 5-level inverter output as shown in Figure 19. Thus, a further increase in the multilevel inverter level is checked to observe the THD obtained after the LC filter is applied at the multilevel inverter output. The seven-level inverter output THD is given in Figure 20, which is without an LC filter.

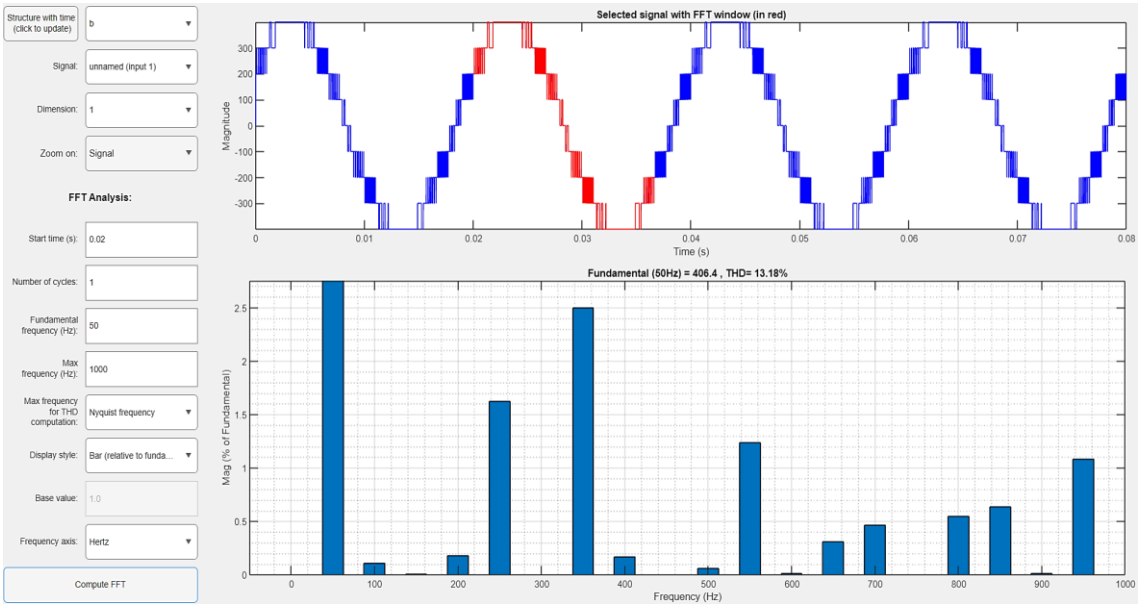

Figure 17. FFT 5 level

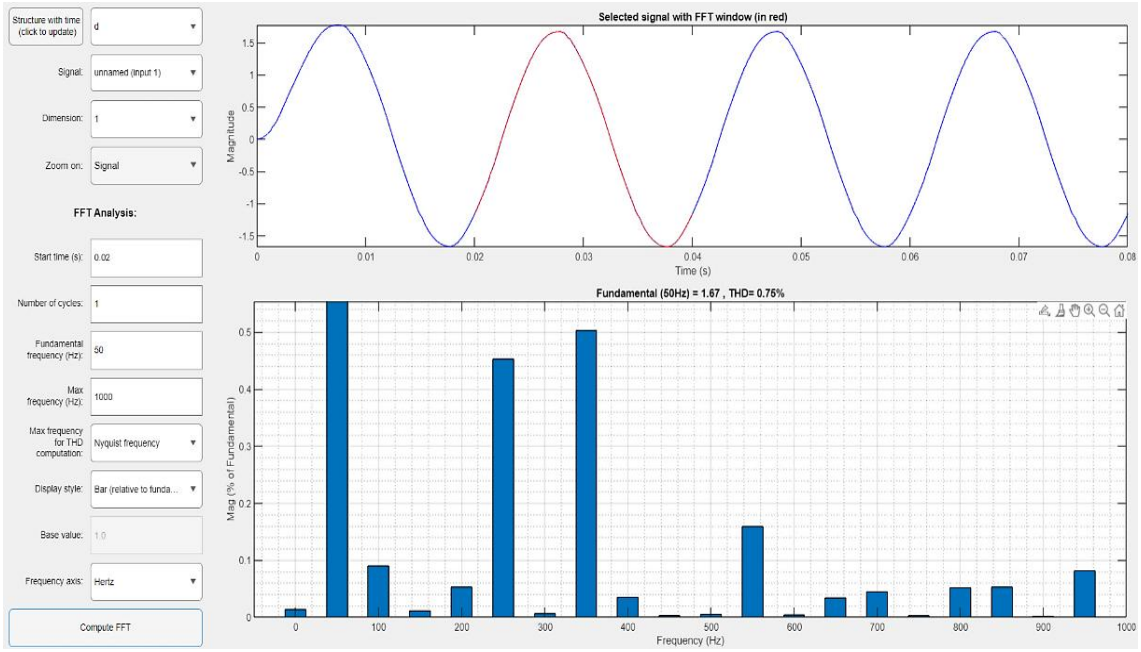

Figure 18. FFT 5 level with LC filter

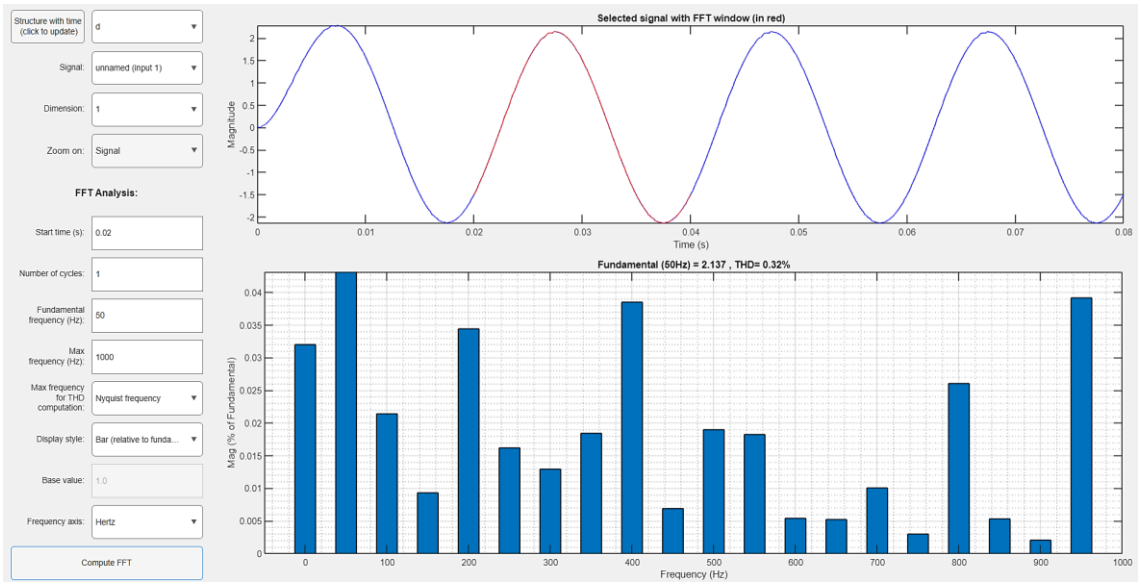

Figure 19. FFT 7 level with LC filter

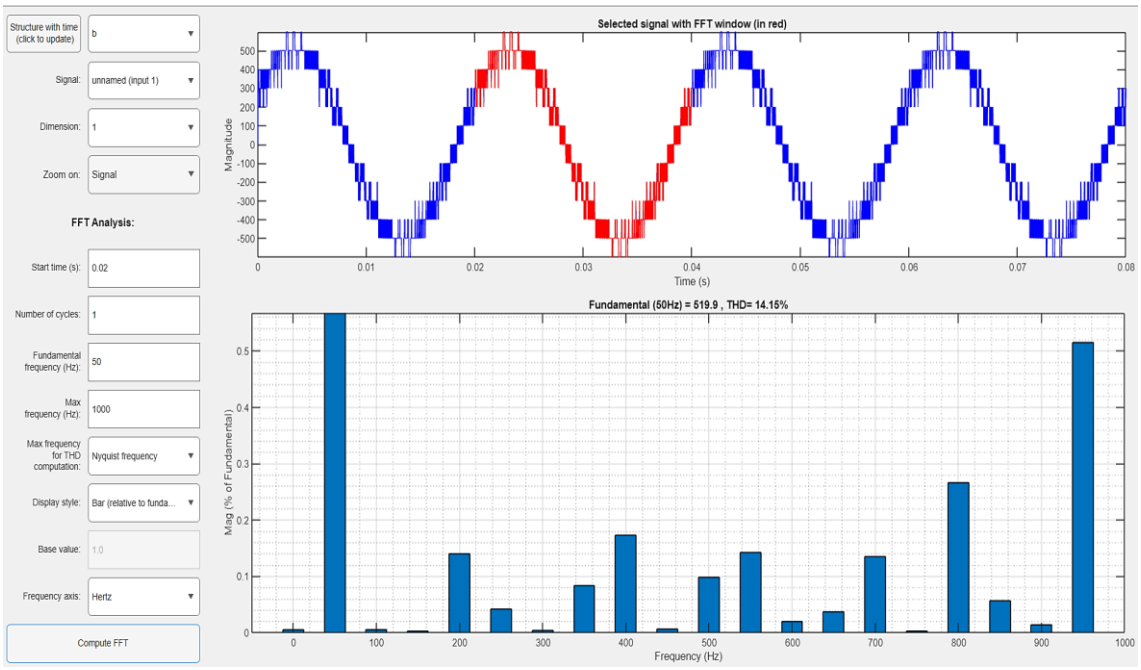

Figure 20. FFT 7 level

With the nine-level inverter in the LC filter, the THD has been brought down the THD to 0.25%, which is less than what was obtained in the 7-level inverter output. In both phase disposition and phase opposition methods, it is found that the nine-level inverter has performed better than its 5 and 7-level inverter topologies. The THD without the LC filter for a 9-level inverter is shown in Figure 21, and with the LC filter is given in Figure 22.

The comparative analysis is concluded in Table 2, which tabulates the THD obtained by all three types of PWM methods and also for different multilevel inverter levels. The table is tabulated for the THD obtained at the inverter output with the LC filter. It is initially observed that the THD obtained always complied with the IEEE 519 standards.

It is observed that there is a progressive improvement in the percentage of THD for an increase in all the different PWM techniques. The THD obtained in the phase disposition method-based multilevel inverter is found to be lower, which makes it advantageous among all three PWM techniques. Phase disposition with

a variable frequency carrier wave is found to be falling second in performance, followed by the phase opposition method.

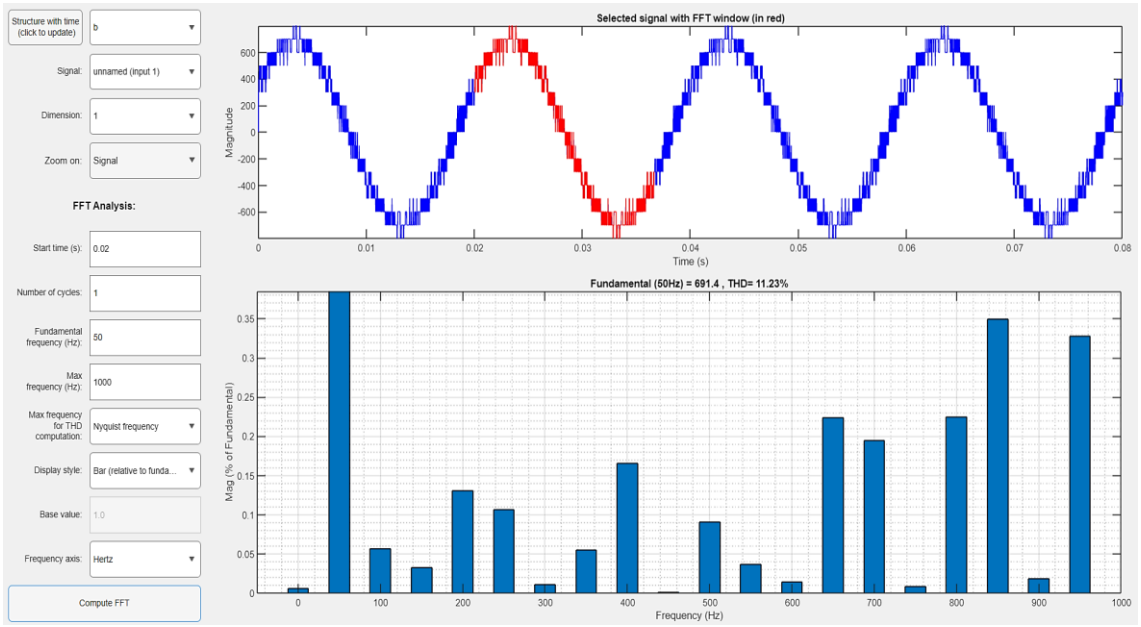

Figure 21. FFT 9 level

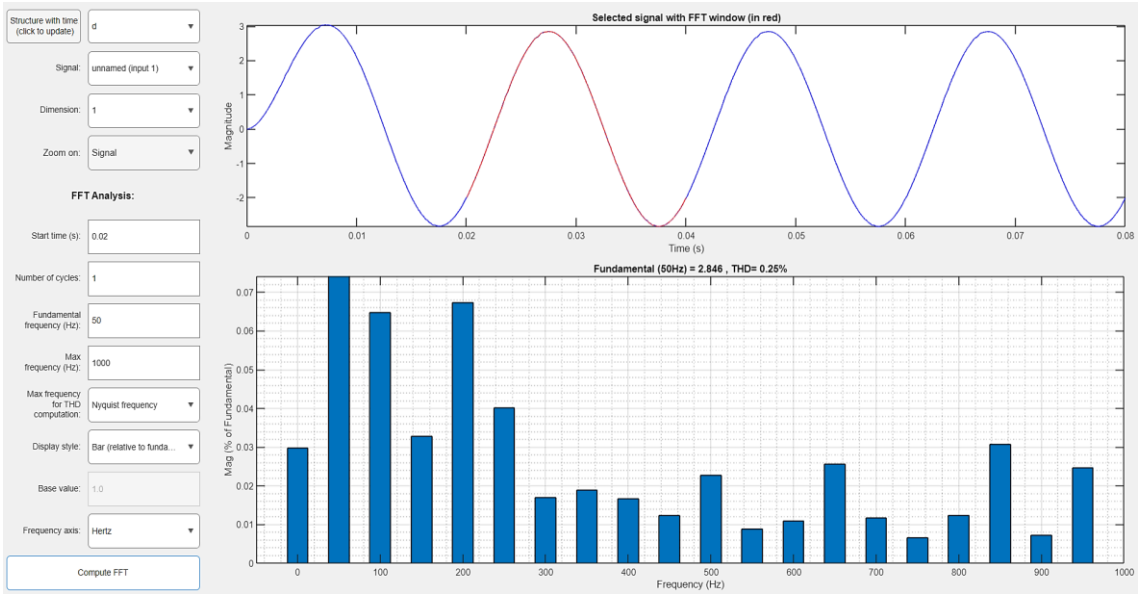

Figure 22. FFT 9 level with LC filter

Table 2. THD for PWM methods

PWM method	Level	THD	PWM method	Level	THD
Phase disposition method	5	0.27%	Phase disposition with variable frequency	5	0.75%
	7	0.17%		7	0.32%
	9	0.15%		9	0.25%
Phase opposition method	5	0.99%			
	7	0.51%			
	9	0.29%			

4. CONCLUSION

The integration of renewable energy sources into distributed generation systems presents challenges in maintaining high power quality, primarily due to harmonic distortions introduced by inverters. Multilevel inverters, especially the CMLI, offer a promising solution by reducing harmonic content and improving overall power quality. Among the various PWM techniques applied to the CMLI, PD, PO, and PD-VF have been explored for their effectiveness in minimizing THD across different inverter configurations (5, 7, and 9-level). The results indicate that these PWM methods can significantly reduce harmonics, with the addition of LC filters further enhancing the performance. This study emphasizes the critical role of selecting an appropriate inverter topology and modulation strategy to enhance power quality in distributed renewable energy systems. The findings contribute to the advancement of efficient, reliable, and high-performance power conversion solutions for modern renewable energy integration.

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AUTHOR CONTRIBUTIONS STATEMENT

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Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
G. Nayana	✓	✓	✓		✓	✓	✓	✓	✓		✓			
Savita D. Torvi	✓			✓					✓	✓		✓		

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

Data availability is not applicable to this paper as no new data were created or analyzed in this study.

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