International Journal of Power Electronics and Drive System (IJPEDS)
Vol. 17, No. 2, June 2026, pp. 1211∼1220
ISSN: 2088-8694, DOI: 10.11591/ijpeds.v17.i2.pp1211-1220

Dual-mode model predictive control for non-minimum phase boost converters

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Article Info

Article history:

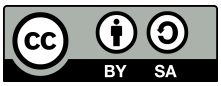
Received Jul 15, 2025
Revised Apr 4, 2026
Accepted Apr 23, 2026

Keywords:

Dual mode MPC
FS-MPC
HIL
Non-minimum phase
Real-time control
Split cost function

ABSTRACT

This paper aims to develop an efficient finite-set model predictive control (FS-MPC) strategy for DC–DC boost converters to improve voltage regulation while reducing computational complexity. The proposed approach introduces a split cost function that decouples voltage and current regulation, providing a simpler alternative to conventional long-horizon FS-MPC schemes used to address the converter's non-minimum-phase (NMP) behavior. A current-estimation technique is incorporated to eliminate the need for additional sensors, lowering hardware cost and improving robustness. Unlike existing FS-MPC methods that rely on horizon extension or extra measurements, the proposed strategy leverages the split cost structure to achieve comparable NMP compensation with significantly lower computational effort. The controller is implemented in real time using a hardware-in-the-loop (HIL) setup on a ZedBoard platform, with accurate data acquisition provided by an external ADC. Experimental results demonstrate that the proposed approach enhances voltage-tracking performance, eliminates overshoot and undershoot, reduces settling time by over 40%, and decreases computational effort by more than 80% compared to traditional FS-MPC methods.



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1. INTRODUCTION

DC–DC boost converters play a critical role in modern energy systems such as electric vehicles [1], renewable energy interfaces [2], and distributed power supplies [3]. Their ability to step up DC voltage levels makes them indispensable in meeting load and subsystem requirements. However, the intrinsic non-minimum-phase (NMP) dynamics of boost converters [4] introduce control challenges, often leading to instability and degraded transient performance when conventional controllers are applied. Traditional proportional–integral (PI) controllers are widely used because of their simplicity but struggle with the nonlinear and NMP characteristics of boost converters [5]. Nonlinear strategies, such as sliding-mode and backstepping techniques [6], [7], improve robustness but require complex implementations and extensive parameter tuning, which limits their practicality for low-cost embedded systems. Model predictive control (MPC) has emerged as a compelling alternative for power electronic converters [8]. In particular, finite-set MPC (FS-MPC) [9],

[10] aligns well with power converter operation because of its discrete nature and moderate computational requirements [11]. Nevertheless, when single-horizon FS-MPC is directly applied to regulate the output voltage of boost converters, the NMP effect can lead to instability and poor transient response [12], [13]. Existing solutions, including long-horizon and move-blocking FS-MPC approaches [14]–[16], alleviate this problem but at the expense of increased computational burden, making them less suitable for real-time applications on low-cost hardware. These challenges highlight a significant research gap because there is still a need for an FS-MPC strategy capable of addressing the NMP behavior of boost converters without relying on horizon extension or additional sensors that increase cost and complexity [17]. The present work addresses this gap by introducing a computationally efficient FS-MPC method based on a split cost function that decouples voltage and current regulation. By leveraging a load-current estimation technique, the proposed approach eliminates the need for extra current sensors, thereby improving robustness and reducing hardware requirements. In addition, a current-limiting feature is embedded within the control algorithm to enhance protection under overcurrent conditions as explained in [18]. The proposed strategy is validated through comprehensive simulations and Hardware-in-the-Loop experiments under a variety of operating conditions, including input-voltage variations, load disturbances, and reference-tracking scenarios. Results demonstrate that the method effectively mitigates the NMP-induced instability while improving transient performance, achieving faster settling time, better voltage tracking, and significantly lower computational effort compared with conventional FS-MPC schemes.

2. METHOD

This section presents a predictive control scheme tailored for DC-DC boost converters, aimed at mitigating the adverse effects of their NMP nature. The proposed solution modifies the classical FS-MPC formulation by evaluating a split cost function based on the switching state. Moreover, a load current estimation strategy is included to eliminate the need for an output current sensor.

2.1. Modeling of the boost converter

The boost converter as shown in Figure 1(a) is represented as a switched system composed of a DC voltage source, a power switch (typically a MOSFET), a diode, an inductor L, an output capacitor C, and a resistive load. The control input $u \in \{0, 1\}$ determines the switching state: $u = 1$ corresponds to the ON state (switch closed), while $u = 0$ indicates the OFF state (switch open), as illustrated in Figures 1(a) and 1(b). The regulation of the output voltage is achieved by rapidly alternating between these two operating modes [16]. When the MOSFET is closed, this state is described by (1).

$$V_L = L\frac{di_L(t)}{dt} = V_{in} - i_L R_L \tag{1}$$

The same for state where the MOSFET is open, Figure 1(c) present the converter topology and (2) described it.

$$V_L = L\frac{di_L(t)}{dt} = V_{in} - i_L R_L - V_c \tag{2}$$

V_c is equal to V_{out}, we can some by (1) and (2) in one equation, we obtain (3).

$$V_L = L\frac{di_L(t)}{dt} = V_{in} - i_L R_L - V_c(1 - u) \tag{3}$$

To predict the future inductor current [19], the conventional Euler approximation is used (4).

$$\frac{di_L}{dt} \approx \frac{i_L(k+1) - i_L(k)}{T_s} \tag{4}$$

Rearranging this equation gives (5).

$$i_L(k+1) = \frac{di_L}{dt}T_s + i_L(k) \tag{5}$$

$i_L(k)$: The measured value of the inductor current; Ts : Sampling time of the control algorithm, wich equal half of period $Ts = \frac{T_{sw}}{2}$.

Then we can put the derivative in (3) into the prediction function (5).

$$i_L(k+1) = \frac{T_s}{L}\left[V_{in} - i_L R_L - V_{out}(1-u)\right] + i_L(k) \tag{6}$$

However, to reduce complexity and preserve computational efficiency in real-time applications, the parasitic resistance is often neglected. Under the assumption $R_L \approx 0$, the simplified discrete-time model is (7).

$$i_L(k+1) = \frac{T_s}{L}\left[V_{in} - V_{out}(1-u)\right] + i_L(k) \tag{7}$$

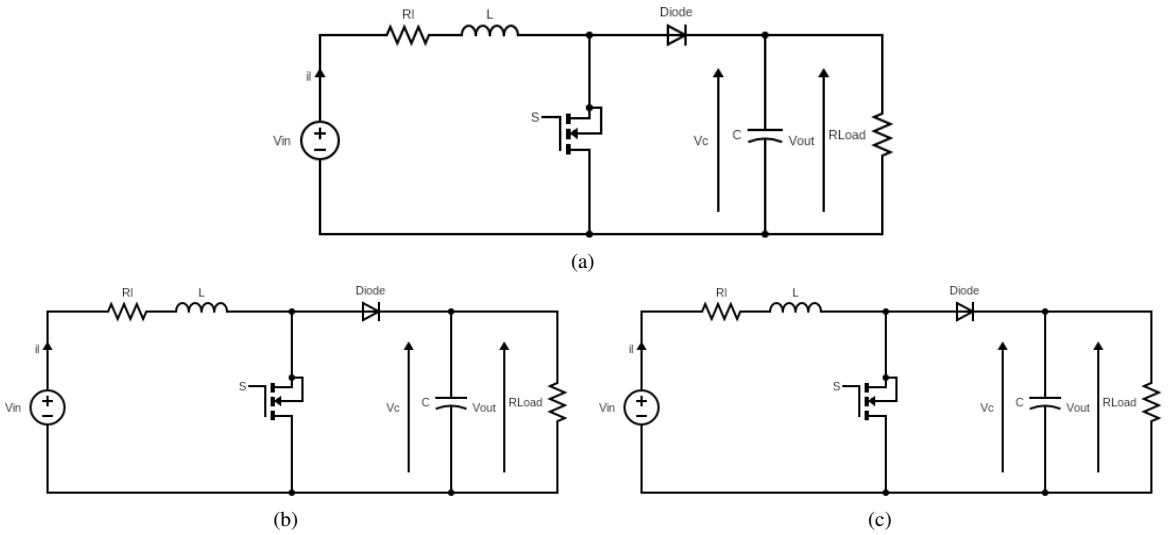


Figure 1. Circuit diagram of a DC–DC boost converter and its operating modes: (a) circuit diagram, (b) MOSFET ON, and (c) MOSFET OFF

2.2. Prediction model

The boost converter is modeled using two state variables: the inductor current i_L and the output voltage V_{out}. Conventional FS–MPC typically relies on a single step prediction, which is adequate for many power converters. However, because of the NMP behavior of boost converters where the output voltage initially moves in the opposite direction to a change in the control input single step prediction is insufficient for accurate control [20].

To overcome this limitation, the proposed strategy adopts a dual mode approach with a two step prediction horizon [21]. At each sampling instant k, the switch state $u^*(k)$ has already been applied, so the controller focuses on selecting the optimal future action $u(k+1)$ by evaluating its effect on the system at $k+2$. First, the intermediate state at $k+1$ is predicted based on the applied control $u^*(k)$, and then each candidate switching action for $u(k+1)$ is used to forecast the state at $k+2$. To further enhance the controller's ability to manage the NMP dynamics, the decision at each candidate switching action is guided by a split cost function structure that evaluates the system response differently for the switch ON and switch OFF modes, section 2.5 describe this. This combined use of a dual–mode prediction horizon and split cost function enables the controller to anticipate the inverse voltage response and select the switching sequence that ensures stable and well regulation.

The inductor current at $k+1$ is given by (8).

$$i_L(k+1) = i_L(k) + \left(\frac{V_{in}(k)}{L} - \frac{(1-u^*(k))V_{\text{out}}(k)}{L}\right) T_s \tag{8}$$

And the corresponding output voltage is predicted as (9).

$$V_{\text{out}}(k+1) = V_{\text{out}}(k) + \left(\frac{(1-u^*(k))i_L(k)}{C} - \frac{i_{\text{load}}(k)}{C}\right) T_s \tag{9}$$

Then, for each candidate switching action $u \in \{0, 1\}$, the prediction at $k + 2$ is calculated in (10) and (11).

$$i_L(k+2) = i_L(k+1) + \left(\frac{V_{in}(k)}{L} - \frac{(1-u)V_{\text{out}}(k+1)}{L} \right) T_s \tag{10}$$

$$V_{\text{out}}(k+2) = V_{\text{out}}(k+1) + \left(\frac{(1-u)i_L(k+1)}{C} - \frac{i_{\text{load}}(k)}{C} \right) T_s \tag{11}$$

The (8) and (9) provide the intermediate prediction, while in (10) and (11) estimate the future state at $k + 2$ for each control candidate. This extended prediction horizon allows the controller to anticipate the actual effect of switching actions and better handle the NMP behavior of the system.

2.3. Load current estimation

The load current is estimated without using a physical sensor, based on the capacitor current dynamics and the average inductor current. To derive this expression, we start from Kirchhoff's current law (KCL) at the output node of the boost converter. The load current is equal to the difference between the current supplied by the inductor (when the switch is OFF) and the capacitor current [22]. The capacitor current is given by (12).

$$i_C(k) = C \cdot \frac{V_{\text{out}}(k) - V_{\text{out}}(k-1)}{T_s} \tag{12}$$

When the switch is OFF, i.e., $u(k-1) = 0$, the inductor current flows to the output stage. The average inductor current over one sampling period is approximated by (13).

$$i_L^{\text{avg}}(k) = \frac{i_L(k) + i_L(k-1)}{2} \tag{13}$$

Consequently, the load current can be expressed as (14).

$$i_{\text{load}}(k) = (1 - u(k-1)) \cdot i_L^{\text{avg}}(k) - i_C(k) \tag{14}$$

Substituting by (12) and (13) into (14), we obtain the final estimation in (15).

$$i_{\text{load}}(k) = (1 - u(k-1)) \cdot \frac{i_L(k) + i_L(k-1)}{2} - C \cdot \frac{V_{\text{out}}(k) - V_{\text{out}}(k-1)}{T_s} \tag{15}$$

This approach enables the estimation of the output current using only voltage and inductor current measurements, eliminating the need for an additional current sensor.

2.4. Reference current calculation

The reference value for the inductor current is derived based on the principle of ideal power balance between the input and output of the converter. Assuming lossless operation and continuous conduction mode (CCM) [23], the input power P_{in} is equal to the output power P_{out}. That is,

$$P_{\text{in}} = V_{in}(k) \cdot i_L^{\text{ref}} = V_{\text{out}}^* \cdot i_{\text{load}}(k) \tag{16}$$

solving in (16) for i_L^{ref} yields:

$$i_L^{\text{ref}} = \frac{V_{\text{out}}^* \cdot i_{\text{load}}(k)}{V_{in}(k)} \tag{17}$$

2.5. Split cost function

To address the NMP behavior inherent to boost converters, a modified cost function structure is proposed. Instead of using a unified objective for both switching states, the controller evaluates two separate cost functions depending on the candidate control input $u \in \{0, 1\}$. This allows the decision-making process to account for the different system responses when the switch is ON or OFF [24]. Specifically, when the switch is OFF ($u = 0$), as in (18).

$$J_{\text{OFF}} = \left(V_{\text{out}}^{*} - V_{\text{out}}^{\text{OFF}}(k+2)\right)^2 + \lambda_I \left(i_L^{\text{ref}} - i_L^{\text{OFF}}(k+2)\right)^2 \tag{18}$$

When the switch is ON ($u = 1$), as (19).

$$J_{\text{ON}} = -\left(V_{\text{out}}^{*} - V_{\text{out}}^{\text{ON}}(k+2)\right)^2 + \lambda_I \left(i_L^{\text{ref}} - i_L^{\text{ON}}(k+2)\right)^2 \tag{19}$$

In this formulation, the tracking objective for the output voltage is weighted differently based on the switch state [25]. In the OFF state, the controller aims to directly minimize the tracking error, encouraging the output voltage to approach its reference. In the ON state, the sign of the voltage error term is inverted. This design choice intentionally rewards energy accumulation in the inductor, anticipating future output needs. By doing so, the controller compensates for the delayed effect of control actions on the output voltage a key challenge posed by the NMP dynamics. The current regulation term remains quadratic and symmetric in both cases, ensuring consistent tracking of the reference inductor current.This split evaluation strategy improves both transient performance and steady-state regulation, while reducing the risk of overshoot or instability.

At each sampling instant, both cost functions are evaluated, and the optimal switching action is chosen as described in (20).

$$u^{*}(k+1) = \begin{cases} 1, & \text{if } J_{\text{ON}} < J_{\text{OFF}} \\ 0, & \text{otherwise} \end{cases} \tag{20}$$

To ensure safe operation, an overcurrent protection mechanism is also implemented (21).

$$\text{If } i_L^{\text{ON}}(k+2) > i_L^{\max} \Rightarrow u^{*}(k+1) = 0 \tag{21}$$

3. RESULTS AND DISCUSSION

3.1. Experimental setup

The experimental validation of the proposed dual-mode FS-MPC was performed on a hardware-in-the-loop (HIL) platform based on a ZedBoard Zynq-7000. The ARM cortex-A9 processor executed the real-time control algorithm, strictly following the sequence presented in Algorithm 1. This implementation excluded the FPGA fabric to assess the computational efficiency of the controller on a low-cost embedded processor. The experimental boost converter, built according to the parameters listed in Table 1, used an IRFZ44N MOSFET driven by an gate driver.

Voltage and current measurements were obtained using LV25-P and HAS50-S sensors, respectively. The analog signals were digitized by an external 16-bit ADS1115 ADC communicating via an I^2C bus at 1.2 MHz, ensuring synchronized sampling. The control algorithm—comprising state prediction, load-current estimation, and dual cost-function evaluation was executed every 10 μs (10 kHz switching rate). Real-time monitoring and data acquisition were achieved through MATLAB/Simulink in external mode, as illustrated in Figure 2.

Table 1. Boost converter parameters

Component	Value
Input voltage	[30 V–50 V]
Output voltage	[40 V–60 V]
Inductor	200 μH
Capacitor	1000 μF
Sampling time	10 μs
Reference switching frequency	10 kHz
Load resistor	[10 Ω – 20 Ω]

Algorithm 1 Dual-mode-MPC controller for buck converter

function DUAL-MPC($i_L(k), i_L(k-1), V_{out}(k), V_{out}(k-1), u(k-1), V_{ref}$)
  Set parameters: T_s, L, C, λ_I, $i_{L,max}$; Estimate load current i_L
  Predict next states using $u(k-1)$; Init: $J_{ON} \leftarrow \infty$, $J_{OFF} \leftarrow \infty$
  for $u \in \{0,1\}$ **do**
    Predict $(i_{L,k+2}, V_{out,k+2})$, compute e_V, e_I
    if $u=1$ **then**
      $J_{ON} \leftarrow f(e_V, e_I)$ (favor ON if $e_V > 0$)
    else
      $J_{OFF} \leftarrow f(e_V, e_I)$ (favor OFF if $e_V < 0$)
    end if
  end for
  $u(k+1) \leftarrow 1$ if $J_{ON} < J_{OFF}$ else 0; **return** $u(k+1)$
end function

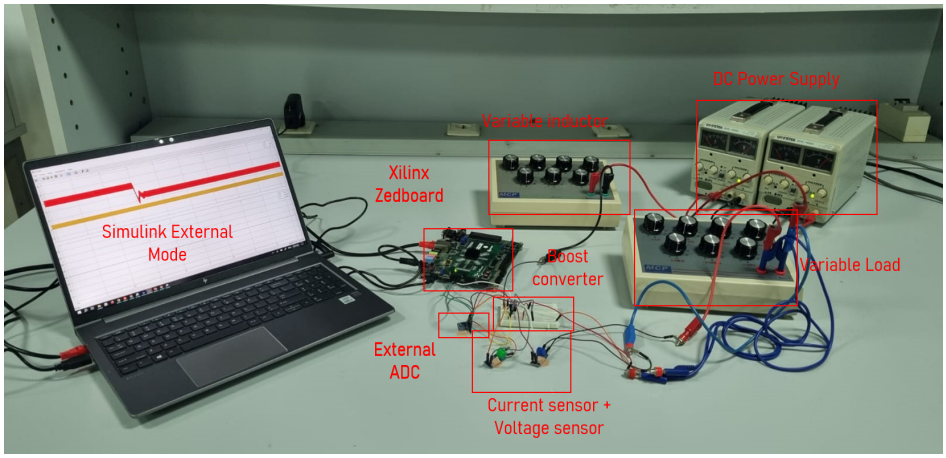


Figure 2. HIL setup

3.2. Experimental results

3.2.1. Test scenario 1: Variable input voltage with fixed output reference

In this first test, the objective is to evaluate the behavior of the boost converter and its control strategy under a time-varying input voltage while maintaining a constant output voltage reference. The input voltage V_{in} varies over time as described in (22).

$$V_{\text{in}}(t) = \begin{cases} 30\ \text{V}, & \text{for } 0 \leq t < 1\ \text{s} \\ 40\ \text{V}, & \text{for } 1 \leq t < 1.5\ \text{s} \\ 50\ \text{V}, & \text{for } t \geq 1.5\ \text{s} \end{cases} \tag{22}$$

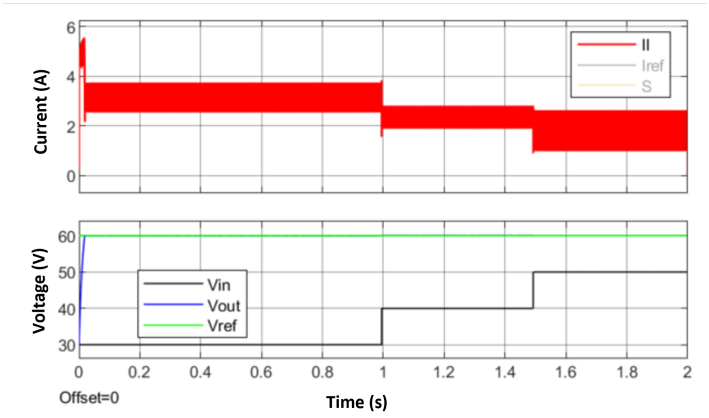
In contrast, Figure 3(a) illustrates the response when the proposed control technique is applied. The output voltage follows the reference value $V_{\text{ref}} = 60$ V with excellent accuracy and without overshoot as shown in Figure 3(b). The inductor current shows smooth transitions and improved tracking of the reference current, even during changes in input voltage. This confirms the enhanced robustness and dynamic performance of the proposed split cost function-based control.

3.2.2. Test scenario 2: Fixed input voltage with variable output reference

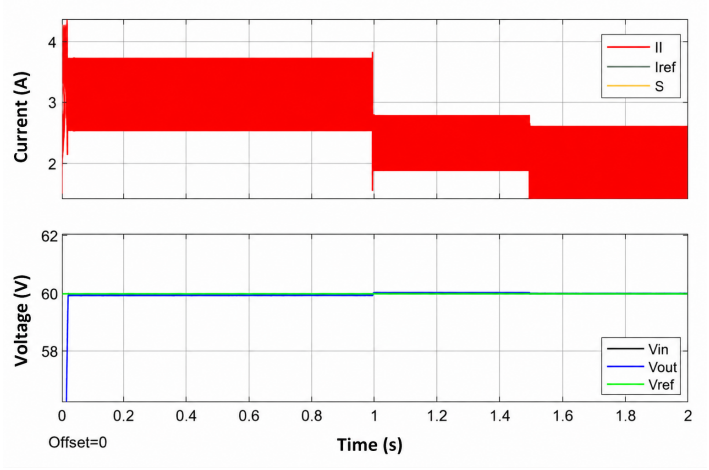
In this second test, the input voltage V_{in} is kept constant at 30 V throughout the simulation, while the output voltage reference V_{ref} is varied in steps to evaluate the converter's ability to track different reference values. The reference profile is defined as follows:

$$V_{\text{ref}}(t) = \begin{cases} 60\ \text{V}, & \text{for } 0 \leq t < 1\ \text{s} \\ 80\ \text{V}, & \text{for } 1 \leq t < 1.5\ \text{s} \\ 50\ \text{V}, & \text{for } t \geq 1.5\ \text{s} \end{cases}$$

This test evaluates the performance proposed approach. The goal is to verify how accurately and quickly the converter responds to downward steps in V_{ref}, and eliminates overshoot or undershoot during transients as it clearly shown in Figure 4 despite the abuse change in V_{ref}.



(a)



(b)

Figure 3. Converter response using proposed FS-MPC under input voltage variation: (a) system response using proposed FS-MPC and (b) zoomed view of the output voltage and current response

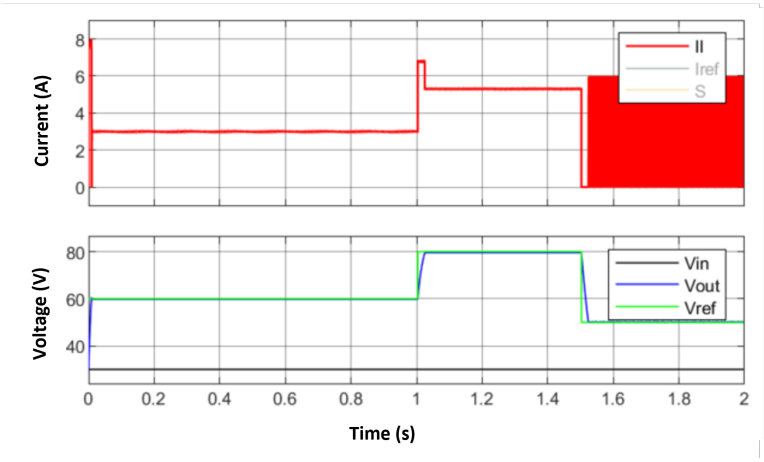


Figure 4. Converter response using proposed FS-MPC under reference voltage variation

3.2.3. Test scenario 3: Load variation under fixed input and output reference

In this third test, the robustness of the proposed control method is evaluated under a sudden and severe load variation. The input voltage V_{in} is held constant at 30 V, and the output voltage reference is fixed at $V_{\text{ref}} = 60$ V. The resistive load undergoes an abrupt change from 41.6 Ω to 4.16 Ω, corresponding to a tenfold increase in current demand. This variation is applied at $t = 1$ s, simulating a highly dynamic operating condition. The objective of this test is to observe how effectively the proposed split cost function-based FS-MPC handles the disturbance while maintaining output voltage regulation and current stability. The results show that the proposed controller quickly reacts to the increased load without overshoot or voltage drop, and restores steady-state conditions with minimal transient deviation as seen in Figure 5.

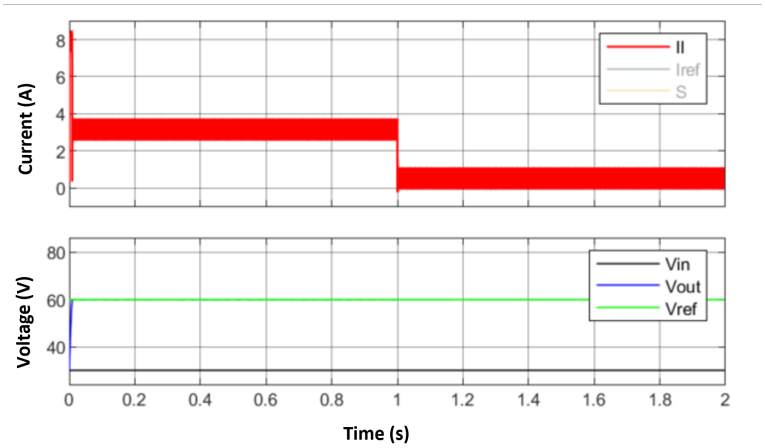


Figure 5. Converter response using proposed FS-MPC under load disturbance

3.3. Comparative analysis

For benchmarking purposes, the proposed method was compared with a standard FS-MPC implementation. As summarized in Table 2, the split cost-function strategy achieves lower overshoot and a shorter settling time while simultaneously reducing switching activity. In addition, it delivers a significant improvement in computational efficiency compared with the conventional approach. These results confirm that the proposed control strategy not only addresses the non-minimum phase challenge but also enhances real-time feasibility, making it suitable for embedded implementations on low-cost hardware platforms.

Table 2. Experimental performance comparison

Metric	FS-MPC (classical)	Proposed method
Overshoot (%)	6.8	0.9
Settling time (ms)	1.1	0.6
Computation time (ARM, μs)	18	8.5

4. CONCLUSION

This work presented a real-time implementation of a split cost function-based finite-set model predictive control (FS-MPC) strategy for a DC-DC boost converter using a hardware-in-the-loop (HIL) setup with a ZedBoard and an ADC. The proposed method successfully addressed the limitations of classical FS-MPC by improving voltage regulation, suppressing overshoot, and enhancing current tracking. Experimental results under different scenarios, including input voltage variation, reference changes, and sudden load disturbances, demonstrated the superior dynamic performance and robustness of the proposed approach. The controller was able to maintain output voltage stability and react quickly to system variations, confirming its suitability for real-time embedded power conversion applications.

FUNDING INFORMATION

Authors state no funding involved.

AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
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Anass Mansouri		✓		✓		✓	✓			✓	✓	✓	✓	✓
Ali Ahaitouf						✓	✓			✓			✓	✓

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal Analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject Administration
Fu : **Fu**nding Acquisition

CONFLICT OF INTEREST STATEMENT

The authors declare that there is no conflict of interest regarding the publication of this paper.

DATA AVAILABILITY

The data supporting this study's findings are available from the corresponding author, [JEL].

REFERENCES

[1] J. Wang, B. Wang, L. Zhang, J. Wang, N. I. Shchurov, and B. V. Malozyomov, "Review of bidirectional DC–DC converter topologies for hybrid energy storage system of new energy vehicles," *Green Energy and Intelligent Transportation*, vol. 1, no. 2, p. 100010, Sep. 2022, doi: 10.1016/j.geits.2022.100010.

[2] T. Sutikno, A. S. Samosir, R. A. Aprilianto, H. S. Purnama, W. Arsadiando, and S. Padmanaban, "Advanced DC–DC converter topologies for solar energy harvesting applications: a review," *Clean Energy*, vol. 7, no. 3, pp. 555–570, Jun. 2023, doi: 10.1093/ce/zkad003.

[3] M. F. Akhtar, S. R. S. Raihan, N. A. Rahim, M. N. Akhtar, and E. Abu Bakar, "Recent developments in DC-DC converter topologies for light electric vehicle charging: a critical review," *Applied Sciences*, vol. 13, no. 3, p. 1676, Jan. 2023, doi: 10.3390/app13031676.

[4] J. Asish, T. S. Megha, N. Laqueta, and R. Seethur, "Analysis of non-minimum phase fourth-order buck boost converter," in *2023 7th International Conference on Computer Applications in Electrical Engineering-Recent Advances (CERA)*, IEEE, Oct. 2023, pp. 1–6. doi: 10.1109/CERA59325.2023.10455739.

[5] A. Daraz, A. Basit, and G. Zhang, "Performance analysis of pid controller and fuzzy logic controller for dc-dc boost converter," *PLOS ONE*, vol. 18, no. 10, p. e0281122, Oct. 2023, doi: 10.1371/journal.pone.0281122.

[6] I. A. Ayad *et al.*, "Optimized nonlinear integral backstepping controller for dc-dc three-level boost converters," *IEEE Access*, vol. 11, pp. 49794–49805, 2023, doi: 10.1109/ACCESS.2023.3274773.

[7] L. Wu, J. Liu, S. Vazquez, and S. K. Mazumder, "Sliding mode control in power converters and drives: a review," *IEEE/CAA Journal of Automatica Sinica*, vol. 9, no. 3, pp. 392–406, 2022, doi: 10.1109/JAS.2021.1004380.

[8] M. Schwenzer, M. Ay, T. Bergs, and D. Abel, "Review on model predictive control: an engineering perspective," *International Journal of Advanced Manufacturing Technology*, vol. 117, no. 5–6, pp. 1327–1349, 2021, doi: 10.1007/s00170-021-07682-3.

[9] Y. Hakam, A. Gaga, M. Tabaa, and B. El hadadi, "Enhancing electric vehicle charger performance with synchronous boost and model predictive control for vehicle-to-grid integration," *Energies*, vol. 17, no. 7, 2024, doi: 10.3390/en17071787.

[10] P. Verma, M. N. Anwar, M. K. Ram, and A. Iqbal, "Internal model control scheme-based voltage and current mode control of DC-DC boost converter," *IEEE Access*, vol. 11, pp. 110558–110569, 2023, doi: 10.1109/ACCESS.2023.3320272.

[11] P. Karamanakos and T. Geyer, "Guidelines for the design of finite control set model predictive controllers," I*EEE Transactions on Power Electronics*, vol. 35, no. 7, pp. 7434–7450, Jul. 2020, doi: 10.1109/TPEL.2019.2954357.

[12] M. Schwenzer, M. Ay, T. Bergs, and D. Abel, "Review on model predictive control: an engineering perspective," *The International Journal of Advanced Manufacturing Technology*, vol. 117, no. 5–6, pp. 1327–1349, Nov. 2021, doi: 10.1007/s00170-021-07682-3.

[13] D. Rojas, M. Rivera, J. Munoz, C. Baier, and P. Wheeler, "A study of weighting factor design in model predictive control applications," in *2021 IEEE CHILEAN Conference on Electrical, Electronics Engineering, Information and Communication Technologies (CHILECON)*, IEEE, Dec. 2021, pp. 1–5. doi: 10.1109/CHILECON54041.2021.9702932.

[14] Q. Yang *et al.*, "Computationally efficient fixed switching frequency direct model predictive control," *IEEE Transactions on Power Electronics*, vol. 37, no. 3, pp. 2761–2777, 2022, doi: 10.1109/TPEL.2021.3114979.

[15] F. A. Villarroel et al., "Stable shortest horizon fcs-mpc output voltage control in non-minimum phase boost-type converters based on input-state linearization," *IEEE Transactions on Energy Conversion*, vol. 36, no. 2, pp. 1378–1391, 2021, doi: 10.1109/TEC.2021.3055733.
[16] N. Dias and A. J. Naik, "Design, modeling and simulation of bidirectional buck and boost converter for electric vehicles," in *2022 International Conference for Advancement in Technology, ICONAT*, 2022. doi: 10.1109/ICONAT53423.2022.9725830.
[17] E. Zafra, S. Vazquez, T. Geyer, R. P. Aguilera, and L. G. Franquelo, "Long prediction horizon FCS-MPC for power converters and drives," *IEEE Open Journal of the Industrial Electronics Society*, vol. 4, pp. 159–175, 2023, doi: 10.1109/OJIES.2023.3272897.
[18] B. Fan, T. Liu, F. Zhao, H. Wu, and X. Wang, "A review of current-limiting control of grid-forming inverters under symmetrical disturbances," *IEEE Open Journal of Power Electronics*, vol. 3, pp. 955–969, 2022, doi: 10.1109/OJPEL.2022.3227507.
[19] G. Sanchez, M. Murillo, L. Genzelis, N. Deniz, and L. Giovanini, "MPC for nonlinear systems: a comparative review of discretization methods," in *2017 XVII Workshop on Information Processing and Control (RPIC)*, IEEE, Sep. 2017, pp. 1–6. doi: 10.23919/RPIC.2017.8214333.
[20] B. Bandyopadhyay and M. Patil, "An overview of non-minimum phase systems," 2024, pp. 1–29. doi: 10.1007/978-3-031-70988-31.
[21] X. Zhang, Y. Cao, C. Zhang, and S. Niu, "Model predictive control for pmsm based on the elimination of current prediction errors," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 12, no. 3, pp. 2651–2660, 2024, doi: 10.1109/JESTPE.2024.3387428.
[22] P. Pal, R. K. Behera, and U. R. Muduli, "Eliminating current sensor dependencies in dab converters using a luenberger observer-based hybrid approach," *IEEE Transactions on Industry Applications*, vol. 60, no. 4, pp. 6380–6392, 2024, doi: 10.1109/TIA.2024.3384465.
[23] I. Bashir, A. H. Bhat, and S. Ahmad, "A review on soft switched PFC boost converter for efficient lowering of switching losses," *Electric Power Systems Research*, vol. 242, 2025, doi: 10.1016/j.epsr.2025.111430.
[24] C. Minchala-Ávila, P. Arévalo, and D. Ochoa-Correa, "A systematic review of model predictive control for robust and efficient energy management in electric vehicle integration and v2g applications," *Modelling*, vol. 6, no. 1, 2025, doi: 10.3390/modelling6010020.
[25] E. Zerdali, M. Rivera, and P. Wheeler, "A review on weighting factor design of finite control set model predictive control strategies for AC electric drives," *IEEE Transactions on Power Electronics*, vol. 39, no. 8, pp. 9967–9981, Aug. 2024, doi: 10.1109/TPEL.2024.3370550.

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