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Modelling enhancement-mode GaN HEMTs with graded AlGaN barrier, graphene passivation, and dual field plates via TCAD

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ABSTRACT

An enhancement-mode aluminum gallium nitride (AlGaN)/gallium nitride (GaN) HEMT is presented in which graphene-capped SiN passivation, a recessed composite p-GaN gate, dual discrete field plates, and a compositionally graded AlGaN barrier (35%→18% Al) are co-engineered in a single device. The novelty lies in integrating these four techniques within a single enhancement-mode architecture to simultaneously suppress surface trapping, reduce gate leakage, strengthen electrostatic gate control, and redistribute the electric field for higher breakdown and more uniform field profiles. TCAD results indicate a threshold voltage (Vth) of +2.6 V, transconductance (gm) of 335 mS/mm, and breakdown voltage (Vbr) around 1 kV. The radio-frequency (RF) analysis shows a cut-off frequency (fT) of ~42.57 GHz, with favorable gate capacitance characteristics. These outcomes show that co-optimization delivers normally-off operation with improved breakdown and RF speed relative to using the techniques separately, supporting suitability for high-power, high-frequency applications.

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1. INTRODUCTION

Gallium nitride (GaN)-based heterostructure field-effect transistors have garnered considerable attention for applications in high-frequency, radio-frequency (RF), and high-power electronic systems due to their inherent material advantages, which include a wide bandgap, high-breakdown field, excellent electron mobility, and superior thermal conductivity [1]. The aluminum gallium nitride (AlGaN)/GaN heterostructure, in particular, facilitates the spontaneous formation of a high-density two-dimensional electron gas (2DEG) at the interface without requiring intentional doping. This feature results in a low-resistance conduction path that is highly desirable for efficient power switching and RF signal amplification [2].

Although AlGaN/GaN high electron mobility transistors (HEMTs) exhibit excellent performance, their reliability is limited by localized electric field crowding near the gate, causing early breakdown and current collapse through trap formation [3], [4]. Carrier trapping, aggravated by self-heating, increases on-resistance and reduces efficiency [5]. Furthermore, achieving enhancement-mode operation remains challenging due to strong polarization effects that sustain a conductive channel without gate bias [6], [7].

To address these issues, graded AlGaN barriers have been introduced to smooth the polarization charge distribution and improve mobility and threshold control while minimizing defects [8]–[10]. Recessed

gate designs with p-GaN caps further enhance gate control and reduce leakage [11]. In addition, field-plate (FP) structures redistribute the electric field and increase breakdown voltage while mitigating current collapse [4], [12], [13], with reports of breakdown improvements from several hundred volts to over 1100 V under optimized configurations [14], [15]. Dual field plates further help balance breakdown strength, switching speed, and gate charge [14], [16]. Moreover, the integration of graphene passivation has shown promise in enhancing device stability by reducing surface-state trapping and improving thermal management under high-power and humid conditions without introducing parasitic effects [17].

While each of these techniques, such as graded barriers, recessed gates, field plates, and graphene passivation, offers performance improvements in isolation, their full potential remains underexplored in a single co-optimized architecture. The challenge lies in their integration, which introduces complexities related to strain management, electrostatic interference, and fabrication compatibility. To date, few studies integrate graded AlGaN barriers, recessed p-GaN gates, dual field plates, and graphene passivation in one co-optimized architecture. In particular, it remains unclear whether such integration yields merely additive gains or produces synergistic behavior where the combined effect exceeds the sum of individual optimizations.

Motivated by this gap, the present study introduces a GaN HEMT structure that integrates a compositionally graded AlGaN barrier with an aluminum profile transitioning from 0.35 to 0.18, a recessed p-GaN gate, a dual discrete field plate design, and graphene on SiN passivation. Simulation results validate that this structure achieves multiple performance milestones: i) Enhancement-mode operation: $V_{th} = +2.6$ V with strong transconductance ($g_m = 335$ mS/mm); ii) High-voltage robustness: $V_{br} \approx 1001$ V; and iii) RF readiness: $f_T = 42.57$ GHz; reduced gate-to-drain capacitance (C_{gd}). These improvements reflect not only a summation of enhancements but also the emergence of synergistic effects where integrated optimization leads to non-linear, compounded performance gains. These results further support next-generation high-power RF/power GaN electronics by providing integration-focused design guidance with improved reliability margins against field crowding and trap-related instabilities.

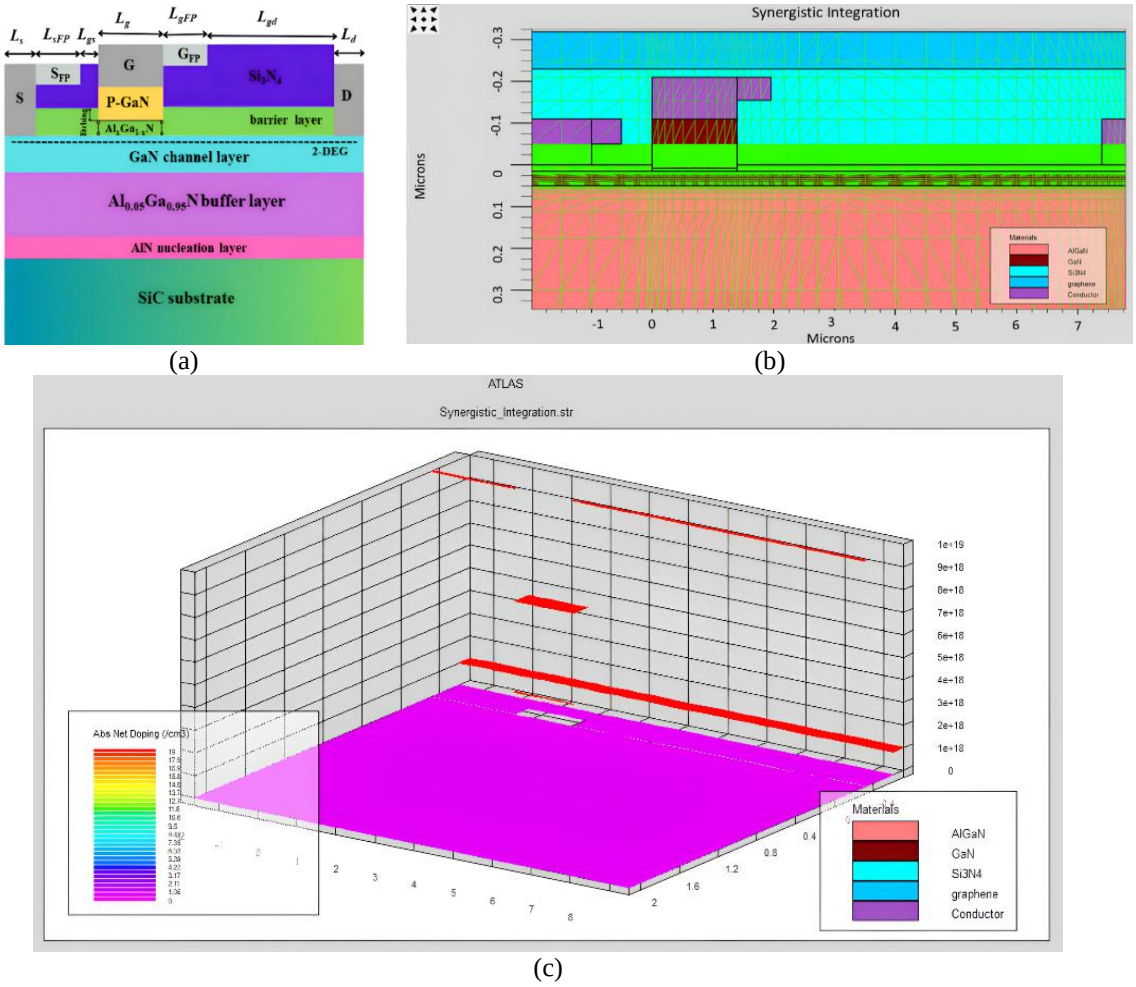
2. METHOD

The device is modeled using Silvaco TCAD, with ATHENA handling the process simulation covering deposition, diffusion, etching, and ATLAS performing the subsequent electrical and quantum-mechanical analyses. Fabrication begins on a 250 µm SiC substrate, chosen for its superior thermal conductivity and ability to sustain high-power operation. A 30 nm AlN nucleation layer promotes lattice matching and high-quality epitaxial growth, followed by a 5% AlGaN buffer layer that enhances crystalline quality and reduces dislocation density. On top of this, a 35 nm GaN channel is formed to serve as the primary electron transport region.

The barrier layer is compositionally graded, with aluminum content gradually decreasing from 35% to 18%. This smooth compositional transition mitigates polarization-induced charge spikes and strengthens electron confinement at the heterointerface, resulting in improved carrier transport. Above the barrier lies a p-GaN cap layer (118 nm) doped with magnesium at 5×10^{18} cm^{-3}, which enables normally-off (enhancement-mode) behavior. The p-GaN region under the gate is precisely recessed through ATHENA's etching simulation to achieve a positive threshold voltage, offering tighter gate control and enhanced switching stability. Once the epitaxial layers are complete, metallization, diffusion, and dielectric passivation steps are simulated to finalize the device structure prior to electrical testing.

A Ni/Au Schottky gate contact with a work function of 5.1 eV provides strong gate modulation, while Ti/Al/Ni/Au ohmic contacts with a work function of 4.04 eV ensure low contact resistance at the source and drain. The gate length is set to 1.4 µm, with 1 µm source and drain contacts, resulting in a total device length of 10.4 µm. Key device parameters used in TCAD simulation are shown in Table 1. Moreover, a Si_3N_4 passivation layer is included, and dual field plates connected to the gate and source are positioned over the passivation to redistribute the electric field, reduce gate-edge crowding, and suppress trap-assisted current collapse. Further reliability is achieved through the integration of a monolayer graphene sheet atop the Si_3N_4 passivation. Graphene on Si_3N_4 functions as an atomically thin, conductive, and chemically inert cap that screens surface charge, passivates dangling-bond/defect states, and stabilizes the surface Fermi level, thereby suppressing trap-assisted current collapse under high field.

Figure 1 illustrates the structural design and simulation framework of the proposed AlGaN/GaN HEMT. The recessed and graded barrier configuration, together with graphene and Si_3N_4 passivation as shown in Figure 1(a), is implemented to improve electrostatic control and electric-field distribution, as confirmed by the 3D layer and doping profile in Figure 1(b). Furthermore, the finely resolved mesh shown in Figure 1(c) enables precise extraction of direct current (DC) and RF characteristics by capturing peak electric-field regions and parasitic capacitances with high fidelity. In the proposed architecture, the graded barrier primarily strengthens the electrostatic control of the 2DEG and supports stable V_{th} while maintaining strong g_m.



(a) (b)

(c)

Figure 1. Structural configuration of the proposed AlGaN/GaN HEMT: (a) The proposed 2D schematic view of AlGaN/GaN HEMT with AlGaN barrier, GaN channel, Si_3N_4 passivation, graphene cap, and contacts; (b) 3D doping and layer distribution used to verify the recessed and graded regions; and (c) meshed simulation domain in ATLAS used for DC and RF analysis to accurately capture peak electric fields and parasitic capacitances

The recessed p-GaN gate enforces enhancement-mode behavior by depleting the channel at $V_g = 0$ V and reducing leakage. Dual field plates shift and spread the peak electric field away from the gate edge, improving V_{br} and reducing trapping-induced dispersion. Graphene passivation suppresses surface trapping and stabilizes the gate–drain surface potential, supporting improved dynamic behavior and reduced C_{gd} coupling. The finalized structure is imported into Silvaco ATLAS for comprehensive electrical characterization. Within ATLAS, the Poisson-Schrödinger and drift-diffusion equations are solved self-consistently under Fermi–Dirac statistics to capture both quantum confinement and carrier transport [18]. The Shockley-Read-Hall recombination mechanism is incorporated to model carrier generation and recombination processes, while a fine mesh grid ensures numerical precision, particularly in the recessed gate region where electric fields are most intense.

$$-\frac{\hbar}{2}\frac{1}{dz^2}\frac{1}{m*(z)}\psi(z) + V(z)\psi(z) = E_i\psi(z) \quad (1)$$

$$\Delta.D(z) = -[n(z) - \sigma(z)] \quad (2)$$

$$div(\varepsilon\nabla\psi) = -\rho \quad (3)$$

$$\frac{\partial n}{\partial t} = \frac{1}{q}div\,\overrightarrow{J_n} + G_n - R_n \quad (4)$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q} div \overrightarrow{J_p} + G_p - R_p \quad (5)$$

Simulation results confirm that the p-GaN recessed, graded barrier AlGaN/GaN HEMT achieves high breakdown voltage, strong gate controllability, and minimal current collapse. The combined effects of the graded barrier, dual field plates, and graphene passivation create a balanced architecture optimized for high-power and high-frequency applications, demonstrating the effectiveness of structural innovation and process-level refinement in advancing GaN-based transistor technology.

Table 1. Key device parameters used in TCAD

Feature	Material	Thickness/dimensions (μm)
Substrate	SiC	250
Nucleation	AlN	0.03
Buffer	$Al_{0.05}Ga_{0.95}N$	2
Channel	GaN	0.035
Barrier (graded)	$Al_xGa_{1-x}N$ (x: 0.35→0.18)	0.008
Barrier (ungraded)	$Al_xGa_{1-x}N$ (x: 0.28)	0.015
p-GaN cap	p-GaN (Mg)	0.118
Gate contact (L_g)	Ni/Au Schottky	1.4
Ohmic contact (L_s & L_d)	Ti/Al/Ni/Au	1
Field plates (L_{sFP} & L_{gFP})	Ti/Al/Ni/Au	0.6

3. RESULTS AND DISCUSSION

Figure 2 illustrates the energy band diagram of the proposed device under ON-state bias conditions. The energy profile at the AlGaN/GaN heterointerface reveals a noticeable drop in the conduction band beneath the Fermi level in the ON-state, signifying strong accumulation of the 2DEG with efficient current flow through the channel. This phenomenon is primarily governed by polarization-induced charge accumulation in the graded AlGaN barrier, with the applied gate bias actively modulating the charge distribution and electrostatic potential profile. This behavior results from the combined effects of the p-GaN cap layer, which introduces a surface depletion region, and the recessed gate, which enhances gate control and ensures a positive threshold voltage. The graded barrier further smooths the band transition, reducing interface states and enhancing the ON-state performance.

Figure 3(a) shows changes in the drain current (I_D) with varying drain voltage for different gate-to-source voltages varying from 2 V to 8 V in steps of 1 V. The proposed combined structure achieves an impressive drain current of 0.63825 A/mm, showing potential for handling high power. At gate-to-source voltage (V_{gs}) = 3 V, the I_D after reaching saturation shows significant current droop up to V_{DS} = 20 V, indicating higher thermal stability. The transfer characteristics of $Al_xGa_{1-x}N$/GaN HEMT shown in Figure 3(b) exhibit a clear enhancement-mode behavior, with drain current increasing with V_{gs} beyond threshold voltage. The designed structure achieves a drain current $I_{D\text{-}on}$ of 0.54874 A/mm at an Al concentration of 0.35 when the drain voltage is fixed at 15 V. This higher drain current indicates a stronger device capability with better performance in power and RF applications.

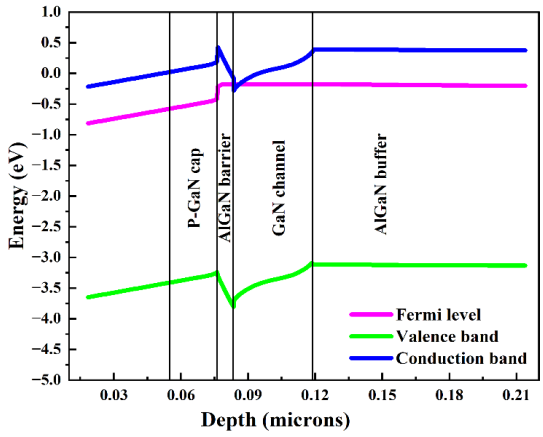


Figure 2. On-state band diagram of the proposed composite HEMT, illustrating enhanced 2DEG confinement under bias due to the graded AlGaN barrier and recessed p-GaN gate electrostatics

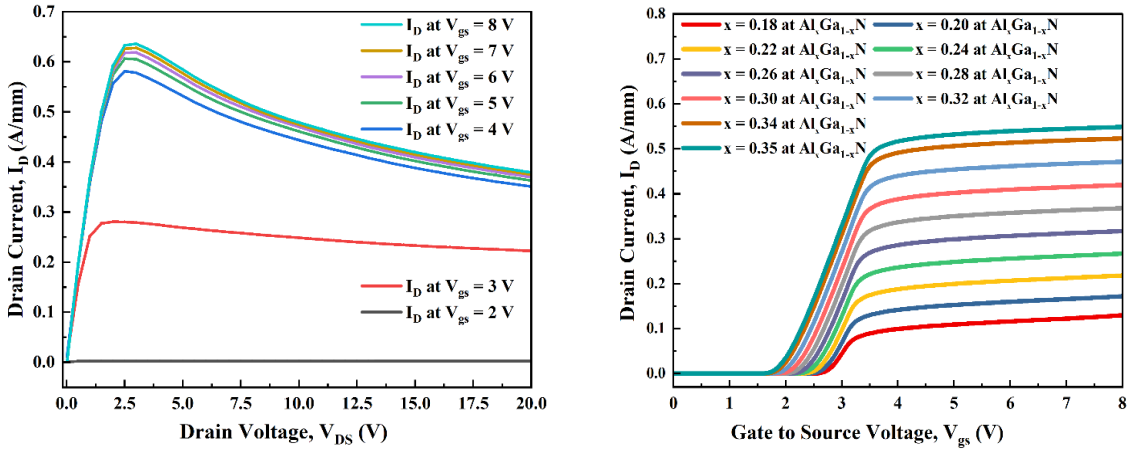


Figure 3. Electrical characteristics of the proposed composite HEMT: (a) output characteristics (I_D–V_DS) of the proposed composite HEMT at different V_gs, confirming high current drivability with stable channel modulation across the applied gate bias range, and (b) transfer characteristics of the proposed structure, demonstrating enhancement-mode operation through a positive V_th

As shown in Figure 4, the combined structure achieves a maximum V_{th} of 2.6 V at an Al concentration of 0.18, which decreases with an increase in Al concentration. It provides a visual comparison that interprets how barrier grading affects V_{th} and a maximum transconductance of 335 mS/mm is attained at an Al concentration of 0.35. Overall, these trends further underscore the effectiveness of the graded design in optimizing performance for high-frequency and high-power applications. Moreover, in the proposed composite structure, the subthreshold swing (SS) demonstrates a non-linear dependence on Al composition, reaching a minimum of 24.62 mV/dec at optimized conditions, indicative of excellent electrostatic control. The same configuration effectively suppresses gate leakage, with the lowest leakage current recorded at 2.44×10^{-14} A. Furthermore, a maximum $I_{D,ON}/I_{D,OFF}$ ratio of 1.2174×10^{14} is achieved at x = 0.22, highlighting the structure's capability for robust channel formation, superior switching efficiency, and minimal off-state conduction—key features for low-power and high-performance device applications. Overall, these DC results address the gap highlighted in the Introduction by showing that the integrated architecture delivers normally-off control while maintaining strong channel performance. The comparative nature of the plot emphasizes the insight that there is a trade-off between threshold voltage and channel conductivity.

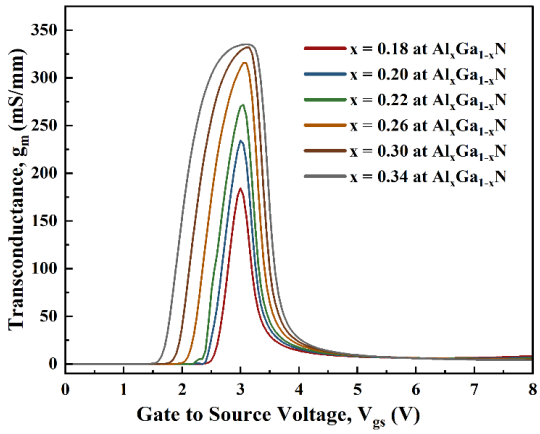
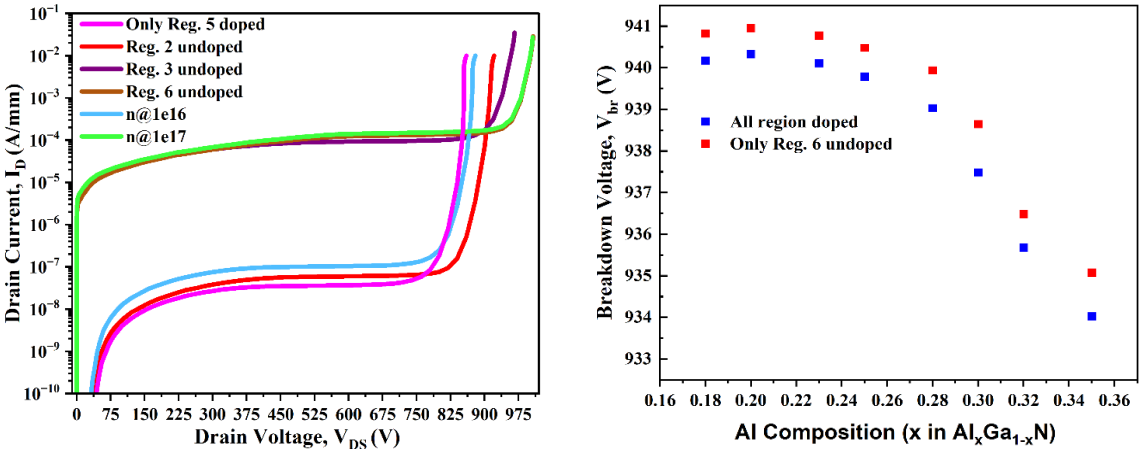


Figure 4. Transconductance vs gate to source voltage for different graded barrier Al concentrations, showing that barrier grading strengthens gate control and improves g_m while enabling V_{th} tuning

Breakdown voltage is crucial for high-power and RF applications, so different doping conditions were tested in the proposed HEMT to analyze its breakdown behavior. Figure 5(a) shows that the highest drain voltage is achieved when all regions are doped or all except region six. This plot illustrates how breakdown

voltage varies with the AlGaN barrier composition under two doping conditions. It elucidates the non-linear relationship between barrier Al content and breakdown robustness, underscoring the insight that moderate Al content (~20%) maximizes breakdown voltage, whereas too high Al content can actually reduce it. The p-GaN cap is doped with magnesium at about 5×10^{18} per cubic centimeter, while other layers receive n-type doping at 1×10^{17} per cubic centimeter. This doping setup improves the electric field distribution and breakdown performance. To further assess the effect, the aluminum content in the AlGaN barrier is adjusted, as depicted in Figure 5(b). It is observed from the adjustment that the breakdown voltage increases with Al content up to 20 percent, but decreases beyond that. The highest breakdown voltage of around 1001 V is observed when all regions except region six are doped. A graphene passivation layer is added to stabilize surface electric fields and prevent leakage under high-voltage stress, ensuring device reliability in high-voltage operation.



(a) (b)

Figure 5. Breakdown characteristics of the proposed composite HEMT: (a) Breakdown characteristics of the proposed composite HEMT under different doping conditions, showing the sensitivity of V_br to charge distribution and field management in the gate-edge regions; and (b) Comparison of breakdown voltages for varying Al concentration of the graded barrier layer when all regions are doped, and when all regions except region 6 are doped

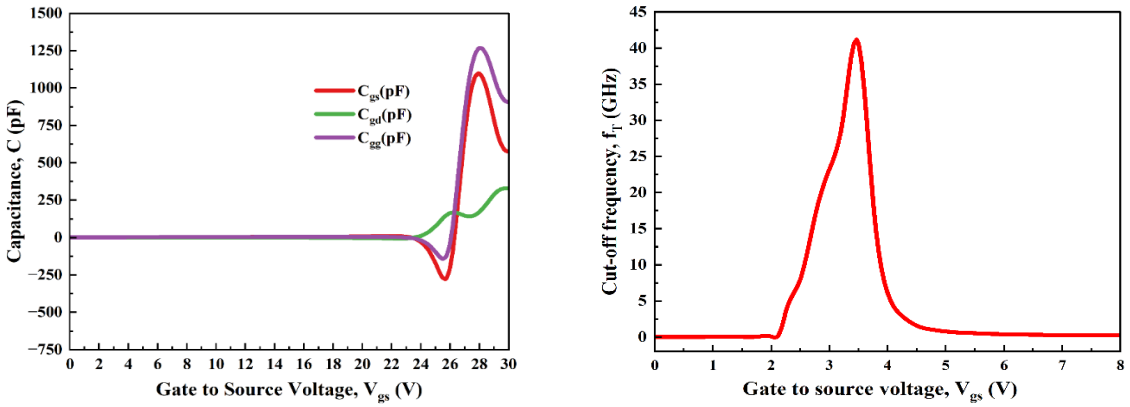
Figure 6(a) shows C_{gs}, C_{gd}, and C_{gg} versus V_{gs} for graded and ungraded devices. In the graded case, C_{gs} and C_{gg} stay near zero or negative at low V_{gs} due to deep depletion and polarization effects. Both rise sharply with V_{gs}, peaking around 1100 pF, then decline as the channel forms. Low C_{gs} ensures better high-frequency performance, confirming improved gate control and reliable normally-off behavior. The proposed structure achieves a notable cut-off frequency of ~42.57 GHz (Figure 6(b)) and a low DIBL of 4.25 mV/V, which highlights its strong potential for integration into RF, microwave, and high-speed digital systems where superior high-frequency performance is critical. The cut-off frequency, denoted as f_T, represents the frequency at which the current gain of the transistor drops to unity. It is a key figure of merit in high-frequency transistor operation and is mathematically defined as (6).

$$f_T = \frac{g_m}{2*\pi*C_{gg}} \tag{6}$$

Although the focus of this study is on small-signal characteristics, large-signal RF behavior remains essential for evaluating power performance. Key metrics such as power-added efficiency (PAE) and power gain determine suitability for GHz operation. Comparable enhancement-mode GaN HEMTs have demonstrated power-added efficiency (PAE) values of approximately 70% and output power densities near 1 W/mm output at V_{DS} = 10 V, with advanced devices exceeding 80% PAE in the 2–3 GHz range and 10–20 dB gain at microwave frequencies. Future work should include large-signal characterization, such as load-pull measurements and RF stress testing, to verify that the proposed device maintains high efficiency and reliability under real operating conditions.

To contextualize the advancements achieved through our integrated device architecture, it is instructive to examine how these performance metrics compare against established GaN HEMT technologies reported in the literature. While the earlier discussions have detailed the physical mechanisms and simulated

outcomes of the proposed structure, a broader performance landscape allows us to assess whether these improvements are incremental or indicative of a more fundamental design shift. Accordingly, a comparative summary is presented in Table 2, incorporating key figures of merit alongside the structural innovations employed in each referenced work.



(a) (b)

Figure 6. Capacitance characteristics and RF performance of the proposed composite HEMT: (a) Capacitance characteristics of the proposed composite HEMT, indicating reduced C_{gd} that supports improved switching or RF behavior; and (b) Cut-off frequency vs gate to source voltage of the composite HEMT, identifying the bias region that maximizes RF performance

Table 2. Comparative performance metrics of reported GaN HEMTs employing individual or partial enhancement strategies with the proposed synergistically integrated structure

Ref	Techniques used	g_m (mS/mm)	I_{Dmax} (A/mm)	f_T (GHz)	V_{br} (V)	V_{th} (V)	SS (mV/decade)	On/off ratio
[9]	p-GaN + gate recess + graded barrier (simulation)	94.7	0.718	–	–	8.6	–	–
[11]	Gate recess + FP (experimental)	210	0.61	16	160	0.5	80	10^8
[14]	Dual FP (simulation)	–	–	17.86	750	–	–	–
[15]	FP (simulation)	16.3	–	–	1100	-3.3	–	–
[19]	Gate recess + FP (simulation)	232	1.5	49.8	633.1	2.8	–	–
[20]	p-GaN (simulation)	–	0.243	–	1487	1.1	–	–
[21]	Ultra-thin barrier layer (simulation)	430	1.01	27	650	0.5	63	10^{12}
[22]	p-GaN (simulation)	511	0.95	122	825	–	–	–
[23]	Gate FP (simulation)	337	1.85	18	690	–	–	–
[24]	Thin barrier layer (simulation)	–	0.304	–	–	1.39	–	11.4×10^{14}
[25]	Gate recess (experimental)	370	1.13	26	–	–	–	–
This work	p-GaN + gate recess + graded barrier + dual FP + graphene	335	0.638	42.57	1001.17	2.6	24.61	1.03×10^{14}

Table 2 shows that most studies use one or two techniques, improving specific traits but sacrificing others. Our design combines five methods, achieving high threshold voltage, low SS, strong RF performance, and stable breakdown together, something prior isolated approaches could not deliver. For instance, gate-recess and field-plate integration in [19] reports a higher f_T (~49.8 GHz) but with lower V_{br}. Similarly, using only p-GaN in [20] yields a higher V_{br} (1487 V) but a lower V_{th} (1.1 V). The proposed design provides a more balanced trade-off by maintaining enhancement-mode operation while achieving V_{br} near 1 kV with a compact 1.4 µm gate length. In addition, ultra-thin barrier approaches in [21] achieve high g_m (430 mS/mm) but at the expense of V_{th} (0.5 V), whereas our structure achieves $V_{th} = 2.6$V while maintaining a stable transconductance profile. Overall, these comparisons indicate that meaningful performance advancement in GaN HEMTs is enabled not by isolated optimizations, but by careful co-integration of complementary design strategies.

The proposed co-integrated architecture also offers practical guidance for fabrication by separating which process "knobs" control which device outcomes. In particular, the recessed p-GaN gate depth and Mg activation primarily set enhancement-mode behavior (V_{th}) and gate leakage, the graded barrier provides an additional handle to tune electrostatics and maintain a stable g_m profile, and the dual field plates mainly govern peak-field redistribution and V_{br}. Graphene and SiN passivation then targets surface-trap suppression to limit current collapse and dynamic R_{on}. This role-based mapping reduces trial-and-error during epitaxy

and lithography by narrowing the set of critical variables and providing a structured co-optimization path when transferring the design from TCAD to hardware.

Since this work is TCAD-based, experimental performance may deviate due to process variability, particularly p-GaN activation and recess control, ohmic contact resistance, and interface/surface trap densities. Implementing the proposed enhancement-mode GaN HEMT is feasible, but practical fabrication can deviate from TCAD simulation results. Achieving the required doping profiles is challenging: p-type GaN for normally-off operation requires high-temperature acceptor activation (up to ~1200 °C), and heavy n-type doping for low-resistance contacts is also difficult. In practice, low-resistance access regions typically rely on alloyed metallization (e.g., Ti/Al/Ni/Au), yet contact resistances of ~0.5–1 Ω·mm and interface or surface traps can degrade mobility and increase dynamic R_{on}, demanding careful passivation. Integrating p-GaN recess and barrier engineering with field-management features requires tight epitaxy and process control, so interface roughness and trapping may cause differences between simulated and measured performance. Nevertheless, similar normally-off AlGaN/GaN HEMT structures have been demonstrated in literature, and ongoing advances in GaN processing (such as improved lithography, selective area doping, and regrowth techniques) continue to mitigate these fabrication challenges.

In spite of the fabrication-related limitations, practical implementation remains feasible because this TCAD study is based on fabrication-relevant materials and validated physical models. The key outcome is that synergistic integration of advanced techniques can be co-optimized to balance normally-off control, breakdown robustness, and RF performance within a single device. Overall, the results suggest a move beyond additive optimization toward a co-engineered device architecture that manages multiple trade-offs in a unified and scalable framework.

4. CONCLUSION

This study co-designed and validated via TCAD an enhancement-mode GaN HEMT integrating a graded barrier, recessed p-GaN gate, dual field plates, and graphene passivation. The simulated device results confirm that this co-integration can simultaneously strengthen gate control, enhance breakdown robustness, and preserve RF performance. A key limitation of this work is that the results are simulation-only, and practical realization may be influenced by fabrication constraints such as p-GaN activation and recess control, ohmic contact resistance, and interface/surface trap densities. Nevertheless, the proposed architecture provides a promising route for next-generation GaN power and RF electronics, supporting 5G RF front-ends, EV power conversion, and renewable-energy inverters where high efficiency, high voltage robustness, and reliability are critical. Future work will focus on experimental fabrication and validation, including large-signal RF characterization, stress or reliability testing (e.g., dynamic R_{on} and bias-temperature stress), and process optimization to reduce leakage and trapping effects.

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AUTHOR CONTRIBUTIONS STATEMENT

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C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

The authors state no conflict of interest with respect to the research, authorship, and publication of the article.

DATA AVAILABILITY

The authors confirm that the data supporting the findings of this study are available upon request from the corresponding author.

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