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Fuzzy logic-based adaptive PLL switching strategy for voltage control in DVR assisted grid tied PV systems

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ABSTRACT

This study aims to enhance power quality in grid-connected photovoltaic (PV) systems by introducing an intelligent fuzzy logic-based adaptive control strategy for dynamic PLL switching in a DVR-supported configuration. A 100-kW grid-tied PV system is modeled with a digital phase-locked loop (DPLL), a conventional synchronous reference frame PLL (CTPLL), and a dynamic voltage restorer (DVR). A Mamdani-type fuzzy inference system (FIS) performs real-time PLL selection based on phase-wise real-time fault monitoring. The system was tested under symmetrical and asymmetrical 20% sag and swell conditions, evaluating voltage stability at both PCC and load, total harmonic distortion (THD), recovery time, and synchronization accuracy. Results show that the proposed method reduces unnecessary DVR voltage injection from ~50 V to ~5–6 V under healthy conditions, maintains a near-unity power factor (< 0.95), and achieves up to 15% THD reduction in inverter current and PCC currents compared to DPLL-only operation. Recovery times improved by up to 25%, with stable synchronization maintained in all fault cases. The integration of adaptive PLL switching and targeted DVR activation offers a novel, hardware-efficient approach to harmonic suppression, voltage stabilization, and fault resilience in medium-scale PV systems.

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1. INTRODUCTION

Solar photovoltaic (PV) systems have emerged as a key component in the transition to sustainable energy due to their clean and renewable nature. However, integrating these systems into the utility grid introduces several technical challenges. The intermittent nature of solar energy, along with the switching behavior of power electronic converters, often results in power quality issues such as voltage fluctuations, harmonic distortion, frequency instability, and synchronization errors. These disturbances compromise grid stability, disrupt PV inverter performance, and degrade voltage quality at the load terminals [1]-[5].

Synchronization between the PV inverter and the utility grid is vital for stable power exchange and compliance with grid code requirements. Accurate phase detection supports effective current injection, reactive power compensation, and fault ride-through capability. To achieve synchronization, methods such as zero-crossing detection, frequency-locked loops (FLL), second-order generalized integrators (SOGI), and phase-locked loops (PLL) have been explored [6]-[8]. Among them, the synchronous reference frame PLL (SRF-PLL) is the most widely adopted due to its structural simplicity, ease of implementation, and reliable operation under

balanced, steady-state conditions [9]-[13]. However, the performance of SRF-PLL deteriorates significantly under voltage unbalance, harmonic-rich environments, and transient grid disturbances.

Under such conditions, it suffers from poor phase tracking, sluggish dynamic response, and vulnerability to harmonic injection. Various improvements, including adaptive filtering, feedforward compensation, and optimized tuning strategies, have been proposed to enhance its performance [14]-[17]. Nonetheless, SRF-PLL continues to underperform during severe grid faults such as voltage sags and swells, resulting in inaccurate synchronization and degraded output power quality [18], [19].

To overcome these challenges, digital phase-locked loops (DPLLs) have been developed in the discrete-time domain, offering enhanced precision and robustness during dynamic grid conditions. Although some digital variants have been previously proposed, many lacked practical implementation or failed to demonstrate their applicability in real-time [20]-[24]. In our prior work [25], a DPLL based on backward Euler approximation was implemented and validated under various symmetrical and asymmetrical fault conditions. This design not only improved phase tracking but also significantly reduced total harmonic distortion (THD), thereby enhancing overall power quality.

Yet, the DPLL alone could not address voltage quality issues at the load and point of common coupling (PCC) during grid faults. Voltage sags and swells persisted due to the inverter's limited capability in dynamic voltage support. Dynamic voltage restorers (DVRs) have proven effective in regulating voltage under such conditions [26]-[30]. Recent studies highlight that PI controllers suffer from drawbacks such as delayed recovery and high sensitivity to grid disturbances, while fixed-mode DVRs can inject unnecessary compensating voltage even during normal operating conditions. This not only wastes energy but also imposes additional stress on dynamic voltage restorer (DVR) components, potentially affecting both the load and the grid [31], [32]. To address these issues, the proposed design employs sliding mode control (SMC), which offers strong robustness under fast transients, effective operation during unbalanced conditions, and minimal tuning requirements, thereby enhancing both efficiency and reliability. Despite these advancements, three key limitations persist in existing approaches: i) SRF-PLL performs reliably only under ideal conditions but fails to synchronize accurately during disturbances; ii) While DPLL improves harmonic suppression and synchronization under faults, it lacks voltage support capability; and iii) DVRs, though effective in compensating faults, introduce inefficiencies when operated without intelligent control in normal grid conditions.

To overcome the above challenges, this work presents a novel hybrid control architecture that unifies synchronization and intelligent voltage regulation without introducing additional system complexity. A phase-wise monitoring system continuously evaluates the grid condition and classifies it as either nominal or faulted. Based on this evaluation, the fuzzy inference system (FIS) dynamically selects the appropriate PLL: the CTPLL is engaged during normal grid operation due to its stable and precise phase-tracking capability, while the DPLL is activated under fault conditions to ensure robust synchronization and effective harmonic suppression. In parallel, the DVR is also controlled in response to the real-time grid classification, injecting compensating voltage only when disturbances are detected, thus avoiding unnecessary intervention during healthy grid states and minimizing stress on DVR components. This unified, adaptive framework enhances overall system performance by ensuring accurate synchronization, improved power quality at both the point of common coupling and the load, and reduced hardware and control complexity.

The rest of this paper is organized as follows: i) Section 2 details the proposed methodology, including the mathematical implementation of the DVR, the fuzzy inference system (FIS) for adaptive PLL switching, and the phase-wise voltage monitoring logic; ii) Section 3 describes the complete system architecture and the implementation in MATLAB Simulink of the 100-kW grid-tied PV system, its control framework, and the integrated operation of DVR with adaptive PLL selection; iii) Section 4 presents simulation results and discussion for symmetrical and asymmetrical sag/swell conditions across three control cases, DPLL-only, DVR with DPLL, and the proposed DVR with FIS-based adaptive PLL switching—evaluating voltage restoration, harmonic performance, and recovery time; and iv) Section 5 concludes the work with key findings and outlines directions for future research.

2. METHODOLOGY

The mathematical formulations of the core subsystems constituting the proposed FIS-based DVR control strategy are detailed in this section.

2.1. Dynamic voltage restorer (DVR)

The DVR, a series voltage injection device, is used in this work to mitigate voltage fluctuations at the point of common coupling (PCC). In the proposed system, the DVR operates under a voltage injection strategy regulated by a robust sliding mode controller (SMC) implemented in the synchronous reference

frame (dq-frame). The DVR's primary objective is to ensure load-side voltage stability during both symmetrical and asymmetrical grid disturbances.

The measured three-phase grid voltages $V_{abc}(t)$ at the PCC are first converted into per-unit (p.u.) values using the base phase voltage, as expressed in (1).

$$V_{abc}^{pu}(t) = \frac{V_{abc}(t)}{V_{base}} \quad (1)$$

This normalization aligns the measured signals with the dq-frame reference values, where, V_{dref} is typically set to 1.0 or 1.13 p.u. and $V_{qref} = 0$.

$$\begin{bmatrix} V_d \\ V_q \\ V_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} cos\theta & cos\left(\theta - \frac{2\pi}{3}\right) & cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin\theta & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} V_a^{pu} \\ V_b^{pu} \\ V_c^{pu} \end{bmatrix} \quad (2)$$

The per-unit voltages are transformed into the synchronous reference frame using the Park transformation, as shown in (2) [33]. The transformation angle θ is derived from either the digital PLL (DPLL) or CTPLL, depending on the condition-based switching logic governed by the fuzzy inference system (FIS).

2.1.1. SMC-based DVR control

The SMC tracks the error between the reference and actual dq-frame voltages. The error and its derivative are defined in (3).

$$e_d(t) = V_d^{ref} - V_d \ , \dot{e}_d(t) = \frac{d}{dt} e_d(t) \quad (3)$$

Unlike traditional SMCs that use discontinuous sign functions, this work employs a saturation function to reduce chattering and improve convergence, as shown in the equation, which is known as the control law (4):

$$u(t) = k\ sat\big(s(t)\big) \quad (4)$$

where $s(t) = f\big(e_d(t), \dot{e}_d(t)\big)$.

This approach ensures a smooth transition of the control signal within bounded limits, making it well-suited for power electronic converters and enhancing system longevity and control precision. The final control signal is then transformed back to the ABC frame and applied through the DVR inverter to inject the appropriate compensating voltage at the PCC [34].

2.1.2. DVR sizing

The DVR's power rating and energy requirements are determined using (5) and (6):

$$S_{DVR} = \sqrt{3} * V_{inj,rms} * I_{load} \quad (5)$$

$$E_{DVR} = \int_{t1}^{t2} V_{inj}(t) * I_{load}(t)\, dt \quad (6)$$

where $V_{inj,rms} = V_{ref}(t) - V_{load}(t)$. These equations guide the design of DVR capacity to ensure effective compensation during grid disturbances.

2.2. Fuzzy logic-based adaptive PLL switching mechanism

To enhance synchronization during grid disturbances while ensuring control simplicity in normal conditions, an adaptive PLL switching strategy is implemented using a Mamdani-type fuzzy inference system (FIS). This mechanism dynamically selects between a conventional SRF-based PLL (CTPLL) and a digital PLL (DPLL) based on real-time fault monitoring.

2.2.1. Real-time fault detection logic

A three-phase voltage monitoring unit (Figure 1) computes RMS values of V_a, V_b, and V_c. Then compares with the threshold of ±10% of the nominal value, and each phase is assigned a fault status based on deviation thresholds: i) 0: no fault detected (voltage within nominal limits), ii) 0.5: likely fault or pre-fault

behavior (minor deviation), and iii) 1: Confirmed fault (significant voltage sag or swell. These discrete values allow the system to detect both normal and fault (symmetrical or asymmetrical faults, sag or Swell) effectively.

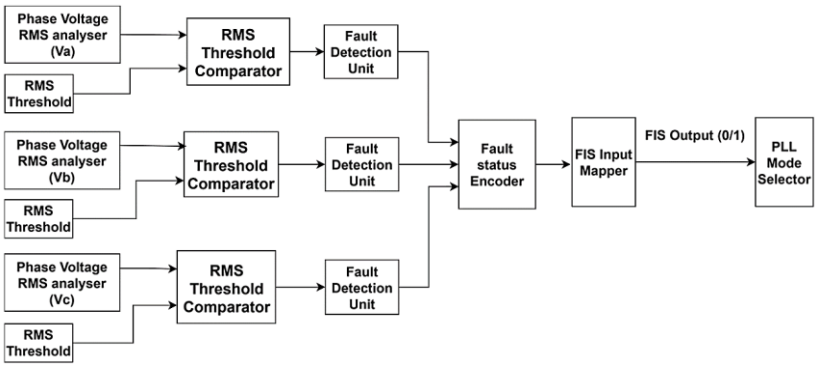


Figure 1. Phase-wise RMS voltage monitoring and fuzzy logic-based adaptive PLL switching architecture

2.2.2. Switching mechanism

The FIS (Figure 2) accepts three inputs (phase fault statuses) and produces two outputs: CTPLL_mode and DPLL_mode. Each input uses three trapezoidal membership functions (Figure 3(a)), while outputs follow a three-level fuzzy structure: off, partial, and on (Figure 3(b)). The FIS rule base interprets all possible combinations of the three input phases (3^3 = 27 combinations). However, for system simplicity and relevance, only selected meaningful rules are implemented, such as:

- No Fault (0): CTPLL remains fully ON, DPLL remains fully OFF;
- Fault (1): CTPLL ramps down to OFF, DPLL ramps up to ON; and
- Likely Fault (0.5): Both PLLs are partially active for a short transition period. CTPLL starts ramping down while DPLL starts ramping up.

This rule-based logic ensures that the DPLL is activated only when necessary, optimizing computational efficiency. The proposed control framework has been designed with minimal computational overhead. DVR sizing is based on standard per-unit voltage injection calculations, avoiding iterative optimization routines. The phase-wise monitoring logic and FIS-based switching require only simple RMS voltage evaluations and trapezoidal membership evaluations per control cycle, which are computationally light for modern DSP or FPGA controllers. As such, the adaptive PLL switching and DVR operation can be executed in real time without increasing hardware requirements or compromising system response speed.

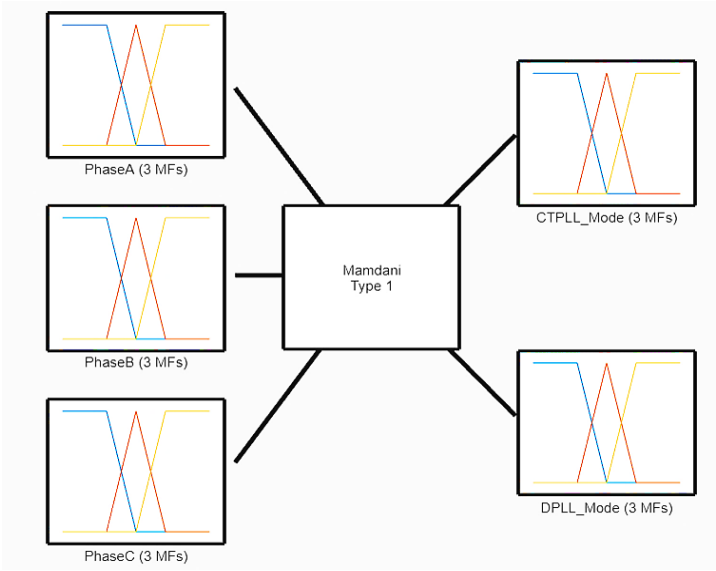
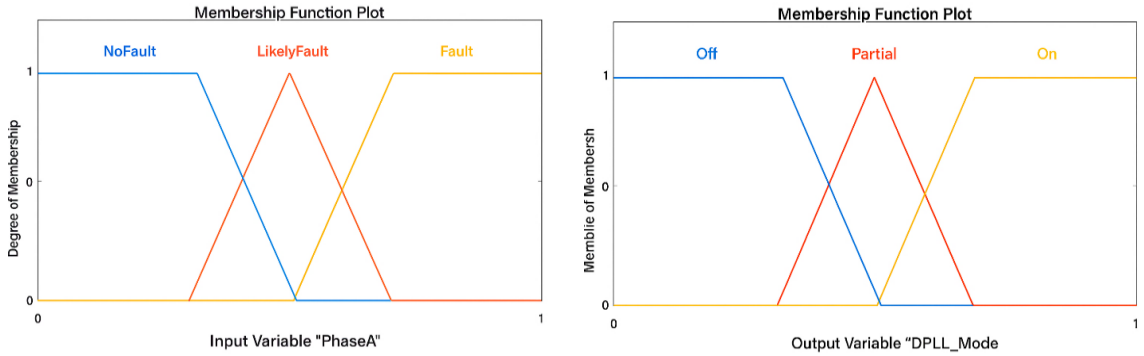


Figure 2. Fuzzy inference system



(a) (b)

Figure 3. Membership functions plot: (a) input variable "PhaseA" and (b) output variable "DPLL_Mode"

2.3. Overview of phase-locked loop (PLL) structures

This work employs a dual-PLL synchronization approach consisting of a conventional synchronous reference frame phase-locked loop (CTPLL) and a digital phase-locked loop (DPLL), whose operations are adaptively controlled based on real-time grid conditions. The complete design, mathematical formulation, and implementation details of both CTPLL and DPLL have been extensively discussed and validated in our earlier work [25]. Therefore, only a concise overview is presented here to contextualize their role in the proposed hybrid control strategy. The CTPLL, grounded in the synchronous reference frame theory, uses Park transformation for phase detection and operates reliably under balanced, steady-state grid conditions. Its advantages include low computational complexity and fast steady-state response, making it suitable for deployment during normal grid operation to conserve resources and maintain system stability.

The DPLL, in contrast, is developed using a discrete-time backward Euler approximation technique to enhance synchronization accuracy under distorted and faulted grid scenarios. As demonstrated in [25], this structure provides superior dynamic performance, reduces harmonic distortion significantly, and improves system stability without increasing control complexity. The DPLL achieved notable reductions in THD and inter-harmonic effects, along with a near-unity power factor, validating its robustness and computational efficiency.

In the current system, these two PLLs are not operated concurrently. Instead, their engagement is determined by a phase-wise monitoring logic and fuzzy inference system that assesses the voltage condition of each phase. CTPLL is engaged under nominal grid conditions, while the DPLL is selectively activated when fault signatures are detected. This adaptive configuration ensures precise synchronization, enhanced harmonic resilience, and optimal control performance across varying grid disturbances, without altering the core operation of either PLL.

3. SYSTEM DESCRIPTION

The proposed control architecture builds upon the validated 100 kW grid-tied solar PV system presented in [25], which includes a single-diode model-based PV array, a boost converter for DC-link regulation, a voltage-source inverter (VSI) with an LC filter, and dual synchronization schemes using CTPLL and DPLL. That foundational system operating under a voltage-controlled inverter strategy demonstrated reliable phase tracking and power quality under varying irradiance, load, and fault conditions.

In this extended work, a DVR with a 15 kVA power rating is integrated in series between the utility grid and the point of common coupling (PCC) to address voltage disturbances. Additionally, an adaptive synchronization layer is introduced to enable real-time PLL switching through a fuzzy inference system (FIS), as shown in Figure 4, significantly enhancing response flexibility without increasing system complexity. A phase-wise monitoring unit analyses RMS grid voltage over time, discarding initial transients and classifying each phase as healthy (0), pre-fault (0.5), or faulted (1).

The "pre-fault" state (0.5) enables a smooth ramped transition, where the outgoing PLL gradually disengages while the incoming PLL gradually takes over. This avoids abrupt control mode changes and minimizes transient disturbances during switching.

These severity indices are fed into a Mamdani-type FIS, which governs the PLL selection logic—activating CTPLL during stable conditions, DPLL when disturbances are detected, and partial overlap in pre-fault conditions to ensure a seamless switchover.

The selected PLL governs the generation of Vabc reference signals used for PWM-based VSI control. The DVR operates in injection mode, supplying corrective voltages to maintain stable load and PCC voltage during grid faults, while remaining inactive during healthy grid operation. This entire setup is modeled and simulated using MATLAB/Simulink as shown in Figure 5 (see Appendix).

System performance is tested under multiple grid fault scenarios, including balanced and unbalanced voltage sags and swells introduced at specific time instances. The proposed FIS-driven PLL adaptation is evaluated based on its ability to restore the PCC voltage, reduce total harmonic distortion (THD), suppress inter-harmonic components, and maintain a unity power factor at the load side.

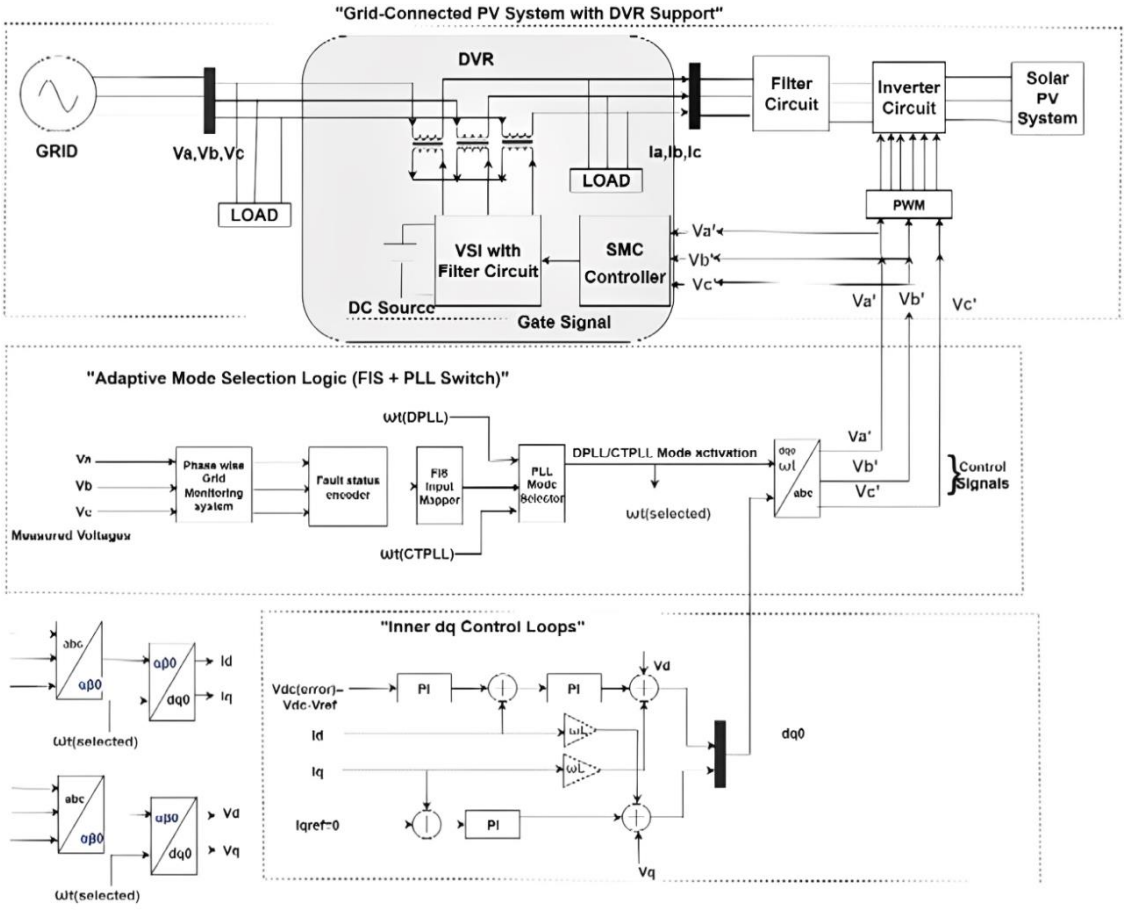


Figure 4. Complete system architecture of grid-tied PV system with DVR and FIS-based adaptive PLL switching

4. SIMULATION RESULTS AND DISCUSSION: VOLTAGE REGULATION UNDER GRID FAULTS

This section presents the simulation results to assess the voltage regulation performance of the proposed system under two grid disturbance conditions, symmetrical swell and asymmetrical sag. These two cases are selected as they represent the most balanced and most critical scenarios, respectively. Simulations are carried out across three progressive configurations: i) Case 1: DPLL-based synchronization (No DVR), ii) Case 2: DPLL with DVR compensation, and iii) Case 3: DPLL + DVR with FIS-based adaptive PLL switching.

4.1. Case 1: DPLL-based synchronization without DVR

Figure 6 illustrates the system performance when only the digital phase-locked loop (DPLL) is used for grid synchronization, without any DVR-based voltage compensation.

– Figure 6(a) presents the grid and PCC voltage waveforms under two grid fault conditions: a symmetrical swell (20% increase in all three phases) and an asymmetrical sag (20% drop in Phase A only). In both cases, the disturbances at the grid level are directly reflected at the PCC, leading to elevated voltages during swell and imbalanced voltages during sag.

- Figure 6(b) shows the voltage and current responses of a nonlinear load under the same fault conditions. The voltage swells cause overvoltage stress at the load terminals, while the asymmetrical sag leads to distorted voltage waveforms and imbalance in current magnitudes across phases.
- Figure 6(c) displays the response of a regular RL load. Similar to the nonlinear case, the voltage and current waveforms deviate from their ideal sinusoidal shape. Under asymmetrical sag, unbalanced current flow is observed due to phase voltage disparity, and under symmetrical swell, overvoltage affects current amplitude uniformly.

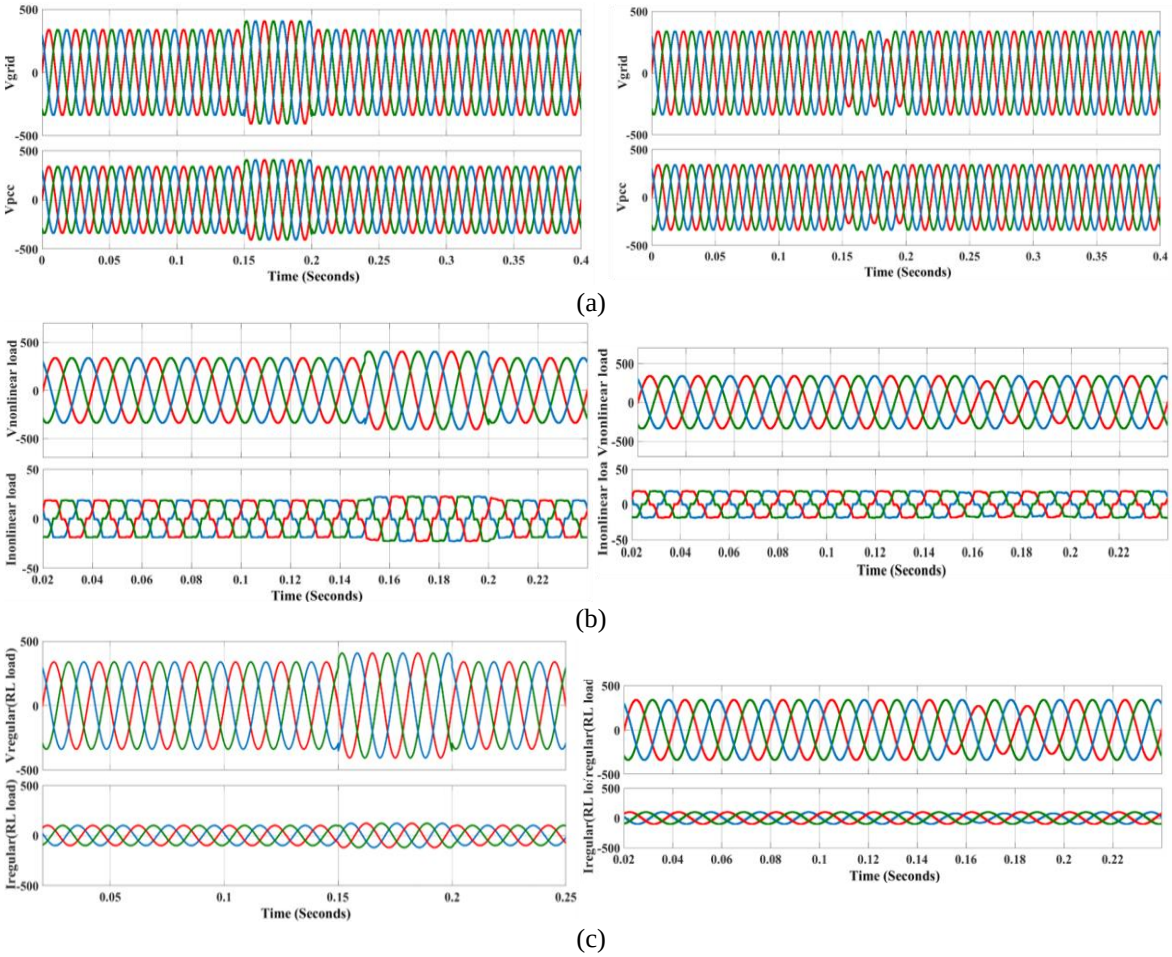


Figure 6. Voltage (V) and current (A) waveforms under symmetrical swell and asymmetrical sag conditions without DVR compensation: (a) grid and PCC voltages, (b) nonlinear load voltages and currents, and (c) RL load voltages and currents

4.1.1. Impact on load current and power quality

The distortion in voltage directly affects the load current profiles. Nonlinear load currents show an increase in harmonic content and unbalanced behavior under asymmetrical sag, as illustrated in Figures 5(b) and 5(c). RL load current also deviates from its expected sinusoidal profile due to the voltage asymmetry. This not only reduces power transfer efficiency but also creates stress in power electronic devices.

These results confirm that while DPLL maintains synchronization, it alone cannot regulate voltage anomalies at the PCC or prevent their impact on downstream loads. Both load types exhibit voltage distortion and current imbalance under fault conditions, underlining the need for dedicated voltage compensation support.

4.2. Case 2: DVR compensation with DPLL-based synchronization

Figure 7 illustrates the system response under the same grid fault conditions—symmetrical swell and asymmetrical sag—but now with a DVR integrated, operating alongside the DPLL-based synchronization strategy.

i) Figure 7(a): Grid, PCC, and injected voltages

Under symmetrical swell, the DVR operates in voltage injection mode, introducing a compensating negative voltage (V_injected) precisely during the overvoltage interval. As a result, the PCC voltage is regulated close to its nominal magnitude, even though the grid remains in an overvoltage state. During asymmetrical sag, the DVR selectively injects voltage in the affected phase (Phase A), effectively restoring PCC voltage symmetry. The waveform shows timely and phase-specific V_injected action, ensuring that the voltage imbalance does not propagate downstream.

ii) Figure 7(b): Nonlinear load voltage and current response

For both swell and sag conditions, the nonlinear load voltages maintain their sinusoidal shape and nominal RMS value. The current waveforms exhibit minimal distortion compared to the unregulated case, reflecting reduced harmonic impact due to stabilized input voltages at the PCC. This demonstrates that the DVR, even with just DPLL control, significantly enhances voltage quality for nonlinear loads.

iii) Figure 7(c): RL load voltage and current response

RL load voltages remain uniform and undistorted, closely following the regulated PCC waveform. Load currents recover their sinusoidal nature and phase symmetry, indicating that the power flow balance is restored. Compared to the previous case (Figure 6), this highlights the voltage stabilization capability of the DVR across both linear and nonlinear load types. While the DPLL-based synchronization coupled with DVR compensation improves PCC voltage regulation and restores waveform symmetry under both symmetrical swell and asymmetrical sag conditions, certain limitations persist. Notably, the DVR continues to inject compensating voltage—up to 50 V—even during normal grid conditions, which is undesirable. This unnecessary injection can disrupt power flow, induce losses, and accelerate wear of DVR components. Hence, a more intelligent control mechanism is needed—one that discriminates between fault and healthy states in real time. This sets the stage for the FIS-based adaptive switching strategy, discussed next, which enhances selectivity and optimizes DVR operation based on actual grid conditions.

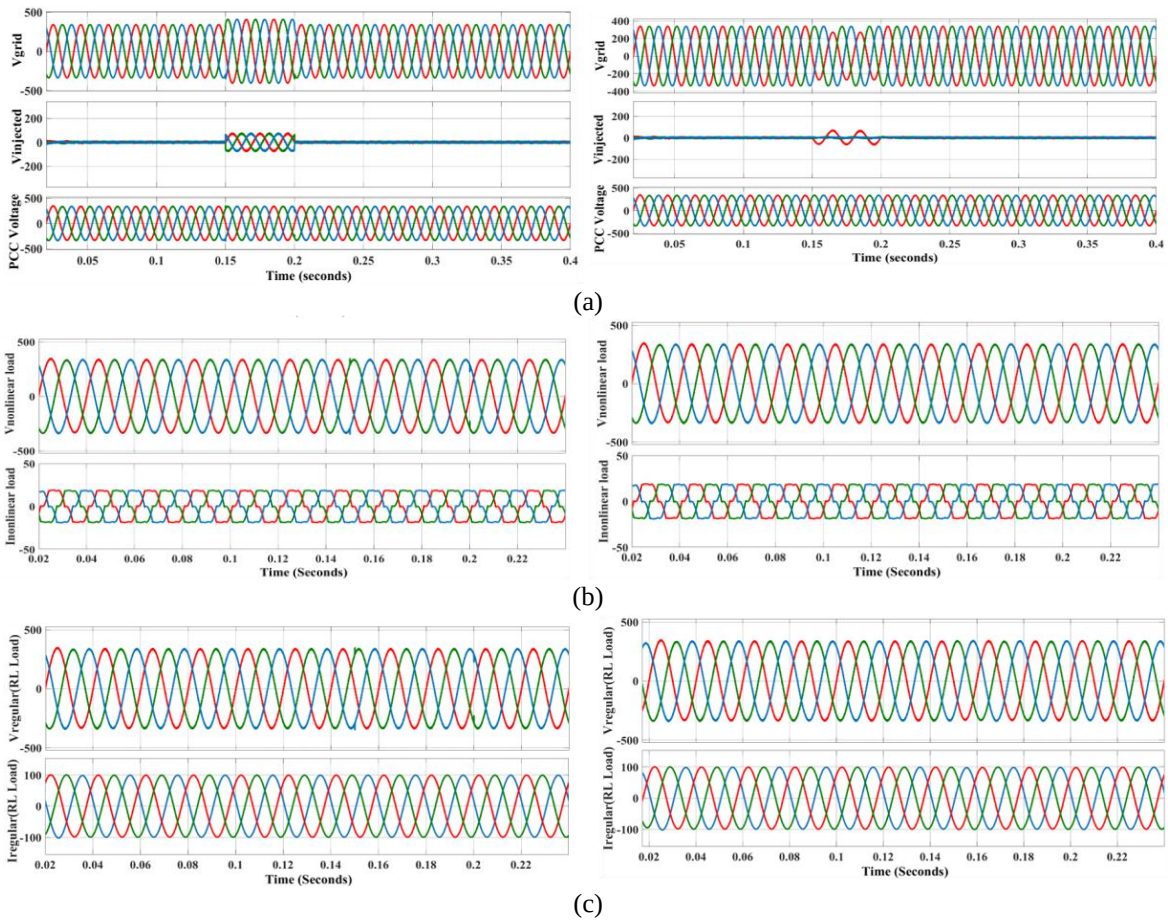


Figure 7. Voltage (V) and current (A) waveforms under symmetrical swell and asymmetrical sag conditions with DVR Compensation: (a) grid and PCC voltages, (b) nonlinear load voltages and currents, and (c) RL load voltages and currents

4.3. Case 3: Performance with FIS-based adaptive PLL and DVR

Figure 8 illustrates the voltage and current response of the system under symmetrical swell and asymmetrical sag scenarios when the proposed fuzzy logic-based adaptive PLL mechanism is integrated with DVR control. Compared to the DVR-only case, this configuration demonstrates marked improvement in voltage regulation precision, current waveform balance, and system responsiveness. Notably, the DVR injection is now limited to ~5–6 V during steady-state, avoiding unnecessary action during healthy grid conditions. This directly addresses the overcompensation observed earlier, preserving grid stability and reducing DVR switching effort and component stress. All three phases at the PCC exhibit better sinusoidal symmetry, and both nonlinear and RL load currents show high waveform quality with minimal distortion, even under unbalanced conditions. The FIS effectively enables fast PLL switching, ensuring that DPLL is invoked only during actual faults, allowing CTPLL to handle nominal conditions efficiently.

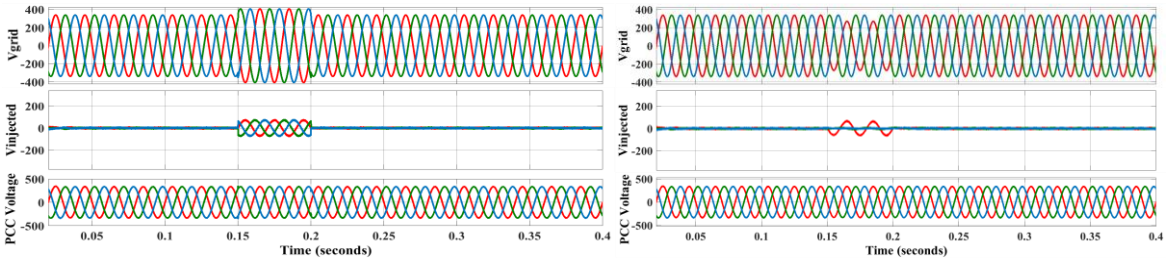


Figure 8. Voltage (V) and current (A) waveforms under symmetrical swell and asymmetrical sag conditions, FIS-based adaptive PLL and DVR: grid and PCC voltages

Smaller deviations indicate higher restoration accuracy and better voltage profile regulation. For instance, parameters such as VPCC and VRL load approaching 338.7 V closely reflect ideal steady-state operation. Similarly, inverter and PCC current values converging towards their nominal references IPCC =204.6A, IRL load=100.3 A confirm improved current symmetry and reduced distortion. The recovery time row provides the measured delay from fault inception to full voltage restoration; lower values represent faster compensation response. This combined comparison of magnitude accuracy and recovery speed offers a quantitative basis for assessing and ranking the three control strategies. A summary of voltage restoration accuracy and recovery time for each case is presented in Table 1. The “Ideal Values” column lists the nominal reference values for each parameter under perfect operating conditions, serving as the benchmark for comparison. All measured voltages and currents from the three configurations, DPLL-only, DVR + DPLL, and DVR + DPLL + FIS are evaluated against these nominal values.

4.4. Total harmonic distortion (THD) analysis

To assess the impact of DVR and adaptive PLL switching on harmonic performance, a detailed total harmonic distortion (THD) analysis is carried out across three configurations:

i) Base system: DPLL only (no DVR, no FIS)
ii) Enhanced system: DPLL + DVR (without FIS)
iii) Proposed adaptive system: DVR with FIS-based CTPLL/DPLL switching

The THD is evaluated for inverter current, nonlinear load current, and PCC current under symmetrical swell and asymmetrical sag conditions. The analysis uses a 2-cycle window during fault intervals, complemented by 10-cycle windows before and after the disturbance to observe recovery behavior. Observations:

i) Case 1: The DPLL-only system exhibits significant THD in nonlinear load current and PCC current, especially during grid voltage disturbances. This is due to the inability to correct the grid voltage and phase, leading to distortion propagation from the inverter side.
ii) Case 2: Introducing a DVR with DPLL control reduces THD by injecting compensating voltage during disturbance periods. However, during nominal conditions, residual DVR activity and DPLL estimation delays cause minor harmonic injection, slightly affecting inverter-side current quality.
iii) Case 3: The DVR + FIS adaptive system delivers the best performance across all metrics. The FIS selectively activates DPLL only during disturbed intervals and switches back to CTPLL during normal operation. This strategy minimizes unnecessary switching and harmonic distortion during steady-state, while still ensuring robust compensation during faults.

Table 1. Comparative analysis of voltage (V), current (A), and recovery time (msec) performance under grid fault conditions

	Parameters	Vnon-linear	Inon-linear	Vpcc	Ipcc	V inverter	I inverter	V grid	I grid	V injected	$V_{RL\ load}$	$I_{RL\ load}$	Recovery time
20%	DPLL	406.4	22.14	406.6	173.2	472.5	169.7	406.6	40.85	nil	406	120.2	NA
Symmetric	DPLL+DVR	332.6	18.43	331.7	204.7	474.2	197.9	406.6	86.85	-70.8	336.9	99.07	0.045 msec
Swell	DPLL+DVR+FIS	336.3	18.5	334.6	202.1	455.7	192.6	406.6	85.09	-71.99	336.3	99.07	0.035 msec
20%	DPLL	406.4	20.28	406.4	186.2	485.9	175.9	406.6	45.71	nil	406	120.2	NA
Asymmetric	DPLL+DVR	338.7	18.34	333.5	207	464	190.9	406.6	82.43	-73.12	339.1	99.39	0.053 msec
Sag	DPLL+DVR + FIS	338.2	18.49	335	205	452.3	192	406.6	82.23	-73.22	335.3	99.95	0.028 msec
20%	DPLL	271	14.99	271	274.2	455.9	240.7	271	159.9		271	80.22	NA
Symmetric	DPLL+DVR	336.3	18.51	339.06	205.4	474.5	198.8	271	78.25	66.16	336.4	99.07	0.05 msec
Sag	DPLL+DVR +FIS	336.5	18.32	335.9	201.5	469.2	198.5	271	91.96	60.9	334.8	99.09	0.03 msec
20%	DPLL	271	16.72	271	218.1	454	208.4	271	103.4	nil	271	80.22	nil
Asymmetric	DPLL+DVR	335.4	18.49	336.2	203.1	470.1	197.8	271	80.86	68.01	338.6	98.2	nil
Sag	DPLL+DVR+FIS	335.9	18.51	335.7	203.3	467.5	199.6	271	74.69	69.05	336.4	99.03	no delay
	Ideal Values	338.7	18.65	338.7	204.6	474	190.5	338.8	81.92	nil	338.8	100.3	-

4.4.1. Harmonic analysis under asymmetric swell and sag faults

Table 2 presents the harmonic performance of the system under 20% symmetric swell and sag conditions, including DC components, fundamental RMS/peak values, and THD for inverter current, nonlinear load current, and PCC current. The results compare three control configurations: i) Base System: DPLL only (no DVR, no FIS); ii) Enhanced system: DPLL + DVR (without FIS); and iii) Proposed adaptive system: DVR with FIS-based CTPLL/DPLL switching.

Table 2. The performance of harmonic analysis of inverter, PCC, and load currents under symmetrical faults (swell and sag)

	Harmonic analysis during symmetric swell and sag faults												
	Parameters	DC component			Fundamental(peak)			Fundamental(rms)			%THD		
Fault	current component	Case 1	Case 2	Case 3	Case 1	Case 2	Case 3	Case 1	Case 2	Case 3	Case 1	Case 2	Case 3
20%	Iinverter	0.06732	0.7079	0.5658	162.2	195.6	196.1	114.7	138.3	138.6	3.91	1.82	1.71
Symmetric	Inonlinear load	0.001245	0.0007	0.0026	24.12	19.87	19.85	17.05	14.05	14.03	14.42	14.42	14.41
Swell	Ipcc	0.003792	0.7464	0.5811	164.4	197.5	197.8	116.3	139.7	139.9	5.53	4.23	3.59
20%	Iinverter	3.659	0.7302	0.5658	245.9	196.3	196.1	173.9	138.8	138.6	3.02	1.78	1.71
Symmetric	Inonlinear load	0.001226	0.0011	0.0026	16.06	19.85	19.85	11.36	14.03	14.03	14.41	14.41	14.41
Sag	Ipcc	3.62	0.722	0.5811	247.6	198.3	197.8	175.1	140.2	139.9	3.8	2.97	2.5

The proposed FIS-based SMC DVR (Case 3) demonstrates significant THD reduction compared to both the uncompensated system (Case 1) and the conventional DVR (Case 2). Under 20% symmetric swell, inverter current THD decreased by 56.26% relative to Case 1 and by 6.04% over Case 2, while PCC current THD improved by 35.08% and 15.14%, respectively. Similar trends were observed for 20% symmetric sag, with inverter current THD reductions of 43.38% and 3.93%, and PCC current reductions of 35.57% and 15.82%. These results confirm the proposed controller's ability to deliver substantial additional harmonic mitigation beyond that of a standard DVR.

Fundamental RMS and peak current values are maintained close to nominal in all FIS-assisted cases, ensuring voltage stability while minimizing unnecessary DVR activity. This confirms that adaptive PLL switching improves harmonic suppression and voltage regulation simultaneously. Figure 9 illustrates the THD reduction for all cases, showing that the proposed FIS-based control outperforms both DPLL-only and DVR-only systems across all measured points.

4.4.2. Harmonic analysis under asymmetric swell and sag faults

Table 3 summarizes the absolute THD values under asymmetric swell and sag conditions for each phase. For a 20% asymmetric swell (Phase A), the proposed FIS-based SMC DVR (Case 3) reduced inverter current THD by 26.73% compared to the uncompensated system (Case 1) and by 13.42% over the conventional DVR (Case 2). PCC current THD improved by 25.99% and 11.37%, respectively.

In the 20% asymmetric sag scenario, inverter current THD reductions were 9.49% and 14.77% compared to Cases 1 and 2, while PCC current THD decreased by 7.56% and 11.15%, respectively. Nonlinear load current THD changes were minimal across cases, indicating that the primary benefit of the proposed controller is in mitigating grid-side and inverter harmonics under unbalanced fault conditions.

Across Phases B and C, the proposed FIS-based SMC DVR consistently reduced inverter and PCC current THD compared to both the uncompensated system (Case 1) and the conventional DVR (Case 2).

Peak improvements were observed for inverter THD in Phase B asymmetric swell (29.09% vs Case1, 14.80% vs Case2) and PCC THD in Phase B asymmetric swell (16.43% vs C1). Minor changes were noted for nonlinear load THD, with slight increases in certain sag conditions, indicating that the primary harmonic mitigation effect is concentrated on the inverter and PCC currents, which directly influence grid power quality. Figure 10 illustrates these reductions for inverter, PCC, and nonlinear load currents.

These findings, combined with the results from Section 4.3, confirm that the proposed FIS-based SMC DVR not only improves voltage stability and eliminates unwanted DVR injection but also ensures faster recovery during fault events. The THD analysis in Section 4.4 further validates its effectiveness in suppressing inverter and PCC harmonics under asymmetric faults, achieving substantial reductions compared to both DPLL-only and DVR-only configurations. This dual benefit—enhanced voltage regulation and superior harmonic mitigation—is enabled by the adaptive PLL switching with FIS, which provides precise fault detection, optimal PLL selection, and timely DVR voltage injection.

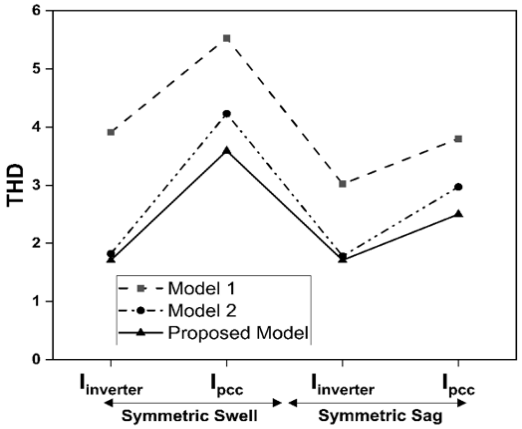


Figure 9. THD reduction during symmetric swell/sag fault conditions

Table 3. Harmonic Analysis of Inverter, PCC, and load currents under asymmetrical faults (swell and sag)

Fault	Parameters current component	DC component Case 1	DC component Case 2	DC component Case 3	Fundamental(peak) Case 1	Fundamental(peak) Case 2	Fundamental(peak) Case 3	Fundamental(rms) Case 1	Fundamental(rms) Case 2	Fundamental(rms) Case 3	%THD Case 1	%THD Case 2	%THD Case 3
Harmonic analysis during Asymmetric Swell and Sag faults (Phase A)													
20% asymmetric Swell	Iinverter	1.215	0.3292	0.471	186.8	205.3	202.7	132.1	145.2	143.3	4.49	3.8	3.29
	Inonlinear load	0.000168	0.0035	0.0187	22.68	19.87	19.87	16.04	14.05	14.05	12.79	14.44	14.4
	Ipcc	1.208	0.2963	0.4437	189.1	207.4	204.7	133.7	146.7	144.8	5.58	4.66	4.13
20% asymmetric Sag	Iinverter	1.512	0.4571	0.2864	198.8	185.9	189.3	140.6	131.4	133.8	4.53	4.81	4.1
	Inonlinear load	0.000193	0.0633	0.0802	17.41	19.85	19.83	12.31	14.04	14.02	17.45	14.48	14.46
	Ipcc	1.462	0.4546	0.2034	200.3	187.6	190.7	141.6	132.7	134.9	5.43	5.65	5.02
Harmonic analysis during Asymmetric Swell and Sag faults (Phase B)													
20% asymmetric Swell	Iinverter	1.117	0.3777	0.3878	176.4	189.6	189.3	124.7	134.1	133.8	4.71	3.92	3.34
	Inonlinear load	0.000277	0.0002	0.011	21.05	19.87	19.87	14.88	14.05	14.05	15.11	14.44	14.43
	Ipcc	1.109	0.4103	0.3801	177.9	191.9	191.4	125.8	135.7	135.3	5.66	4.73	4.26
20% asymmetric Sag	Iinverter	1.094	0.7233	1.081	215.1	204	203.2	152.1	144.3	143.7	4.16	4.36	3.66
	Inonlinear load	0.000224	0.0397	0.0512	19.3	19.86	19.87	13.65	14.05	14.05	13.4	14.43	14.37
	Ipcc	1.102	0.7148	1.158	217.4	205.6	204.8	153.7	145.4	144.8	5.24	5.24	4.68
Harmonic analysis during Asymmetric Swell and Sag faults (Phase C)													
20% asymmetric Swell	Iinverter	0.09794	0.0485	0.0831	179.9	193.5	195.4	127.2	136.8	138.2	4.11	4.05	3.37
	Inonlinear load	0.000447	0.0037	0.0077	20.63	19.86	19.87	14.59	14.05	14.05	16.13	14.42	14.43
	Ipcc	0.09932	0.114	0.0636	182.1	194.9	196.8	128.8	137.8	139.1	5.05	4.7	4.28
20% asymmetric Sag	Iinverter	0.3759	0.2661	1.367	209.8	198.8	196.9	148.4	140.6	139.2	4.23	4.54	3.82
	Inonlinear load	0.000418	0.0235	0.029	19.58	19.84	19.83	13.85	14.03	14.03	13.56	14.44	14.45
	Ipcc	0.3601	0.2602	1.361	211.7	201.3	199.2	149.7	142.3	140.8	5.32	5.27	4.72

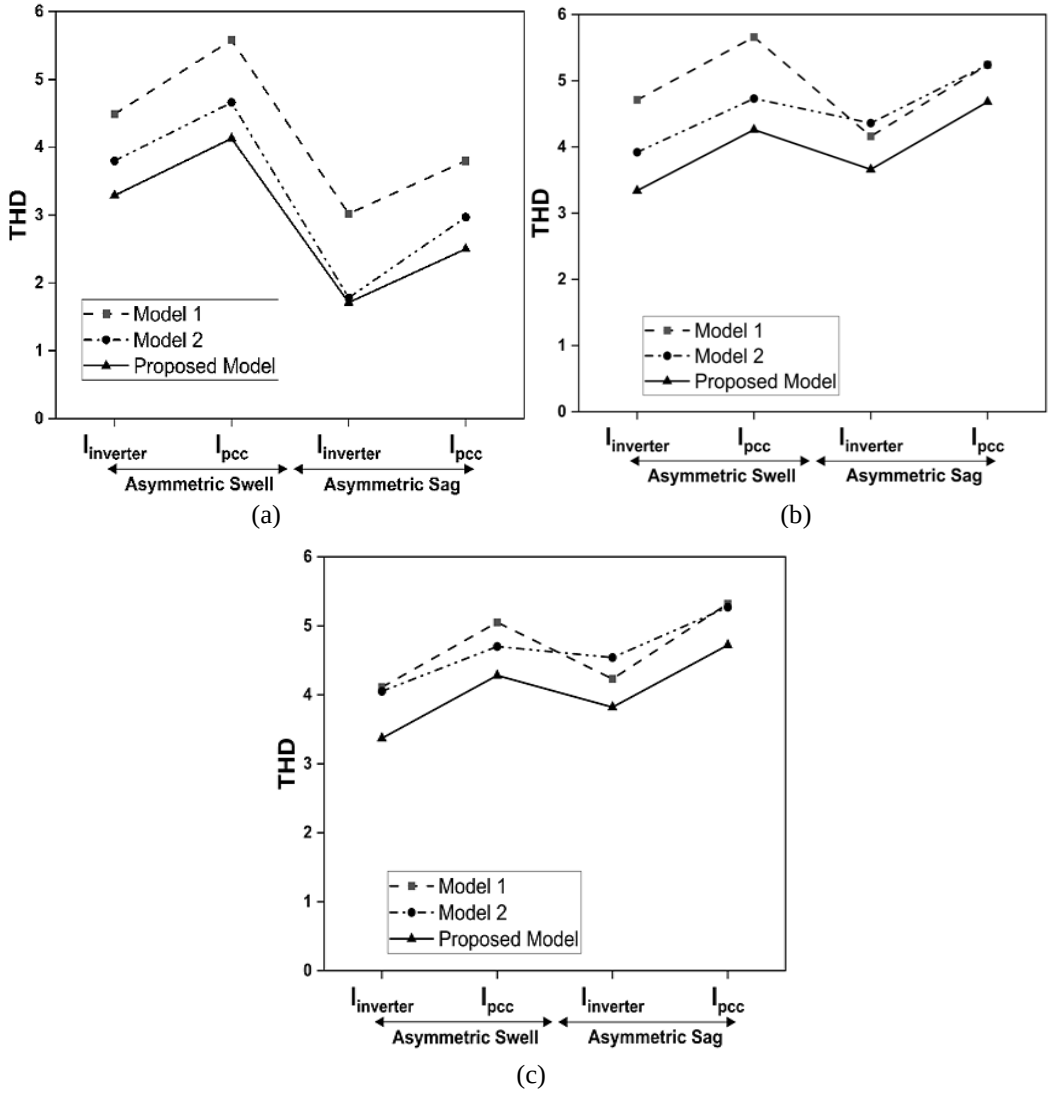


Figure 10. THD reduction during Asymmetric swell/sag fault conditions across each phase: (a) phase a, (b) phase b, and (c) phase c

5. COMPARATIVE ANALYSIS

The comparative table highlights key performance and implementation features of various phase-locked loop (PLL)-based control strategies from recent literature alongside the proposed SRF-DPLL integrated with fuzzy logic-based DVR, as shown in Table 4 (see Appendix) [16], [18], [22], [35]-[39]. Parameters such as THD reduction under fault conditions, voltage sag/swell compensation, stability analysis using Bode plots, and handling of nonlinear loads are evaluated. The proposed system demonstrates superior performance in power quality improvement, especially under distorted grid and unbalanced fault conditions, with low computational complexity and moderate implementation effort due to its digital nature and adaptive FIS switching. Each reference represents a relevant contribution used as a benchmark in developing and validating the proposed approach.

6. CONCLUSION

This work presented a fuzzy logic-based adaptive control strategy for a DVR-assisted 100 kW grid-tied PV system, enabling dynamic switching between CTPLL and DPLL based on real-time, phase-wise fault detection. The proposed controller was validated under symmetrical and asymmetrical 20% sag and swell conditions, demonstrating improvements in both voltage regulation and harmonic suppression. Compared to the uncompensated system (Case 1), the proposed SRF-DPLL + FIS-DVR achieved up to 56.26% THD reduction in inverter current and 35% at the PCC. When compared to a conventional DVR using DPLL only

(Case 2), the method achieved up to 15.82% THD reduction at the PCC and ~15% in inverter current, with consistent gains across all tested fault scenarios. Recovery times improved by 20–25%, and unnecessary DVR injection was reduced from ~50 V to ~5–6 V during nominal conditions, maintaining a near-unity power factor (~0.999). The integration of adaptive PLL switching with targeted DVR activation offers a compact, hardware-efficient solution for harmonic mitigation, voltage stability, and fault resilience, without increasing control complexity. Future work will extend this framework to include voltage flicker analysis, frequency variation studies, and hardware-in-the-loop (HIL) testing for real-time validation.

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C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the report in this paper.

DATA AVAILABILITY

The Simulink models (including encapsulated subsystems) and controller files used in this study are available from the corresponding author upon reasonable request.

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APPENDIX

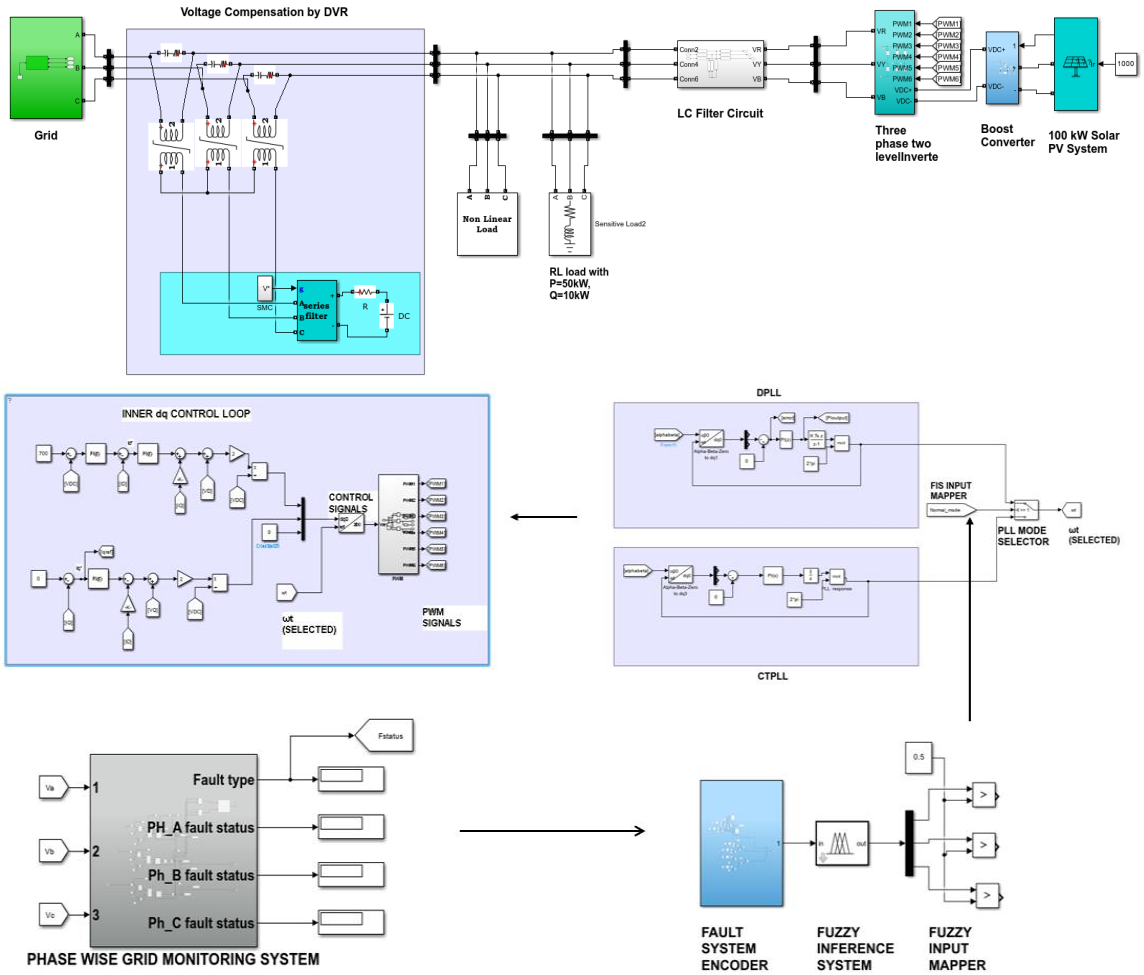

Figure 5. Complete system setup in MATLAB/Simulink for grid-tied PV system with DVR and FIS-based adaptive PLL switching

Table 4. Comparative analysis of the proposed FIS-based DVR with the DPLL system with the existing methods

Parameter	[35]	[36]	[37]	[38]	[16]	[18]	[22]	[39]	Proposed SRF-DPLL + FIS-DVR
THD Reduction (Under Faults)	Not Evaluated	Not Evaluated	Theoretical Only	Before: ~16%, After: ~12.5%	Sag: 29% → 3.5%, Swell: 23% → 3.4%	Before: 1.29%, After: 0.49%	Not Mentioned	Before: 16.42%, After: 12.52%	THD reduced up to 56.26% compared to the uncompensated system & by 15.82% over conventional DVR, with consistent improvement across symmetric & asymmetric sag/swell
Balanced & Unbalanced Grid Analysis	Balanced Only	Balanced Grid Analysis	Not Applicable	Unbalanced Only	Unbalanced Grid	Unbalanced Only	Not Evaluated	Line to Line Fault	Balanced & unbalanced
Nonlinear Load Handling	Not Analyzed	Not Evaluated	Not Applicable	Evaluated	Evaluated	Evaluated	Not Analyzed	Not Analyzed	Evaluated with RL & Nonlinear Load

Table 4. Comparative analysis of the proposed FIS-based DVR with the DPLL system with the existing methods (continued)

Parameter	[35]	[36]	[37]	[38]	[16]	[18]	[22]	[39	Proposed SRF-DPLL + FIS-DVR
Voltage Sag & Swell Compensation	Evaluated	Evaluated	Not Applicable	Evaluated	Evaluated	Not Mentioned	Evaluated	Not Analyzed	Symmetrical and Asymmetrical Sag/Swell (±20%) covered
Stability Analysis (Bode Plot)	Not Mentioned	Not Mentioned	Basic Bode Theory	Robust PLL stability	Stable but degraded under fault	Bode confirms improvement	Digital PLL stability	Stable (Numerical)	Bode shows robust stability of DPLL vs CTPLL
Computational Complexity	Moderate	Moderate	Low	Moderate	Moderate	Moderate	Low	High - FO-SMC + PSO	Low – Simple conventional SRF-PLL is upgraded to SRF-DPLL
Implementation Complexity	High - transformer less inverter design	Moderate - Structural focus	Low - Academic explanation	Moderate - Modified SOGI-PLL	Moderate - PLL shift-based	Low to Moderate	Low - All-digital hardware	High - Complex control logic	Moderate - FIS + mode switching logic

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