International Journal of Power Electronics and Drive System (IJPEDS)
Vol. 17, No. 1, March 2026, pp. 553∼571
ISSN: 2088-8694, DOI: 10.11591/ijpeds.v17.i1.pp553-571

High voltage asymmetric converter for electrostatic particle accelerators

Diego Alberto Fanego[1], Orlando Silvio Sandini[1], Hernán Emilio Tacca[1], Andrés Juan Kreiner[2]
[1]Universidad de Buenos Aires, Facultad de Ingeniería, Laboratorio de Control de Accionamientos, Tracción y Potencia (LABCATYP), Buenos Aires, Argentina
[2]Gerencia de Investigación y Aplicaciones, Comisión Nacional de Energía Atómica (CNEA), Buenos Aires, Argentina

Article Info

Article history:

Received Jun 30, 2025
Revised Dec 23, 2025
Accepted Jan 23, 2026

Keywords:

Asymmetric DC-DC converter topologies
Electrostatic particle accelerators
Forward-flyback converters
High voltage power supplies
Merged topology converters
Power electronics

ABSTRACT

This work presents several topologies of asymmetric high voltage converters for electrostatic particle accelerators. The options are compared on the basis of their transfer functions and the magnetic components required, and the most suitable for the intended purpose is selected. Simulations and measurement results of the prototype, which has symmetrical voltage output and soft switching in the main transistor, are presented. The prototype built features output voltages of 10 kV and -10 kV, the converter uses a single common command ground for the transistors simplifying its drivers, and also by means of the presented snubber circuit it recovers energy during soft switching.

Corresponding Author:

Diego Alberto Fanego
Universidad de Buenos Aires, Facultad de Ingeniería, Laboratorio de Control de Accionamientos Tracción y Potencia (LABCATYP)
Av. Paseo Colón 850 (C1063ACV), Ciuda Autónoma de Buenos Aires, Argentina
Email: dfanego@fi.uba.ar

1. INTRODUCTION

Particle accelerators are machines that use electromagnetic fields to deliver kinetic energy to ions or electrons. Beams of these accelerated charged particles, can be used to interact with different materials, study their properties and produce modifications in a wide variety of physical and biological systems. The energy level that a particle accelerator can reach ranges from kiloelectronvolt to teraelectronvolt. The spectrum of applications of these machines is extremely wide, including problem solving in medicine (radiotherapy and nuclear medicine), nuclear technology, microelectronics, materials science, environmental science and oil exploration, among many others [1].

Probably one of the most socially relevant applications is in the field of human health, in the fight against cancer. Ion accelerators are an important alternative among therapies for the control of malignant tumors, reaching results that have significant advantages over those obtained with conventional gamma ray radiotherapy. These ion and neutron tumor control procedures go by the generic name of hadrontherapy. The physical and radiobiological reasons for the superiority of hadrontherapy over conventional radiotherapy in the treatment of certain tumors are related to the radically different way in which charged hadrons deposit their energy in matter compared to gamma radiation. The penetration depth (range) of the charged hadron beams is well defined and can be controlled, since it is a function of the initial energy of the projectile, accelerating the particles by means of electric fields [2].

In nuclear physics and technology there are two major types of machines (and processes): nuclear reactors (based on nuclear fission) and particle accelerators (based on charged-particle induced reactions). In recent years these two aspects have begun to be unified in hybrid systems or accelerator driven systems (ADS), in which a beam of high-energy protons or deuterons incident on the right target produces very large neutron fluxes that are injected into a subcritical reactor. This principle is one of the most promising concepts for reducing the radiotoxicity of their waste [1]. The other very relevant application of neutron producing accelerators is Boron neutron capture therapy (BNCT).

Particle accelerators mainly involve two well differentiated processes, on the one hand the generation of particles and on the other their acceleration. For the latter, high electric fields are required, so the voltage power supplies must be capable of delivering continuous high voltages, with steps from tens to hundreds of kV, up to a total voltage that can reach MV [3]–[5]. As most electrical loads, the electrostatic particle accelerators have requirements of voltage (order 1 MV to 2.5 MV) and current supply (order 10 mA to 100 mA). There are intermediate voltage specifications for acceleration electrodes and for the total operation voltage which is the serial sum of all the intermediate supply voltages. Moreover, electrostatic lenses are included to avoid the dispersion of the particle beam (i.e. protons) due to repulsion between charged particles (this is called space-charge effect). These electrostatic lenses are powered by other ancillary high voltage power supplies and it is an usual requirement to use symmetrical power supplies to drive the electrostatic lenses. The topology here presented can be used to implement the main stage acceleration electrodes supplies and also the ancillary electrostatic lenses supplies (either single voltage or symmetrical ones).

This paper addresses high voltage generation sources consisting of a cascade converter with a secondary rectifier of the capacitive multiplier type [6]–[8]. In order to reduce the number of power devices required, and thus improve reliability, it is preferred to avoid symmetrical conversion topologies [9], [10]. There are many approaches to implement this type of power supplies, some simple but without isolation [6], [11], [12] others including isolation but operating in discontinuous mode (DCM) [13]–[15] which is not desired in this case, where the objective is to operate in continuous mode (CM) to achieve a better utilization factor of the semiconductors.

The high voltage power supplies presented here are primarily intended to be used in the electrostatic particle accelerators currently under development at the National Atomic Energy Commission (Comisión Nacional de Energía Atómica - C.N.E.A., Rep. Argentina) and eventually in equipment exported to other countries (i.e. South Korea) [1], [16]. Moreover, these high-voltage sources are also a fundamental part of the pulse generators for electroporation, since working with increasingly narrower pulses, on the order of tens of nanoseconds, the voltage of these pulses must be raised to tens of kV [17].

This work focuses on the study of asymmetric high voltage converters to be used mainly in electrostatic particle accelerators: i) In section 2 several converter topologies are presented, their main advantages and disadvantages are analyzed in order to select one and continue with the work; ii) Section 3 presents the simulations of the adopted converter; iii) Section 4 discusses the implementation of the prototype, the control strategy and the measurements on the prototype. In addition, the snubber with energy recovery used in the prototype to achieve soft switching is discussed in subsection 4.4.

2. HIGH VOLTAGE ASYMMETRIC DC-DC CONVERTERS

Three converters with an asymmetrical primary circuit (with a single transistor) are presented theoretically, and the transfer function is determined analytically. Then, with the obtained results, an analysis will be carried out to determine the advantages and disadvantages of each one. The most suitable for the application will be chosen, and on this basis the simulations and the construction of the prototype will continue.

2.1. Boost fed forward-flyback

The proposed topology is an imbricated converter, a forward-flyback fed from a voltage source through a boost inductor, which is shown in Figure 1(a). This arises from the series association of the Boost converter and the forward converter. This converter may operate in CM in order to obtain a better utilization of the power transistor. If the DCM is adopted [14], [15] some circuit simplification is allowed but with higher transistor currents for the same output power.

In the conduction time interval of the transistor (t_{ON}), the energy delivered by the primary source (V_E) is partly stored in the boost inductor (L_B) and the magnetizing inductance (L_m), while another part is delivered to the load. During this time no current flows through the magnetic reset diode (D_{rm}). When the transistor

is open, current flows through the diode D_{rm} and the inductor L_B delivers, together with the inductance L_m, energy to the load.

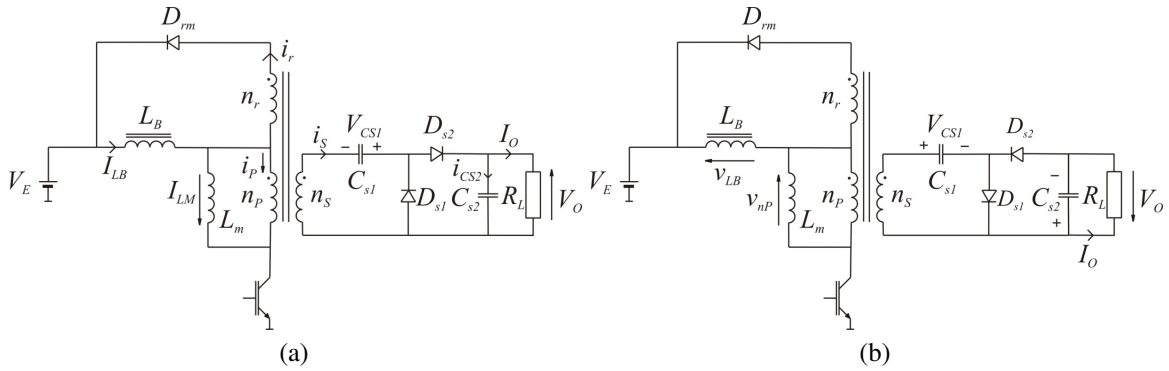


Figure 1. Boost fed forward-flyback: (a) circuit with positive output and (b) circuit with complementary or negative output

The secondary part of the converter consists of a Greinacher (also known as Cockcroft-Walton multiplier) voltage doubler circuit [6], [9], [18], [19]. When the transistor is saturated, no current flows through diode D_{s1}, the current flows through diode D_{s2} discharging capacitor C_{s1} and charging capacitor C_{s2} with the sum of the secondary winding voltage n_S and the voltage on C_{s1}. Finally, when the transistor is blocked, diode D_{s1} conducts charging capacitor C_{s1} through winding n_S and capacitor C_{s2} discharges through the load. Next, the transfer function of the circuit will be obtained in analytical form, this is necessary to evaluate the circuit and then propose the control strategy. The average voltage at the magnetizing inductance referred to the primary must be zero, therefore as in (1).

$$v_{n_{PF}} D = V_{CS1} \frac{n_P}{n_S} (1 - D) \qquad \Longrightarrow \qquad v_{n_{PF}} = \frac{1 - D}{D} V_{CS1} \frac{n_P}{n_S} \tag{1}$$

Where the duty cycle is defined as $D = \frac{t_{ON}}{T}$ and T is the total switching period. In the conduction time of the transistor, on the secondary circuit the output voltage is as (2).

$$V_O = v_{n_{PF}} \frac{n_S}{n_P} + V_{CS1} \tag{2}$$

Using (1) results in (3).

$$V_O = \frac{1 - D}{D} V_{CS1} \frac{n_P}{n_S} \frac{n_S}{n_P} + V_{CS1} \qquad \Longrightarrow \qquad V_{CS1} = D V_O \tag{3}$$

Then (1) can be rewritten as (4).

$$v_{n_{PF}} = (1 - D) \frac{n_P}{n_S} V_O \tag{4}$$

At the boost inductor the average voltage also must be zero, therefore as in (5).

$$D v_{L_{BF}} = (1 - D) v_{L_{BR}} \tag{5}$$

In the conduction time of the transistor, as (6).

$$v_{L_{BF}} = V_E - v_{n_{PF}} \tag{6}$$

Using (4) results in (7).

$$v_{L_{BF}} = V_E - (1 - D) \frac{n_P}{n_S} V_O \tag{7}$$

When the transistor is blocked, and with (3), is obtained as (8).

$$v_{L_{BR}} = \frac{n_r}{n_S} V_{CS1} \qquad \Longrightarrow \qquad v_{L_{BR}} = \frac{n_r}{n_S} D V_O \tag{8}$$

Then, the average voltage is as (9).

$$D\left[V_E - (1-D)\frac{n_P}{n_S} V_O\right] = (1-D)\frac{n_r}{n_S} D V_O \tag{9}$$

Finally, the output voltage is as (10).

$$V_O = \frac{n_S}{n_r + n_P} \frac{1}{(1-D)} V_E \tag{10}$$

And from this, the transfer function is directly obtained.

2.1.1. Complementary output

Given the type of application for these circuits, electrostatic particle accelerators, it is interesting to determine what the transfer function of the circuit is for the complementary output. The circuit is shown in Figure 1(b). The previous analysis is repeated, the average voltage at the magnetizing inductance referred to the primary must be zero, therefore as in (11).

$$v_{n_{PF}} D = v_{n_{SR}} \frac{n_P}{n_S} (1-D) \tag{11}$$

In the conduction time of the transistor, on the secondary side as (12).

$$v_{n_{SF}} = V_{CS1} = v_{n_{PF}} \frac{n_S}{n_P} \tag{12}$$

And when the transistor is blocked as (13).

$$V_O = V_{CS1} + v_{n_{SR}} \tag{13}$$

Combining both expressions gives as (14).

$$v_{n_{SR}} = V_O - v_{n_{PF}} \frac{n_S}{n_P} \tag{14}$$

Using it in (11) gives as (15).

$$v_{n_{PF}} = V_O \frac{n_P}{n_S} (1-D) \tag{15}$$

And also as in (16).

$$v_{n_{SR}} = D V_O \tag{16}$$

The average voltage at the boost inductor must be zero, its expression is the same as (5). In the conduction time of the transistor its voltage is equal to (6), using (15) in it.

$$v_{L_{BF}} = V_E - (1-D)\frac{n_P}{n_S} V_O \tag{17}$$

When the transistor is blocked, and then using (16), gives as (18).

$$v_{L_{BR}} = \frac{n_r}{n_S} v_{n_{SR}} \qquad \Longrightarrow \qquad v_{L_{BR}} = \frac{n_r}{n_S} D V_O \tag{18}$$

Then, the average voltage has the same expression as (9) and the output voltage is as (19).

$$V_O = \frac{n_S}{n_r + n_P} \frac{1}{(1-D)} V_E \tag{19}$$

It can be observed that the transfer is the same as in the previous case, which makes the converter attractive for use in those cases where two complementary outputs with the same voltage values are required using a single secondary winding and two rectifier circuits.

2.1.2. Magnetizing current

For further design of the magnetic components it is important to determine the magnetizing current (I_{LM}), using the circuit shown in Figure 1(a). The average current in the capacitors C_{s1} and C_{s2} must be zero, therefore as (20).

$$i_{S_F} D = i_{S_R} (1 - D) \tag{20}$$

And as (21).

$$i_{CS2_F} D = I_O (1 - D) \tag{21}$$

In the conduction time of the transistor, the current on the secondary side is as (22).

$$i_{S_F} = i_{CS2_F} + I_O \tag{22}$$

Using this in (21) gives (23).

$$i_{S_F} = \frac{I_O}{D} \tag{23}$$

And using the latter in (20) gives (24).

$$i_{S_R} = \frac{I_O}{1 - D} \tag{24}$$

According to the principle of conservation of energy, if losses are neglected:

$$P_O = V_O I_O = P_E = V_E I_{LB} D \qquad \Longrightarrow \qquad I_{LB} = \frac{V_O I_O}{V_E D} \tag{25}$$

When the transistor is blocked, the current through the magnetic reset winding and the current through the magnetizing inductance are in (26).

$$i_{r_R} = I_{LB} \qquad \wedge \qquad I_{LM} = i_{P_R} \tag{26}$$

The magnetomotive force is as (27).

$$m.m.f. = n_S i_{S_R} - i_{r_R} n_r - i_{P_R} n_P \tag{27}$$

assuming an ideal transformer as (28).

$$n_S i_{S_R} = i_{r_R} n_r + i_{P_R} n_P \tag{28}$$

And using (24)–(26).

$$I_{LM} = \frac{n_S}{n_P} \frac{I_O}{(1 - D)} - \frac{V_O I_O}{V_E D} \frac{n_r}{n_P} \tag{29}$$

Finally, using (10), the magnetizing current is as (30).

$$I_{LM} = \frac{n_S}{n_P} \frac{I_O}{(1 - D)} \left[1 - \frac{n_r}{D (n_r + n_P)} \right] \tag{30}$$

An interesting aspect of the magnetizing current is to determine what values of the duty cycle make it zero, resulting in (31).

$$D = \frac{n_r}{n_r + n_P} \qquad \Longrightarrow \qquad \frac{n_r}{n_P} = \frac{D}{1 - D} \tag{31}$$

This last expression is important because the operation of the converter at this point cancels the magnetizing current, which minimizes the core dimensions and avoids the increase of core losses associated with continuous bias magnetization [20], [21].

2.2. Flyback fed forward-flyback

This is an imbricated converter, a forward-flyback fed from a voltage source through the inductance of a flyback subconverter, shown in Figure 2(a). It arises from the series association of the primary sides of a flyback and a forward converter; the secondary sides transfer energy in parallel. In the conduction time interval of the transistor, the energy delivered by the primary source (V_E) is partly stored in the first magnetizing inductance (L_{m1}) and the second magnetizing inductance (L_{m2}), while another part is delivered to the load. During this time, no current flows through the flyback diode (D_f). When the transistor is open, current flows through the diode D_f and the inductance L_{m1} delivers together with the inductance L_{m2} energy to the load. The secondary part of the converter consists of a Greinacher voltage doubler circuit. When the transistor is saturated, no current flows through diode D_{s1}, the current flows through diode D_{s2} discharging capacitor C_{s1} and charging capacitor C_{s2} with the sum of the secondary winding voltage n_S and the voltage on C_{s1}. Finally, when the transistor is blocked, diode D_{s1} conducts charging capacitor C_{s1} through winding n_S and capacitor C_{s2} discharge through the load.

Using the same analysis as for the previous converter, the output voltage is obtained as (32).

$$V_O = \frac{1}{\frac{n_B}{Dn_r} + \frac{n_P}{n_S}} \frac{1}{(1-D)} V_E \tag{32}$$

And from this, the transfer function is directly obtained.

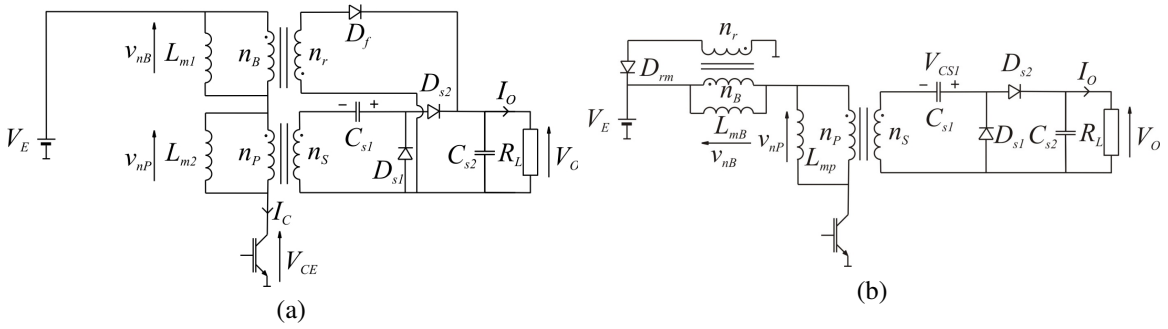


Figure 2. Two topologies studied: (a) flyback fed forward-flyback circuit and (b) boost-flyback fed forward-flyback circuit

2.3. Boost-flyback fed forward-flyback

This is an imbricated converter, a forward-flyback fed from a voltage source through the inductor of a boost-flyback subconverter, shown in Figure 2(b). It arises from the series association of the boost-flyback converter and the forward-flyback converter. In the conduction time interval of the transistor, the energy delivered by the primary source (V_E) is partly stored in the boost inductor (L_{mB}) and the magnetizing inductance (L_{mp}), while another part is delivered to the load. During this time no current flows through the magnetic reset diode (D_{rm}). When the transistor is open, current flows through the diode D_{rm} and the inductor L_{mB} returns energy to the source V_E, the inductance L_{mp} delivers energy to the load. The secondary part of the converter consists of a Greinacher voltage doubler circuit. When the transistor is saturated, no current flows through diode D_{s1}, the current flows through diode D_{s2} discharging capacitor C_{s1} and charging capacitor C_{s2} with the sum of the secondary winding voltage n_S and the voltage on C_{s1}. Finally, when the transistor is blocked, diode D_{s1} conducts charging capacitor C_{s1} through winding n_S and capacitor C_{s2} discharge through the load. Using the same analysis as for the first converter, the output voltage is obtained as (33).

$$V_O = \frac{n_S}{n_P} \left[\frac{1}{(1-D)} - \frac{n_B}{Dn_r} \right] V_E \tag{33}$$

And from this, the transfer function is directly obtained.

2.4. Converter comparison and selection

The first converter, called boost fed forward-flyback and presented in subsection 2.1, requires a transformer with split primary and a boost inductor whose currents have fundamental DC components. However, according to (31), it was determined that for a certain value of D, the magnetizing current of the transformer is zero and allows to reduce the core size and avoid the need for a gap. The second converter, called flyback fed forward-flyback and presented in subsection 2.2, requires two high voltage transformers, which makes it difficult to build, especially the second transformer that requires a secondary winding with twice the voltage of the first one. The third converter, called boost-flyback fed forward-flyback and presented in subsection 2.3, requires two flyback transformers of higher primary current than the other two circuits because when the transistor conducts it returns part of the energy to the primary source. This also worsens the performance of the converter if the primary source is not fully reversible as in the case of a diode-capacitor bridge source. According to the expressions for the output voltage of the converters, (10), (32) and (33), the possibility of varying this voltage is evaluated. The first converter, subsection 2.1, is the most limited in the range of voltages obtained, while the third one, subsection 2.3, requires the smallest variation of the duty cycle to obtain a wide range of voltages.

All topologies were analyzed theoretically and simulated numerically, and the first one (boost fed forward-flyback) was adopted to implement the experimental converter prototype presented in this work. The zero magnetization current operation condition will be adopted for the design in order to reduce the core losses due to DC magnetizing bias [20]. The possibility of having a complementary output with the same transfer function is highly valued for this application, while not being required to vary the output voltage over a wide range. In addition, soft switching in the transistor will be sought, which is discussed in subsection 4.4.

3. SIMULATIONS

The behavior of the selected converter is studied by simulating the circuit through *PSpice*®, and then comparing the results with those obtained analytically. For the simulation, a primary DC voltage source, V_E, of 311 V is used, which corresponds to the rectified voltage value of a distribution network with a rms value of 220 V. An output voltage value, V_O, of 1 kV and an output power of 500 W are adopted. The switching frequency is set at 35 kHz and a duty cycle D at 0.5, since this is the optimum value studied if both primary windings are adopted equal according to (31). The circuit used in the simulation is shown in Figure 3(a).

If the capacitors in the Greinacher capacitive multiplier have small capacitance some current might be drawn through the diode D_{rm}. Therefore, an auxiliary MOSFET transistor was added in series with the magnetic reset diode to avoid unwanted conduction during the conduction time of the main transistor. Both devices are controlled in a complementary way. The auxiliary one, a low voltage MOSFET, has low conduction losses and D_{rm} must be maintained to avoid conduction by the transistor's internal diode. The need for a floating voltage source for the auxiliary transistor command will be solved later in the converter prototype. The resulting waveforms are shown in Figures 3(b)–3(e).

4. PROTOTYPE IMPLEMENTATION

The prototype consists of a full-wave rectifier formed by a four-diode bridge (50 A, 1 kV) followed by three electrolytic capacitors (470 μF, 400 V). Then follows the power stage formed by the selected converter feeding two voltage multipliers to obtain the two symmetrical output voltages. A double control stage for duty cycle and frequency is used, as well as the necessary drivers to control both the main IGBT transistor and the auxiliary MOSFET [22].

4.1. Power stage

4.1.1. Primary side

In order to simplify the control circuit, the primary circuit of the converter was reformed so that both the emitter of the IGBT and the source of the auxiliary MOSFET have a common ground. This eliminates the need for an auxiliary floating source to drive the transistor. The reform can be seen in Figure 4(a).

4.1.2. Voltage multiplier

Two Greinacher (or Cockcroft-Walton) voltage multipliers of 4 stages each were added to the converter, in order to obtain a source with complementary output voltages of 10 kV with a power of 600

W at each output. This is shown in Figure 4(b), where a secondary winding with intermediate point is used to obtain both outputs [9], [19], [23]. The capacitors used in the voltage multipliers were of polypropylene dielectric, 500 V insulation voltage. In the case of the first stage, C_{s1}, 3 capacitors of 1 μF had to be placed in series; then for C_{s2}, 6 in series of 1 μF; for C_{s3} and C_{s4}, 6 in series of 680 nF; for C_{s5} and C_{s6}, 6 in series of 470 nF; and finally for C_{s7} and C_{s8}, 6 in series of 100 nF.

In order to keep the two outputs stable, a double control circuit is used to control the duty cycle on the one hand and the switching frequency on the other hand. For this reason, the value of the first capacitor, C_{s1neg}, is modified to the negative voltage multiplier, decreasing it to 30 nF, making this multiplier more sensitive to frequency variations than the positive multiplier whose voltage is controlled by varying the duty cycle.

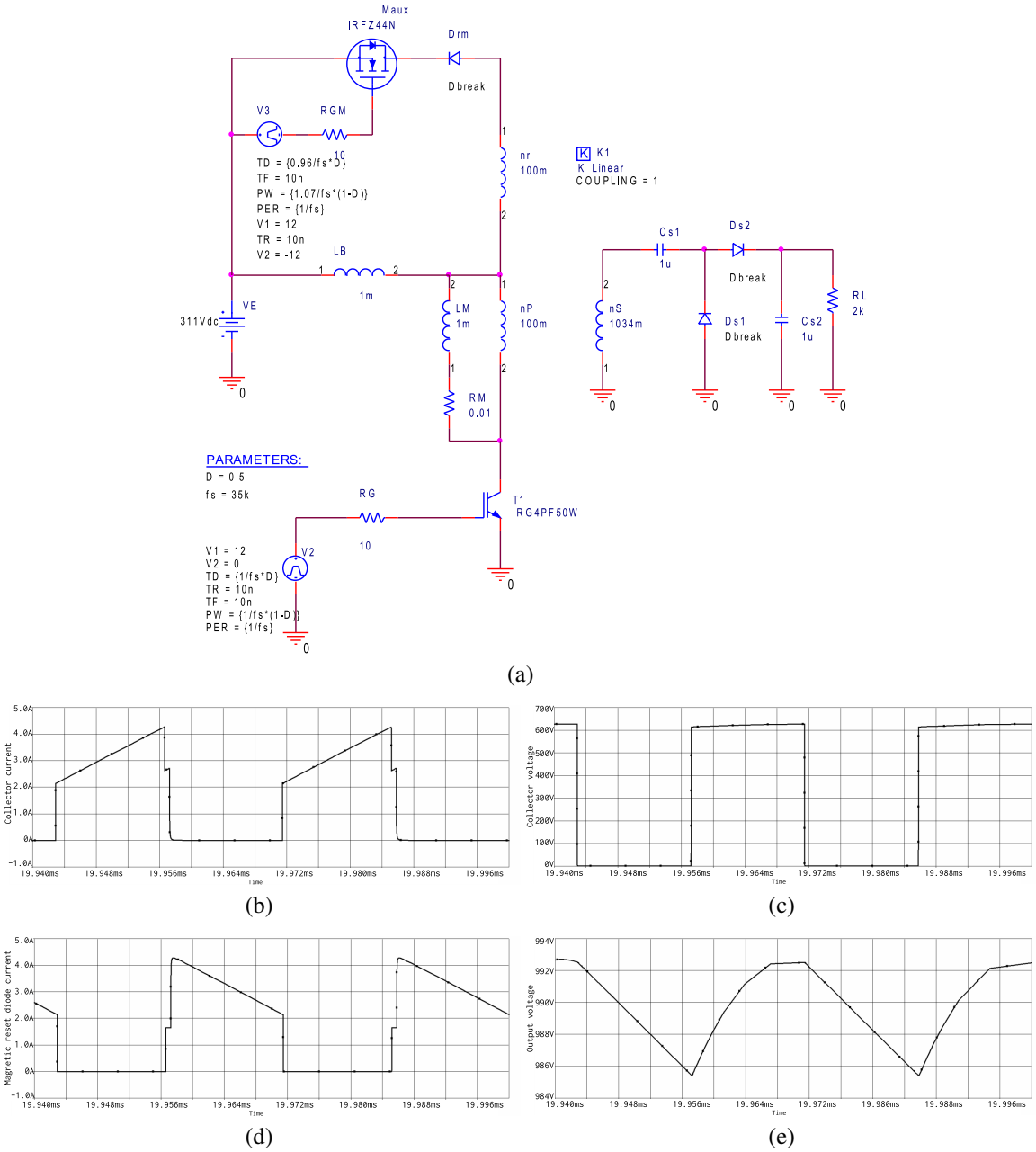
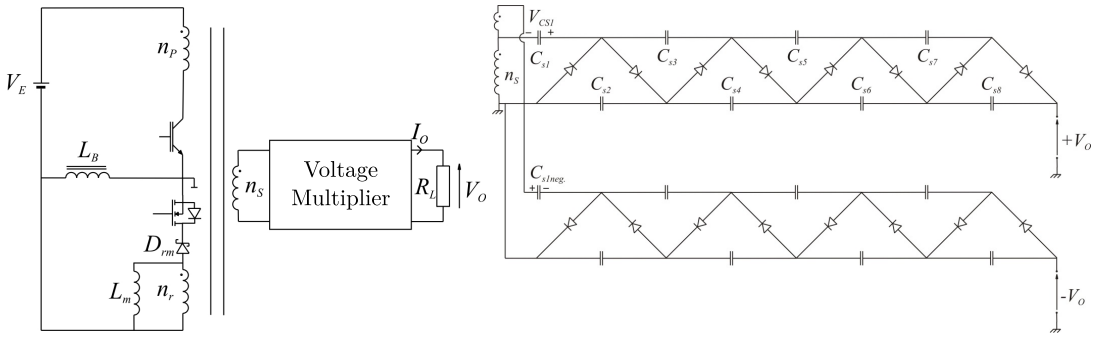


Figure 3. Simulation results of the boost fed forward-flyback converter: (a) circuit used in the simulation, (b) collector current, (c) collector voltage, (d) magnetic reset diode current, and (e) output voltage ripple



(a) (b)

Figure 4. Circuits used in the power stage: (a) modification carried out on the primary side of the converter and (b) the double voltage multiplier

4.2. Control strategy

The main block of the control system was implemented with the SG3524 integrated circuit which has the necessary modules to perform a duty cycle variation control loop. This standard, classic and widely used integrated PWM controller was intentionally adopted to demonstrate that the control method does not require special controllers with sophisticated features. A duty cycle variation control was used for the positive output and a switching frequency variation control was used for the negative output [24].

In an asymmetrical converter composed of two sub-converters merged sharing a single power transistor, each sub-converter will have its own transfer function that will give the output DC voltage as a function of the input voltage of the primary source, the duty cycle, the switching frequency and the current of each output. Assuming that the input voltage is the same for both sub-converters, it is possible to propose:

$$V_{O1} = f_1(D, f, I_{O1}) \qquad \wedge \qquad V_{O2} = f_2(D, f, I_{O2}) \tag{34}$$

Where, V_{O1} and V_{O2} are the output DC voltages; I_{O1} and I_{O2} are the currents delivered to each load; D is the duty cycle; f is the switching frequency; and f_1 and f_2 are the transfer functions of each sub-converter. Under conditions where these transfer curves are distinct functions and have crossing points, the system of two equations formed by (34) will have a solution, and there will be two values of duty cycle and frequency which will be the solution of the system of two nonlinear equations. Necessary but not sufficient conditions for the technique to be applicable are that the transfer functions be continuous and monotonic, since the existence of more than one crossing point will generate multiple solutions and therefore unstable operation.

Each output voltage will be fed back to a control loop that will have its own differential error amplifier, so that the respective error voltages at the output of the amplifiers will be (35).

$$v_{E1} = V_{O1} - V_{O1_{\text{ref}}} \qquad \wedge \qquad v_{E2} = V_{O2} - V_{O2_{\text{ref}}} \tag{35}$$

Where, $V_{O1_{\text{ref}}}$ and $V_{O2_{\text{ref}}}$ are the desired output voltages. Based on these error voltages a duty cycle and switching frequency should be generated such that they are solution of the system of (34). That is, functions should be found such that as(36).

$$D_O = g_D(v_{E1}, v_{E2}) \qquad \wedge \qquad f_O = g_f(v_{E1}, v_{E2}) \tag{36}$$

In previous work [24] it was experimentally found that for usual forward, flyback or their imbrications converters a practical solution can be found by adopting them as control action functions, as (37).

$$D = g_D(v_{E1}) \qquad \wedge \qquad f = g_f(v_{E2}) \tag{37}$$

The functions g_D and g_f adopted in these references were feedback loops with integral and derivative compensations empirically adjusted to obtain the best possible transient behavior under load variations.

To apply this control method to the proposed dual converter, the positive output voltage is fed back with a fast loop to vary the duty cycle, while the negative output is fed back with a slower loop to vary the switching frequency. For this reason, the capacitive multiplier that generates the negative voltage has lower

capacitance so that the plant to be controlled by the slower loop is faster and partly compensates for the slower speed of its control loop. In addition, this is necessary to ensure that the transfers of the sub-converters have different slopes depending on the load currents and there is a crossover point to ensure that the system of equations has a solution and the operation is stable.

According to [6] and [18] a Greinacher (or Cockcroft-Walton) voltage multiplier has a monotonic transfer that is a function of frequency, duty cycle and output current. To ensure that the transfer functions corresponding to both capacitive multipliers have a crossover point, the negative multiplier is fed with a voltage slightly higher than that applied to the positive (by adding turns in the respective secondary). In this way, if the capacitors were all equal to each other, the negative multiplier would always give an output voltage which in modulus would always be higher than that of the positive multiplier (and there would be no crossover point). To ensure that the crossover point exists, the converter is operated at the minimum frequency and the capacitance value of the negative multiplier input capacitor C_{s1neg} (see Figure 4(b)) is reduced until the modulus of the negative voltage is lower than that of the positive voltage. Under these conditions, at minimum frequency the modulus of the negative voltage will be lower than that of the positive voltage, and on the contrary, at maximum frequency the modulus of the negative voltage will be higher.

4.2.1. Joint controller for duty cycle and switching frequency

The controller is an improvement of those initially proposed in [24]. The secondary side circuit (Figure 5) contains the error amplifiers for the feedback of both output voltages to be regulated. Each amplifier couples its error signal to the primary side (Figure 6) with galvanic isolation by means of optocouplers. The non-linearity of these optocouplers has no major influence because their transfer functions are included within two negative feedback loops with high loop gains [25]. The positive voltage feedback signal controls the duty cycle by means of the internal voltage amplifier of the SG3524 controller, while the error signal corresponding to the other supply output varies the switching frequency by means of a bipolar transistor in parallel with the relaxation resistance of the RC oscillator of the PWM modulator integrated circuit. The assembled prototype of the controller is shown in Figure 7(a).

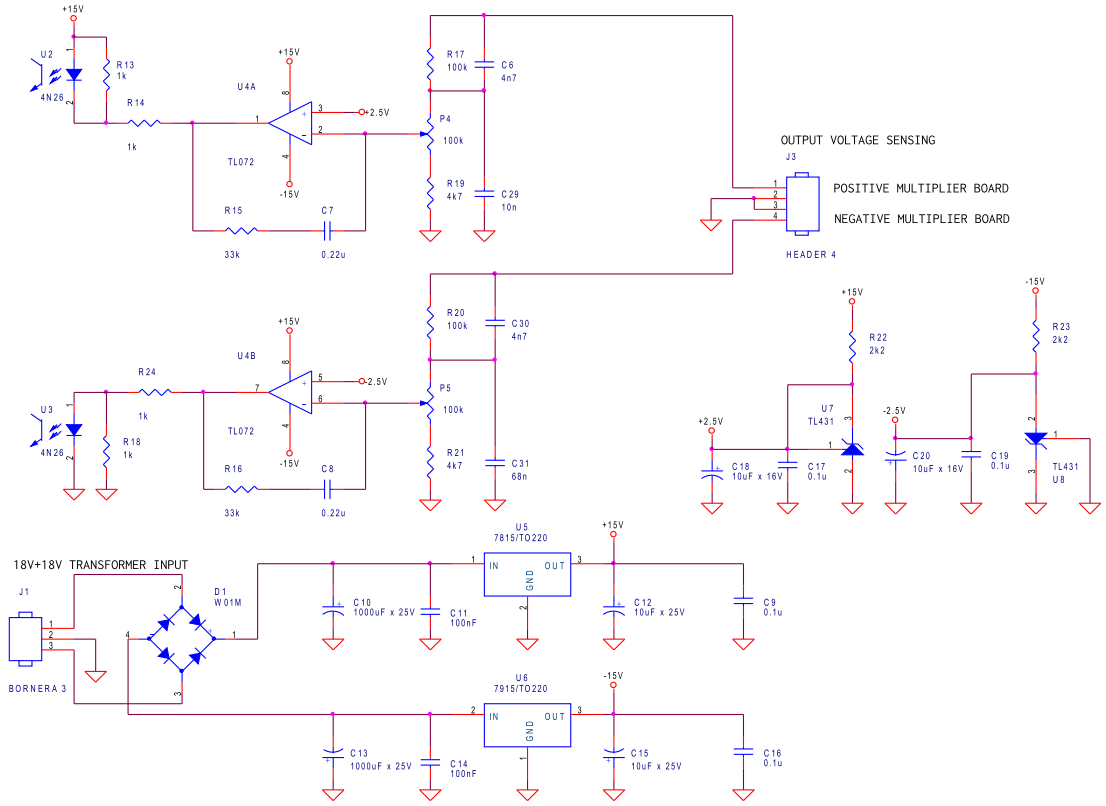


Figure 5. Circuit of the secondary side of the control stage

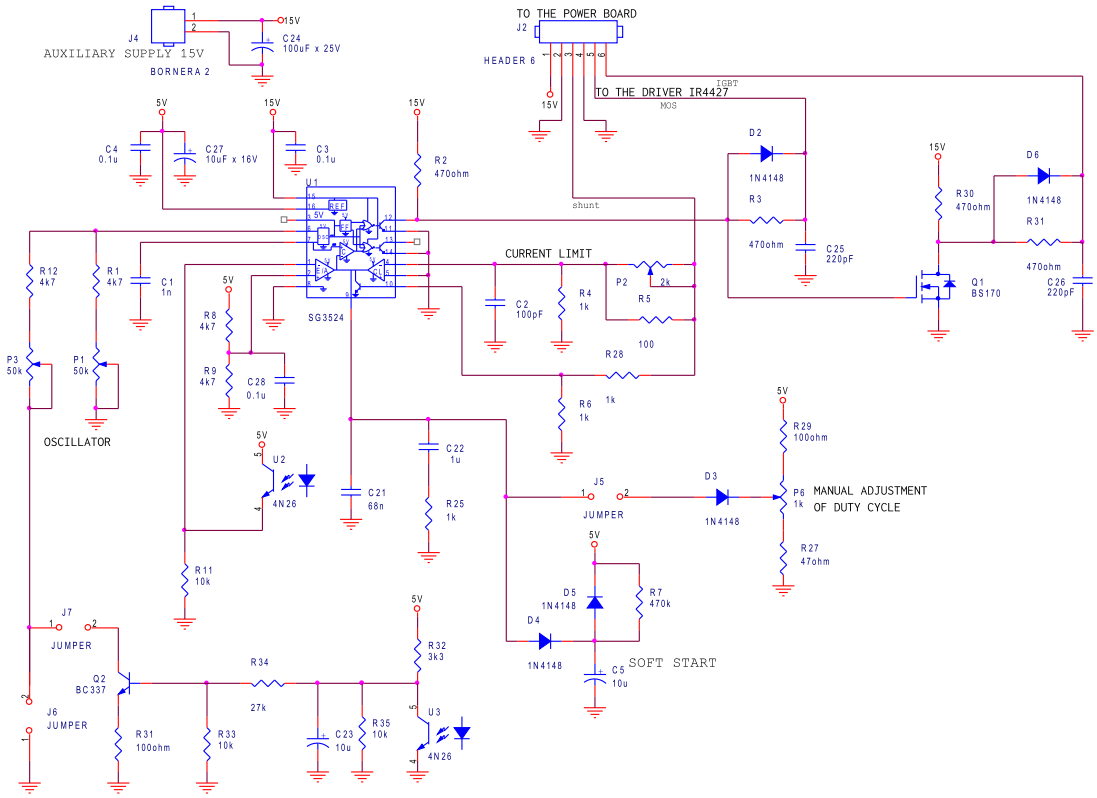
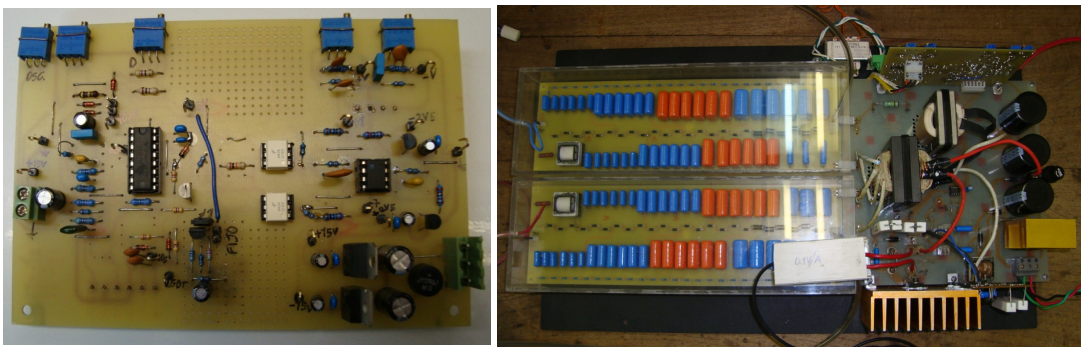


Figure 6. Circuit of the primary side of the control stage



(a) (b)

Figure 7. Converter and control board: (a) view of the control board and (b) top view of the converter with voltage multipliers on the left side and the primary converter on the right

4.3. Measurements

The assembled prototype is shown in Figure 7(b). The left side shows the voltage multipliers, the negative at the top and the positive at the bottom. On the right side is the primary converter with the control circuit at the top placed vertically.

The first measurements performed on the converter were open-loop in order to verify the current and voltage waveforms in the circuit elements. The control parameters were left constant, the duty cycle was set at 50% and the switching frequency at 35 kHz, the load was adjusted to obtain a power of 300 W at the output. The results obtained are presented in Figure 8. Measurements on the IGBT (Figure 8(a)) show the collector-emitter voltage and the collector current. The voltage shows a peak in the transition from saturation to cut-off due to the leakage inductance of the transformer, since the measurement was performed without snubber. In the transition

from cut-off to saturation, a peak is observed on the current due to the overlapping switching of the IGBT and the auxiliary MOSFET. In the measurements on the transformer (Figure 8(b)), the voltage on the windings is observed. The voltage on the primary winding and the magnetic reset winding has the same amplitude due to the equal number of turns, while the voltage on the secondary winding is higher due to the transformation ratio and the need for a high output voltage.

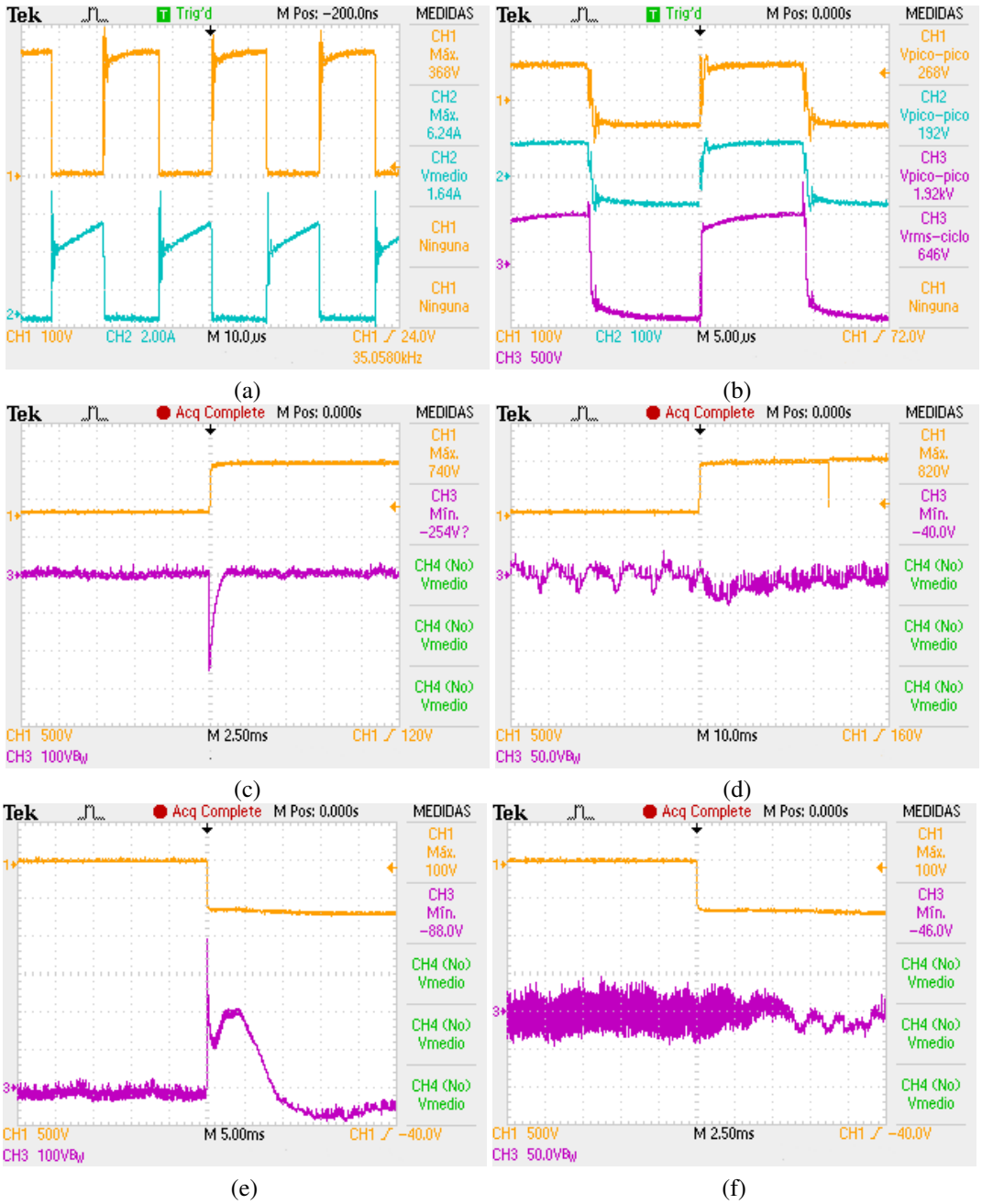


Figure 8. Measurements on the converter: (a) v_{CE} (CH1, orange) and i_C (CH2, cyan, (b) v_{n_P} (CH1, orange), v_{n_r} (CH2, cyan) and v_{n_S} (CH3, magenta), (c) v_{trigger} (CH1, orange) and $+V_O$ (CH3, magenta), (d) v_{trigger} (CH1, orange) and $-V_O$ (CH3, magenta), (e) v_{trigger} (CH1, orange) and $+V_O$ (CH3, magenta), and (f) v_{trigger} (CH1, orange) and $-V_O$ (CH3, magenta)

In order to evaluate the dynamic behavior of the converter under load changes, the load on the outputs was varied by means of a key controlled by a trigger signal, thus verifying the response of the control loop. The output voltage measurements can be seen in Figure 8, in all measurements one channel presents the trigger signal to command the change in load and the other presents the output voltage coupled in AC. Faced with a change of the load on the positive output from a power of 450 W to 600 W, keeping the load on the negative output for a power of 600 W, a reduction of 250 V is observed and after 1 ms the output voltage value is restored, this is observed in Figure 8(c). For a variation of the same type on the positive load, from 300 W to 450 W keeping the load on the negative output for a power of 300 W, on the negative output a reduction of 40 V is observed, this is presented in Figure 8(d). For load changes at the negative output from 450 W to 600 W of power, keeping the load at the positive output for 600 W of power, a variation of 200 V in the positive voltage is observed, which is restored to its previous value after 15 ms, as shown in Figure 8(e). In the case of the negative output it is observed that the frequency increases and thus decreases the ripple of this voltage due to the effect of the control loop, this is presented in Figure 8(f). The overshoot voltage of 100 V over 10 kV represents a 1% overvoltage (acceptable for the intended application), but if better performance is required, the capacitance of the capacitive multiplier capacitors can be increased or the loop compensation modified so that the converter response is underdamped.

The efficiency of the converter was evaluated with symmetrical loads on both outputs for different output power values, from 300 W to 1200 W. A classic RDC snubber was used initially, and the results are shown in Table 1. Then, the proposed LC snubber for soft switching with energy recovery, detailed in section 4.4, was used, and the results obtained are shown in Table 1. The performance achieved is acceptable for most HV DC supply applications.

Static cross-regulation was evaluated for both outputs, varying the load for each channel independently from 150 W to 600 W, measuring the output voltages, duty cycle, and operating frequency of the converter. Since the controller acts on output voltages through the duty cycle and switching frequency of the transistor, some load conditions may not be stable. Table 2 summarizes the static cross-regulation results. For the intended application of electrostatic lens feeding, this performance is acceptable.

Table 1. Efficiency with symmetrical loads on both outputs

With classic RCD snubber				With LC snubber			
$P_O\,(W)$	$I_{IN}\,(A)$	$P_{IN}\,(W)$	Efficiency (%)	$P_O\,(W)$	$I_{IN}\,(A)$	$P_{IN}\,(W)$	Efficiency (%)
300	1.125	350	86	300	1.13	351.4	85
600	2.156	670	90	600	2.16	671.8	89
900	3.22	1000	90	900	3.15	979.6	91
1200	4.4	1368	88	1200	4.3	1320	90

Table 2. Static cross-regulation

$+P_O\,(W)$	$-P_O\,(W)$	$+V_O\,(kV)$	$-V_O\,(kV)$	Duty (%)	$f\,(kHz)$
150	150	10	10.18	39	25
150	300	10	10	38	48.7
150	450	10	9.7	38	49.8
150	600		Unstable		
300	150	10	10.45	42	25
300	300	10	10.05	41	30.9
300	450	10	8.88	39	47.45
300	600		Unstable		
450	300	10	10.2	44	25
450	450	10	10	40	47
450	600	10	10	40	62
600	450	10	10.03	44	28.5
600	600	10	10.03	42	64

4.4. Soft switching

In order to enable the IGBT transistor to operate with soft switching [26], [27], allowing better performance by delivering the energy stored in the parasitic components of the input transformer to the primary source, and also limit the over-peak voltage that occur in the transistor at the time of switching, a passive snubber or LC turn-off circuit is proposed. This is shown in Figure 9(a).

During the transistor conduction time the voltage v_{CE} can be considered very close to zero, diodes D_{S1} and D_{S2} do not conduct and the voltage across the capacitor, v_{CS}, is assumed to be equal to the source voltage V_E. When the transistor is turning off and the voltage v_{CE} increases, the diode D_{S1} becomes direct biased and the capacitor C_S begins to discharge. The transistor current during turn-off can be approximated by a linear function. The expressions for the collector current and the capacitor current, $I_P - i_C$, in this state are

$$i_C = \begin{cases} I_P\left(1 - \frac{t}{t_f}\right) & \text{if } 0 \leq t < t_f\,, \\ 0 & \text{if } t_f \leq t \end{cases} \qquad \wedge \qquad i_{CS} = \begin{cases} \frac{I_P}{t_f} t & \text{if } 0 \leq t < t_f\,, \\ I_P & \text{if } t_f \leq t < t_x\,, \\ 0 & \text{if } t_x \leq t \end{cases} \tag{38}$$

Where t_f is the time it takes for the transistor to turn off, and t_x the time until the primary current is zero and current begins to flow through the magnetic reset winding n_r. The voltage on the capacitor C_S according to its current is as (39).

$$v_{CS} = \begin{cases} V_E - \frac{I_P}{2C_S t_f} t^2 & \text{if } 0 \leq t < t_f\,, \\ V_E - \frac{I_P t_f}{2C_S} - \frac{I_P}{C_S}\left(t - t_f\right) & \text{if } t_f \leq t < t_x\,, \\ V_E - \frac{I_P t_f}{2C_S} - \frac{I_P}{C_S}\left(t_x - t_f\right) & \text{if } t_x \leq t\,. \end{cases} \tag{39}$$

Then, when the transistor becomes active, the voltage v_{CE} decreases, and when it approaches zero, the diode D_{S2} begins to conduct, forming together with the inductor L_S a resonant circuit LC under-damped since the resistance value is only that of the inductor wire. The current can only have a half-cycle because the diode D_{S2} is in series. The inductor current is as (40).

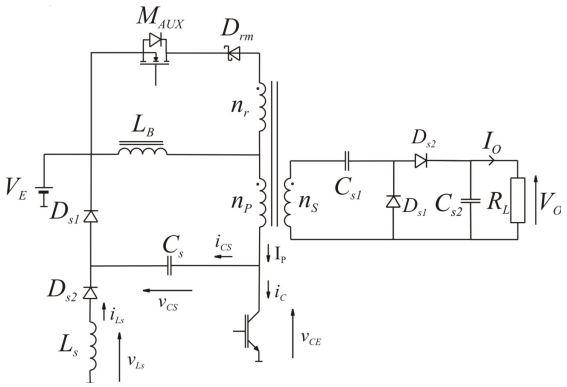
$$i_{LS} = -v_{LS}(0)\sqrt{\frac{C_S}{L_S}}\sin\left(\frac{t}{\sqrt{L_S C_S}}\right) \tag{40}$$

The converter was simulated without the snubber circuit, initially to compare its behavior, and then with the snubber. A transformer leakage inductance of 5 μH was adopted, a value obtained by measurement after its construction. The results obtained are shown in Figure 9(a). It is observed that without the snubber circuit, in Figure 9(b), hard switching occurs and a voltage overshoot of approximately 1 kV occurs at the collector, during the transistor's turn-off, due to the transformer leakage inductance. By adding the LC snubber circuit, with the values used in the prototype C_S = 2.2 nF and L_S = 100 μH, it can be seen in Figure 9(c) that the collector voltage overshoot, during the transistor's turn-off, decreases to a value below 800 V and soft switching occurs. The collector current and voltage during the transistor turn-on can be observed in Figure 9(d), with the snubber circuit, which shows a peak in the current generated when current flows through the snubber inductor, which can also be seen in Figure 9(e). This increases the conduction losses of the transistor, but when operating at high frequency, this increase is compensated by the reduction of the switching losses.

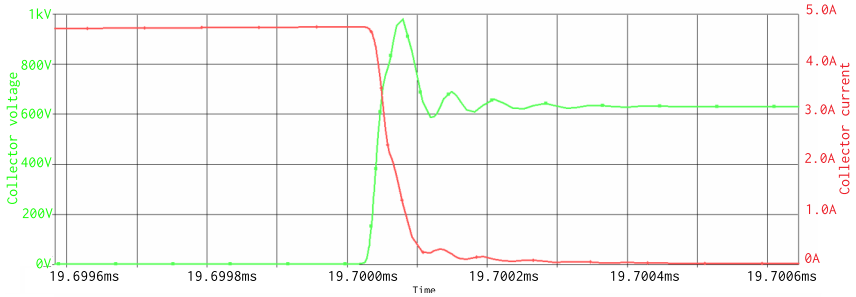
On the prototype [22], the power circuit version for common command drives was adopted (Figure 10(a)). There, when transistor T_{pot} conducts, the capacitor C_{S2} takes charge through D_{S3} with a maximum current limited by the current available in L_B. In turn the current limited by L_S inverts the charge in C_{S1} in a completely analogous way to what happened in the previous snubber circuit. The voltage in C_{S1} reaches a maximum value limited by the conduction of D_{S1} being equal to the secondary voltage multiplied by n_P/n_S. When the transistor T_{pot} is blocked, the current passing through the primary leakage inductance (in series with n_P) discharges the capacitor C_{S1} in a completely similar way to that seen in the previous snubber assembly, reversing the voltage on C_{S1} which is thus prepared for a new switching to the on state (where its discharge current would again be limited by L_S).

On the prototype, the operation of the snubber was verified, the current and voltage at the IGBT collector were measured and observed in an XY representation on the oscilloscope. Figures 10(b) and 10(c) show the measurements with and without snubber for comparison.

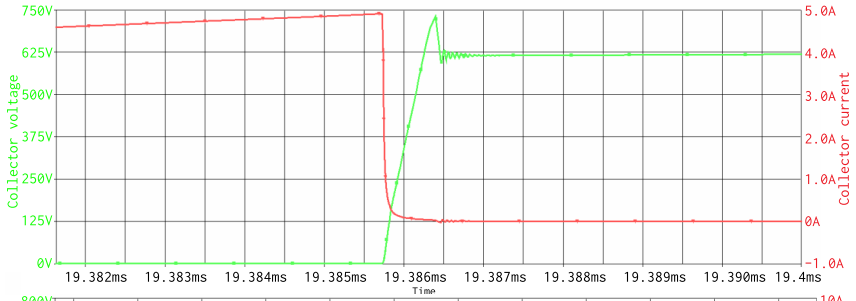
(a)



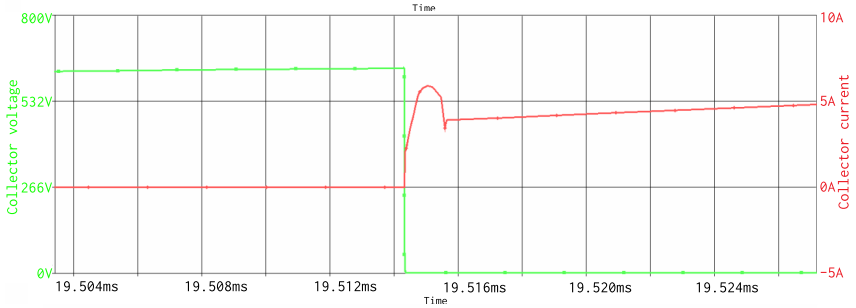
(b)



(c)



(d)



(e)

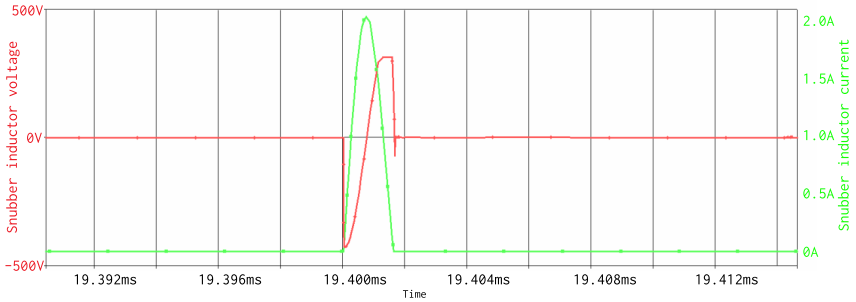
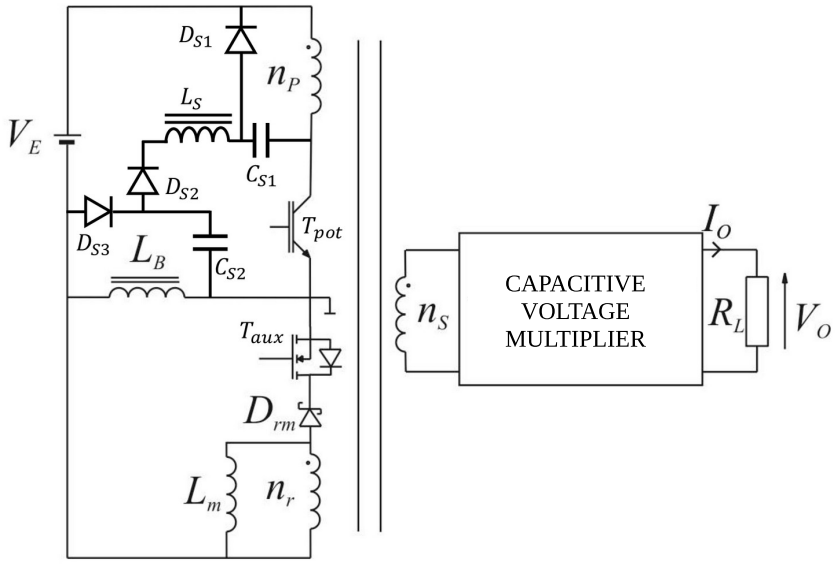
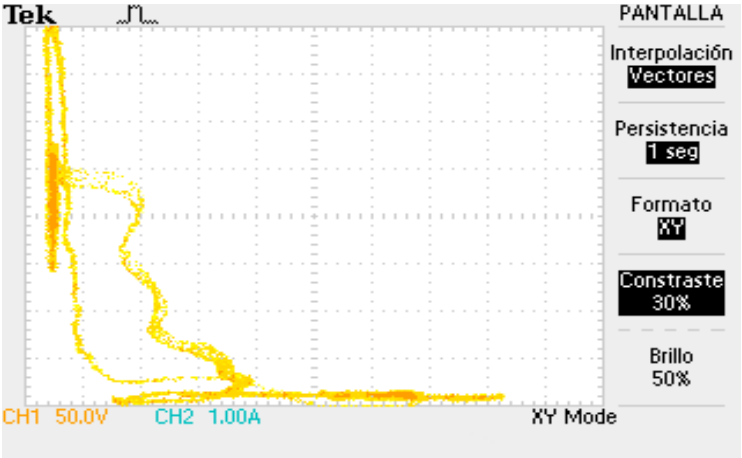


Figure 9. Converter with snubber and simulations results: (a) converter circuit used for soft switching with energy recovery, (b) collector current (red) and voltage (green) during transistor's turn-off without snubber, (c) collector current (red) and voltage (green) during transistor's turn-off with snubber, (d) collector current (red) and voltage (green) during transistor's turn-on with snubber, and (e) current (green) and voltage (red) on snubber's inductor

(a)



(b)



(c)

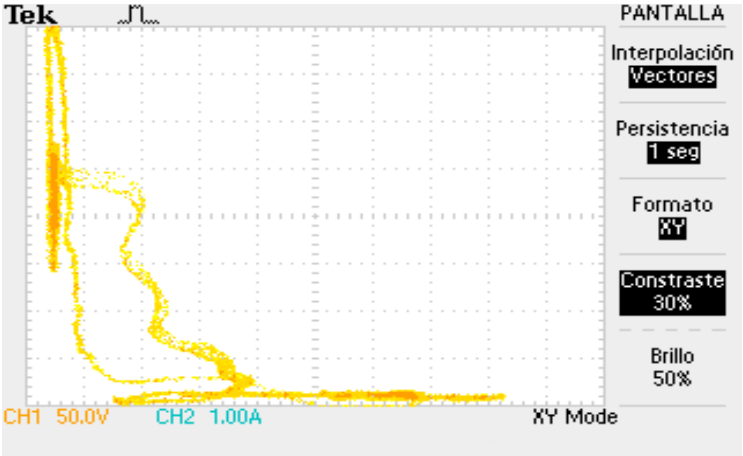


Figure 10. Converter with snubber with common command ground and switching comparison

5. CONCLUSION

In some applications, it is mandatory to use symmetrical supply voltages. In these cases, this converter topology allows the number of power transistors to be halved, thus increasing reliability. This is particularly advantageous when the power supply systems are composed of a large number of converters (as is often the case in electrostatic particle accelerators).

The adopted control strategy, a mixed control by duty cycle variation for the positive output and frequency variation for the negative output, was able to keep the two output voltages stable and without variations. Difficulties were encountered in maintaining both outputs stable when the load unbalance range between the two exceeds 100%, leaving this point as a working target for future improvements. However, the intention of this work is fulfilled, applying this double converter to fixed loads with the intention of better stabilizing the outputs keeping their voltages paired.

The implemented topology is very interesting for other applications. For example, it could be applied to develop lower voltage power supplies using electrolytic type output capacitors with higher capacitance values and consequently the auxiliary MOSFET transistor would not be necessary. Furthermore, a power supply capable of stabilizing the output voltage by actively improving the power factor taken from the grid could be implemented. In this case the proposed dual control should change by feeding back the output voltage controlling the duty cycle with a fast loop and the input current controlling the switching frequency with a slightly slower loop.

FUNDING INFORMATION

This work was supported by the Universidad de Buenos Aires with the Grant "UBACYT 21020230100622BA" titled *"Convertidores de potencia para fuentes de alta tensión, generadores de pulsos y otras aplicaciones industriales"*.

AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
Diego Alberto Fanego	✓				✓	✓		✓	✓	✓	✓			
Orlando Silvio Sandini		✓	✓		✓	✓		✓	✓		✓			
Hernán Emilio Tacca	✓			✓	✓	✓	✓			✓	✓	✓	✓	✓
Andrés Juan Kreiner	✓						✓			✓		✓		✓

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal Analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject Administration
Fu : **Fu**nding Acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author, [DAF], upon reasonable request.

REFERENCES

[1] A. J. Kreiner *et al.*, "Present status of accelerator-based BNCT," *Reports of Practical Oncology & Radiotherapy*, vol. 21, no. 2, pp. 95–101, 2016, doi: 10.1016/j.rpor.2014.11.004.
[2] D. Greene and P . Williams, *Linear accelerators for radiation therapy*. CRC Press, 1997. doi: 10.1201/9780429246562.

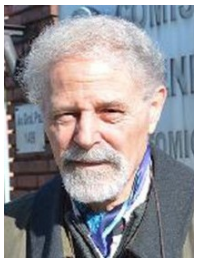
[3] E. Accelerators, "Fundamentals and applications," in *Electrostatic Accelerators*, 1st ed., Springer, 2005. [Online]. Available: http://books.google.com/books?id=tc6CEuIV1jEC&pgis=1.
[4] A. D. Mankani *et al.*, "Design and development of 500 kV, 100 mA DC high voltage power supply for particle accelerators at IPR," in *27th IAEA Fusion Energy Conference*, 2018.
[5] M. T. Outeiro, R. Visintini, and G. Buja, "Considerations in designing power supplies for particle accelerators," *IECON Proceedings (Industrial Electronics Conference)*, pp. 7076–7081, 2013, doi: 10.1109/IECON.2013.6700307.
[6] A. Rajaei, M. Shahparasti, A. Nabinejad, Y. Niazi, and J. M. Guerrero, "Switching strategy development, dynamic model, and small signal analysis of current-fed Cockcroft-Walton voltage multiplier," *IEEE Open Journal of Power Electronics*, vol. 2, pp. 591–602, 2021, doi: 10.1109/OJPEL.2021.3128066.
[7] M. Forouzesh, Y. P. Siwakoti, S. A. Gorji, F. Blaabjerg, and B. Lehman, "Step-up DC–DC converters: a comprehensive review of voltage-boosting techniques, topologies, and applications," *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9143–9178, Dec. 2017, doi: 10.1109/TPEL.2017.2652318.
[8] S. Park, J. Yang, and J. Rivas-Davila, "A hybrid Cockcroft–Walton/Dickson multiplier for high voltage generation," *IEEE Transactions on Power Electronics*, vol. 35, no. 3, pp. 2714–2723, Mar. 2020, doi: 10.1109/TPEL.2019.2929167.
[9] Z.-F. He, J.-L. Zhang, Y.-H. Liu, Y.-T. Zhang, and Y. Zhang, "Characteristics of a symmetrical Cockcroft-Walton power supply of 50 Hz 1.2 MV/50 mA," *Review of Scientific Instruments*, vol. 82, no. 5, May 2011, doi: 10.1063/1.3592597.
[10] S. Iqbal, "A hybrid symmetrical voltage multiplier," *IEEE Transactions on Power Electronics*, vol. 29, no. 1, pp. 6–12, Jan. 2014, doi: 10.1109/TPEL.2013.2251474.
[11] W. Gao, Y. Zhang, X. Lv, and Q. Lou, "Non-isolated high-step-up soft switching DC/DC converter with low-voltage stress," *IET Power Electronics*, vol. 10, no. 1, pp. 120–128, Jan. 2017, doi: 10.1049/iet-pel.2016.0323.
[12] Y. Zheng, W. Xie, and K. M. Smedley, "A family of interleaved high step-up converters with diode–capacitor technique," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 2, pp. 1560–1570, Jun. 2020, doi: 10.1109/JESTPE.2019.2907691.
[13] Z. Zhiguo and Z. Lin, "Analysis and design of isolated flyback voltage-multiplier converter for low-voltage input and high-voltage output applications," *IET Power Electronics*, vol. 6, no. 6, pp. 1100–1110, Jul. 2013, doi: 10.1049/iet-pel.2012.0552.
[14] J. A. Serrano, P. Alou, and J. A. Oliver, "DCM forward-flyback converter with Cockcroft Walton voltage multiplier: steady-state analysis considering the influence of the parasitic capacitances at very low power and very high voltage gain," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2019, pp. 6841–6847. doi: 10.1109/ECCE.2019.8911903.
[15] M. S. Dall'Asta, V. B. Fuerback, and T. Brunelli Lazzarin, "DCM forward-flyback converter integrated with a 5-order cockcroft-walton voltage multiplier: A steady-state and resonant current analysis," in *2017 Brazilian Power Electronics Conference (COBEP)*, Nov. 2017, pp. 1–6. doi: 10.1109/COBEP.2017.8257407.
[16] B. P. Hong, G. Hwan, M. Kim, and H. Kim, "The development progress of the high current tandem accelerator for BNCT in KIRAMS," in *The 5th All-Russian School of Young Scientists on BNCT*, Novosibirsk, 2023.
[17] G. Marshall, "Biomedical applications of electrochemistry, use of electric fields in cancer therapy," in *Encyclopedia of Applied Electrochemistry*, New York: Springer New York, 2014, pp. 126–131. doi: 10.1007/978-1-4419-6996-5_250.
[18] S. Iqbal and R. Besar, "A bipolar Cockcroft-Walton voltage multiplier for gas lasers," *American Journal of Applied Sciences*, vol. 4, no. 10, pp. 795–801, Oct. 2007, doi: 10.3844/ajassp.2007.795.801.
[19] A. Lamantia, P. G. Maranesi, and L. Radrizzani, "Small-signal model of the Cockcroft-Walton voltage multiplier," *IEEE Transactions on Power Electronics*, vol. 9, no. 1, pp. 18–25, Jan. 1994, doi: 10.1109/63.285489.
[20] H. E. Tacca, "Core loss prediction in power electronic converters based on Steinmetz parameters," in *2020 IEEE Congreso Bienal de Argentina (ARGENCON)*, Dec. 2020, pp. 1–8. doi: 10.1109/ARGENCON49523.2020.9505470.
[21] S. Ang, A. Oliva, G. Griffiths, and R. Harrison, *Power-switching converters*, 2nd ed. CRC Press, 2010.
[22] A. J. Kreiner, O. S. Sandini, and H. E. Tacca, "Static electrical energy converter device with asymmetric structure for power supply," AR128160A1, 2022.
[23] F. Belloni, P. Maranesi, and M. Riva, "Parameters optimization for improved dynamics of voltage multipliers for space," in *2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No.04CH37551)*, 2004, pp. 439–443. doi: 10.1109/PESC.2004.1355785.
[24] H. E. Tacca, "Single-switch two-output flyback-forward converter operation," *IEEE Transactions on Power Electronics*, vol. 13, no. 5, pp. 903–911, Sep. 1998, doi: 10.1109/63.712307.
[25] R. W. Erickson and D. Maksimovic, *Fundamentals of power electronics*. Springer Science & Business Media, 2007. doi: 10.1201/9780203913468.ch2.
[26] R. H. Ashique *et al.*, "A comparative analysis of soft switching techniques in reducing the energy loss and improving the soft switching range in power converters," *Electronics*, vol. 11, no. 7, p. 1062, Mar. 2022, doi: 10.3390/electronics11071062.
[27] T. A. Gonzalez, D. O. Mercuri, H. E. Tacca, and M. E. Pupareli, "Single-switch soft-switched boost power factor corrector for modular applications," *International Journal of Power Electronics and Drive Systems (IJPEDS)*, vol. 7, no. 2, p. 279, Jun. 2016, doi: 10.11591/ijpeds.v7.i2.pp279-293.

BIOGRAPHIES OF AUTHORS

Diego Alberto Fanego was born in Buenos Aires, Argentina, in 1985. He received the Engineer's degree in electronics from the University of Buenos Aires, Argentina, in 2016. Since 2013, he has been with the Faculty of Engineering of the University of Buenos Aires, Argentina, where he is currently head teaching assistant. He is currently working towards his Ph.D. degree in electronics engineering at the Drives, Traction and Power Control Laboratory (LABCATYP), in the latter. His current research interest include switching-mode power converters, the use of wide bandgap semiconductors in power converters and high voltage pulse generators. He can be contacted at email: dfanego@fi.uba.ar.

Orlando Silvio Sandini was born in Buenos Aires, Argentina, in 1981. He received the Engineer's degree in electronics from the University of Buenos Aires, Argentina, in 2021. In 2015 he began researching high voltage converters for electrostatic accelerators at the Drives, Traction and Power Control Laboratory (LABCATYP), which he concluded with his degree thesis. His current research interest include power converters and industrial electronics. He can be contacted at email: osandini@fi.uba.ar.

Hernán Emilio Tacca (S'92-M'93-S.M'20-L.S.M.'23) was born in 1954. He received the B.S. degree in electronics engineering in 1981 from the Universidad de Buenos Aires (UBA) and the M.S. degree in electrical engineering (D.E.A.) from the Lille University of Science and Technology, Villeneuve-d'Ascq, France, in 1988, and the Ph.D. degree in engineering from UBA, in 1998. He has been teaching and conducting research with the Faculty of Engineering, University of Buenos Aires, since 1983. He is currently a Full Professor with the Department of Electronics and is leading a laboratory devoted to power electronics and drives (Laboratorio de Control de Accionamientos Tracción y Potencia). His current research interests include power switching converters, magnetics designs for power electronics, power supplies, and motor drives. He can be contacted at email: htacca@fi.uba.ar.



Andrés Juan Kreiner graduated in Physics at the Universidad de Buenos Aires (1973) and obtained a Ph.D. in Natural Sciences at the Technical University of Munich (1978). In 1974 he joined CNEA, the National Atomic Energy Commission of Argentina, where he is currently Head of the Accelerator Technology and Applications Department. 30 years ago he began to work on the applications of nuclear techniques to various interdisciplinary fields. In 1994 he organized the interdisciplinary School of Science and Technology at the National University of San Martin becoming its first dean. Medical Physics was one of the careers introduced. For about 15 years now he and his group decided to pursue the ambitious goal of developing locally accelerator technology for Boron Neutron Capture Therapy and other applications. He is also full professor of physics at the National University of San Martin and superior investigator at CNEA and the National Research Council of Argentina. He can be contacted at email: andreskreiner@cnea.gob.ar.