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Design of 7-level cascade asymmetric multilevel inverter for renewable energy applications using FPGA

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ABSTRACT

The increasing focus on renewable energy has driven the need for efficient and reliable power converters. Multilevel inverters offer low harmonic distortion and high-quality output but often suffer from design complexity and excessive component count. This study presents the design and implementation of a 7-level cascaded asymmetric multilevel inverter optimized for renewable energy applications. The proposed topology utilizes a cascade structure with asymmetric DC voltage sources to generate seven voltage levels, providing a practical balance between performance and simplicity. The design was first validated through MATLAB/Simulink software to analyze circuit operation and evaluate the total harmonic distortion (THD) performance. Experimental evaluation was then conducted using a hardware prototype to verify simulation results. Without a filter, the THD from the simulation was 21.31%, while the experimental setup recorded a slightly higher value of 21.61%, indicating a marginal difference of 0.21%. With a filter, the simulation achieved a THD of 3.81%, whereas the experimental setup outperformed with a THD of 1.5%, showing a notable reduction of 2.31%. These findings confirm the proposed inverter's capability to deliver superior power quality and operational efficiency. The combination of simulation and experimental validation demonstrates the practicality and reliability of the 7-level cascade asymmetric multilevel inverter for renewable energy applications.

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1. INTRODUCTION

The demand for electricity has continuously increased in the era of globalization and the rapid growth of the industry. However, issues such as environmental pollution, resource depletion, and greenhouse gas emissions have been rising, which have contributed to climate change because of the dependence on fossil energy sources such as coal, natural gas, and oil. Renewable energy supplies such as solar and wind have become popular to reduce the negative impacts on the environment and ensure a continuous, sustainable energy supply.

The growing demand for energy-efficient and high-performance power electronic systems drives the continuous evolution of advanced multilevel inverter (MLI) topologies [1]-[3]. Conventional 2-level inverters often generate waveforms that can lead to high harmonic distortion, resulting in elevated harmonic contents that cause high power losses and interference in sensitive electronic equipment [4]. Various configurations of

Multilevel inverters have been introduced to overcome the high total harmonic distortion (THD) by producing an AC waveform that is close to a sinusoidal waveform [4]-[9]. The number of levels in the multilevel inverter significantly affects the THD by generating output waveforms that further closely approximate a pure sine wave. The most widely used topology in multilevel inverters is the cascaded H-bridge multilevel inverter (CHB-MLI) [5], [10]-[14], which offers several advantages, such as easier control, reduced switching frequency, multi-source capability, modular structure, and does not require additional balancing components. This configuration is especially favored in renewable energy applications [6], [15], where modularity, scalability, and improved power quality are essential for integrating sources like solar and wind into the grid.

The 7-level asymmetric cascade H-bridge MLI stands out due to its capability to deliver lower total harmonic distortion (THD), improved power quality, minimized switching losses, and enhanced voltage output characteristics. Despite these benefits, the design and implementation of asymmetric cascade multilevel inverters (ACMLIs) remain challenging. Key concerns include optimizing topologies to minimize the number of required switches [16], [17], simplifying control algorithms [18], [19], and effectively managing unequal voltage sources.

Field-programmable gate arrays (FPGAs) emerge as a compelling solution for addressing these challenges with their advantages, such as reconfigurable architecture, parallelism processing capabilities, and deterministic performance with high-speed operation, making them suitable for complex inverter control and management tasks. Previous research has shown that FPGAs have the ability to control and optimize the switching behavior of power electronic converters, as in AC-DC [20], [21], DC-DC [22]-[24], DC-AC [25], [26], and AC-AC [27]. However, even with basic H-bridge structures, high THD remains an issue, necessitating larger filters to meet the IEEE 519 standard for low-voltage applications, which limits THD to 5%. Excessive THD diminishes power quality and risks damaging sensitive electronic devices.

By adopting a 7-level cascade asymmetric MLI, this work aims to overcome these limitations. Compared to 5-level designs, the proposed inverter achieves higher voltage output quality, improved efficiency, and reduced voltage stress on components. The inclusion of two unequal voltage sources enhances the inverter's capability to produce a refined output with a smaller filter, thus lowering the THD percentage. Ensuring the THD remains within the acceptable range is critical for protecting electrical devices and maintaining reliable operation. This study presents an optimized design for a 7-level asymmetric cascade MLI, demonstrating its potential to address the key challenges in the field while delivering superior performance.

2. PROPOSED SYSTEM CONFIGURATION

Figure 1 illustrates the complete block diagram of the proposed system, which integrates an MLI powered by two asymmetric DC sources, specifically 2 V_{dc} and V_{dc}. This proposed configuration, with the appropriate controlled switching sequence of switches, generates the 7-level voltage waveform by strategically merging the output levels. The asymmetric design is selected to optimize power quality while reducing filter design complexity compared to conventional symmetric configurations.

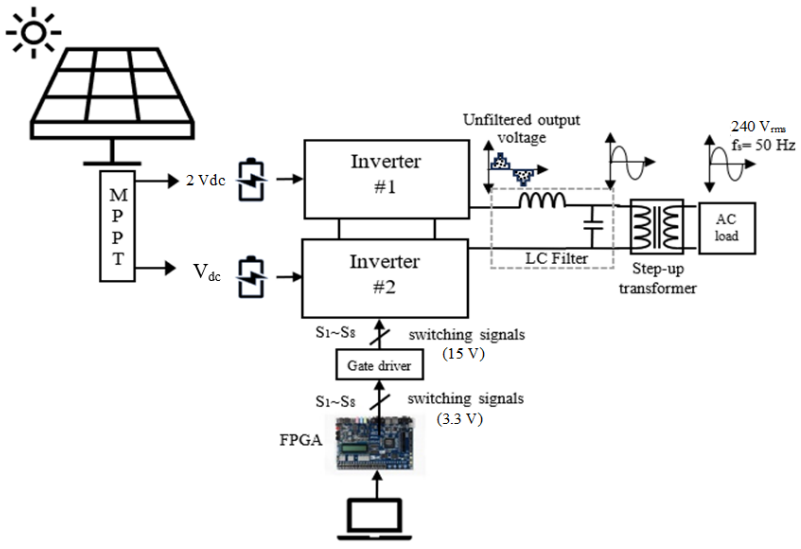


Figure 1. Proposed complete system configuration

The control logic for the inverter is implemented using an Intel Altera DE2-115 development board, which is based on the Cyclone II EP2C70 FPGA. The FPGA's reconfigurable architecture and parallel processing capabilities enable the precise governing of the switching patterns. The FPGA's output signals, initially at 3.3 V, are boosted to 15 V through a gate driver circuit. This ensure the switches are fully turned on to permit the current to flow from the drain to the source terminal under varying load conditions. LC filters suppress high-frequency noise and harmonics to refine the output waveform, resulting in a smoother AC signal.

After filtration, the output is passed through a step-up transformer to raise the voltage to 240 V_{ac}, making it compatible with standard grid-connected or standalone AC loads. The 7-level inverter configuration is designed to closely approximate an ideal sine wave, achieved through careful modulation of switching sequences. This approach reduces THD, minimizes the size of required filters, and enhances the system's efficiency. The proposed configuration represents a compact and efficient solution for renewable energy systems, delivering improved performance while maintaining simplicity in design and implementation.

3. OPERATION PRINCIPLES OF THE PROPOSED CONVERTER

Figure 2 shows a 7-level cascade asymmetric MLI circuit configuration. Meanwhile, Figure 3 shows the output voltage waveform with corresponding switching states. Each level corresponds to specific combinations of switches being turned on or off. The switches are controlled based on the desired output voltage level. Table 1 displays the switching sequence for the 7-level, 8-switch multilevel inverter. It shows the switching sequence from +18 V to -18 V; for 2 V_{dc}=12 V and V_{dc} = 6 V.

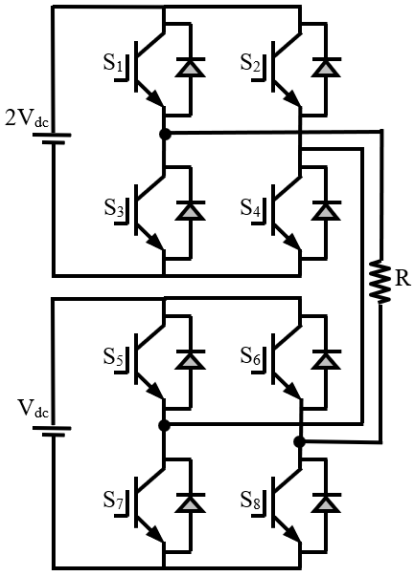


Figure 2. The 7-level cascade asymmetric MLI configuration

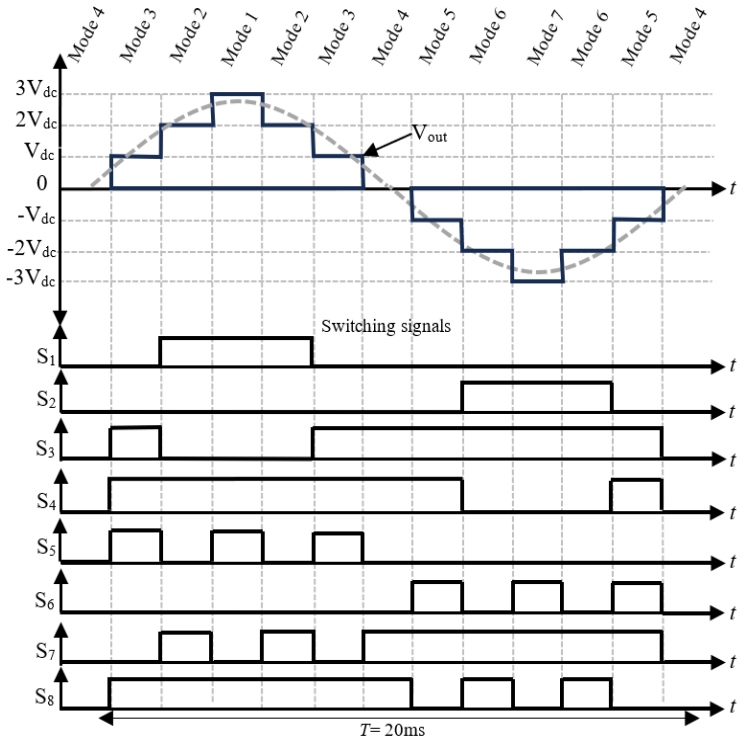


Figure 3. Switching states and corresponding output voltage (V_{out}) of 7-level cascade asymmetric MLI

Table 1. Switching sequence for 7-level 8 switch MLI

Mode	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	V_{dc}
Mode 1	1	0	0	1	1	0	0	1	+18
Mode 2	1	0	0	1	0	0	1	1	+12
Mode 3	0	0	1	1	1	0	0	1	+6
Mode 4	0	0	1	1	0	0	1	1	0
Mode 5	0	0	1	1	0	1	1	0	-6
Mode 6	0	1	1	0	0	0	1	1	-12
Mode 7	0	1	1	0	0	1	1	0	-18

4. OPERATION PRINCIPLES

The proposed operating mode at a steady state is divided into seven sub-modes, and the equivalent circuits for the corresponding mode of operation are presented in Figure 4, which can be explained as follows:

i) Mode 1 (18 V): Active switches, S_1, S_4, S_5, and S_8. Current flows through the switches S_1 and S_4 in the top inverter and S_5 and S_6 in the bottom inverter, combining the voltages from both sources. This mode represents the peak positive level of the inverter's operation and corresponds to the step in the 7-level output waveform.

$$V_{out} = 2\,V_{dc} + V_{dc} = 3\,V_{dc} \quad (1)$$

ii) Mode 2 (12 V): Active switches: S_1, S_4, S_7, and S_8. Current flows through S_1 and S_2 and bypasses the bottom source, resulting in an output voltage equal to 2 V_{dc} (12 V). This produces an intermediate positive voltage level of +12 V, representing the second step in the seven-level waveform.

$$V_{out} = 2\,V_{dc} \quad (2)$$

iii) Mode 3 (6 V): Active switches: S_3, S_4, S_5, and S_8. Current flows through S_3 and S_4, adding the bottom source (V_{dc}) to the circuit. During this mode, only the bottom DC source contributes to the output voltage. This generates an intermediate voltage of +6 V, corresponding to the third positive level of the inverter output.

$$V_{out} = V_{dc} \quad (3)$$

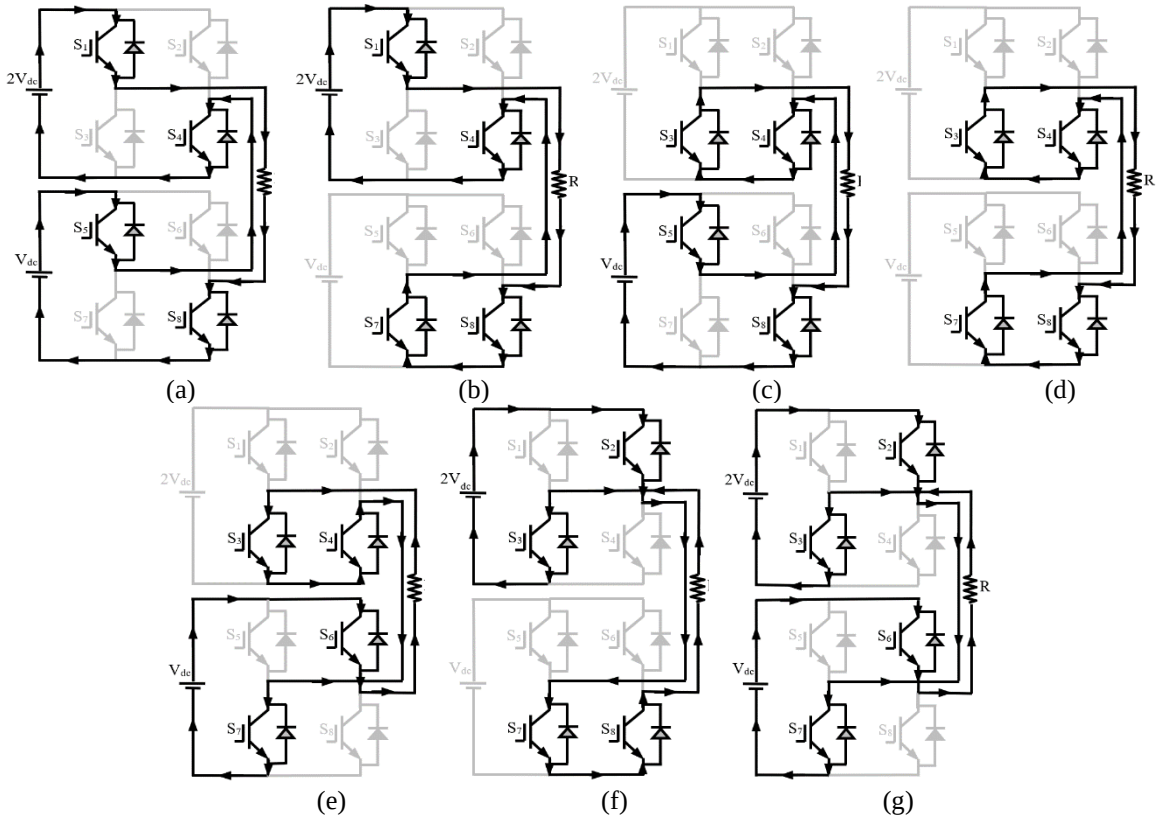


Figure 4. Steady state analysis for each mode (a) Mode 1:18 V, (b) Mode 2: 12 V, (c) Mode 3: 6 V, (d) Mode 4: 0 V, (e) Mode 5: -6 V, (f) Mode 6: -12 V, and (g) Mode 1: -18 V

iv) Mode 4 (0 V): Active switches: S_3, S_4, S_7, and S_8. The top and bottom sources are bypassed, resulting in no net voltage across the output terminal. This operating state corresponds to the zero-voltage level, which provides the transition between positive and negative steps, ensuring waveform symmetry.

$$V_{out} = 0 \quad (4)$$

v) Mode 5 (-6 V): Active switches: S_3, S_4, S_6, and S_7. Current flows through the inverted polarity of the bottom source (V_{dc}). Only the lower source is used, generating an output voltage of -6 V, which mirrors Mode 3 in the negative half cycle.

$$V_{out} = -V_{dc} \quad (5)$$

vi) Mode 6 (-12 V): Active switches: S_2, S_3, S_7, and S_8. Current flows through the inverted polarity of the top source (2 V_{dc}). This results in an output of -12 V, corresponding to the negative counterpart of Mode 2.

$$V_{out} = -2\,V_{dc} \quad (6)$$

vii) Mode 7 (-18 V): S_2, S_3, S_6, and S_7. Current flows through the inverted polarity of both sources (2 V_{dc} + V_{dc}), producing the maximum negative output voltage of -18 V. This mode represents the peak negative of the 7-level output waveform, completing the full symmetrical cycle.

$$V_{out} = -(2\,V_{dc} + V_{dc}) = -3\,V_{dc} \quad (7)$$

5. METHODOLOGY

This section details designing a 7-level cascade asymmetric MLI simulation using MATLAB/Simulink software, including component ratings and generating switching control via Quartus II software.

5.1. MATLAB/Simulink software

This stage focuses on modelling the proposed configuration using MATLAB/Simulink software. Parameters for every component are determined and assessed. Figure 5 illustrates the circuit design for this approach by using 8 MOSFETs and 2 DC sources. The PWM switching block generates the switching sequence for the MLI. The THD of the output waveform was recorded.

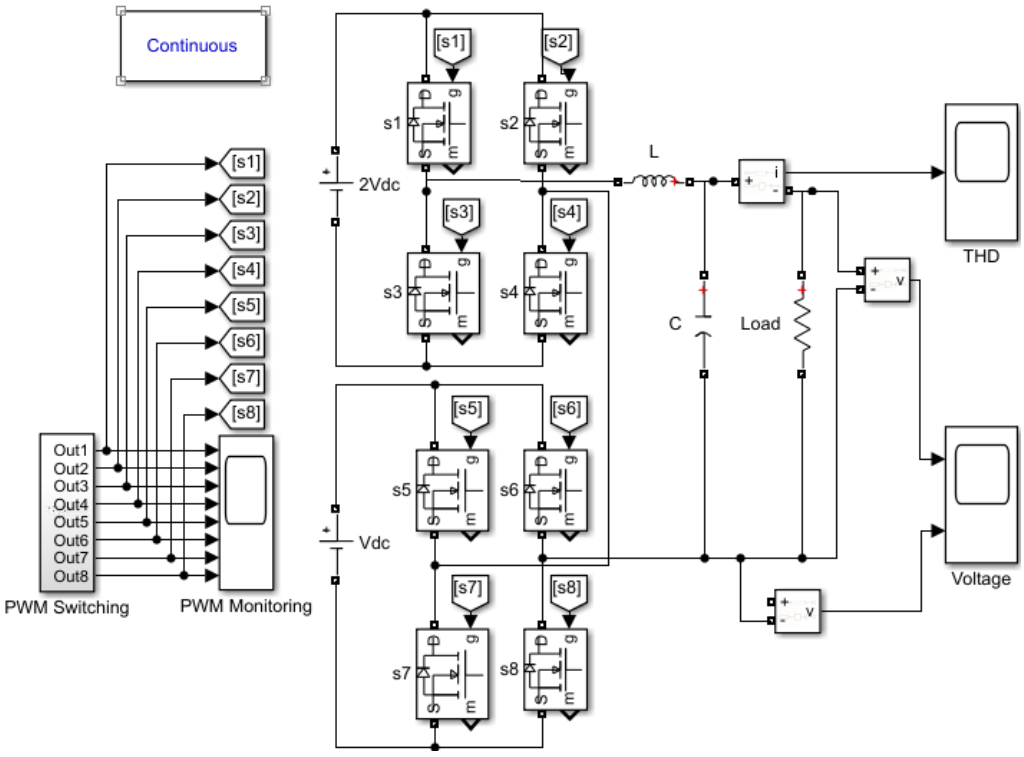


Figure 5. Simulation with MATLAB/Simulink software

5.2. Quartus II software

Figure 6 illustrates the switching design using Quartus II software. The proposed switching strategy was implemented using VHDL, utilizing combinational and sequential logic functions. The altpll is used for clock management, generating multiple clock outputs with different frequencies, spaces and duty cycles. Meanwhile, lpm_counter (predefined megafunction) is used to count pulses triggered from the altpll output clock to provide a 50 Hz output waveform. Both are parameterized megafunctions that can be configured using the Quartus IP catalogue. The lpm_counter is set to count from 0 to 20000, whereby each mode of operation equals ~1667 clock. The higher value of the counter will cause a more accurate output frequency and make it easy to adjust the transition between turning on and off the switches. The PLL manipulates the clock signal to generate the required frequencies. The counters and shift registers are likely used to implement timing, sequencing, and data transformation logic. The output signals are assigned to the corresponding dedicated general-purpose input-output (GPIO) connections.

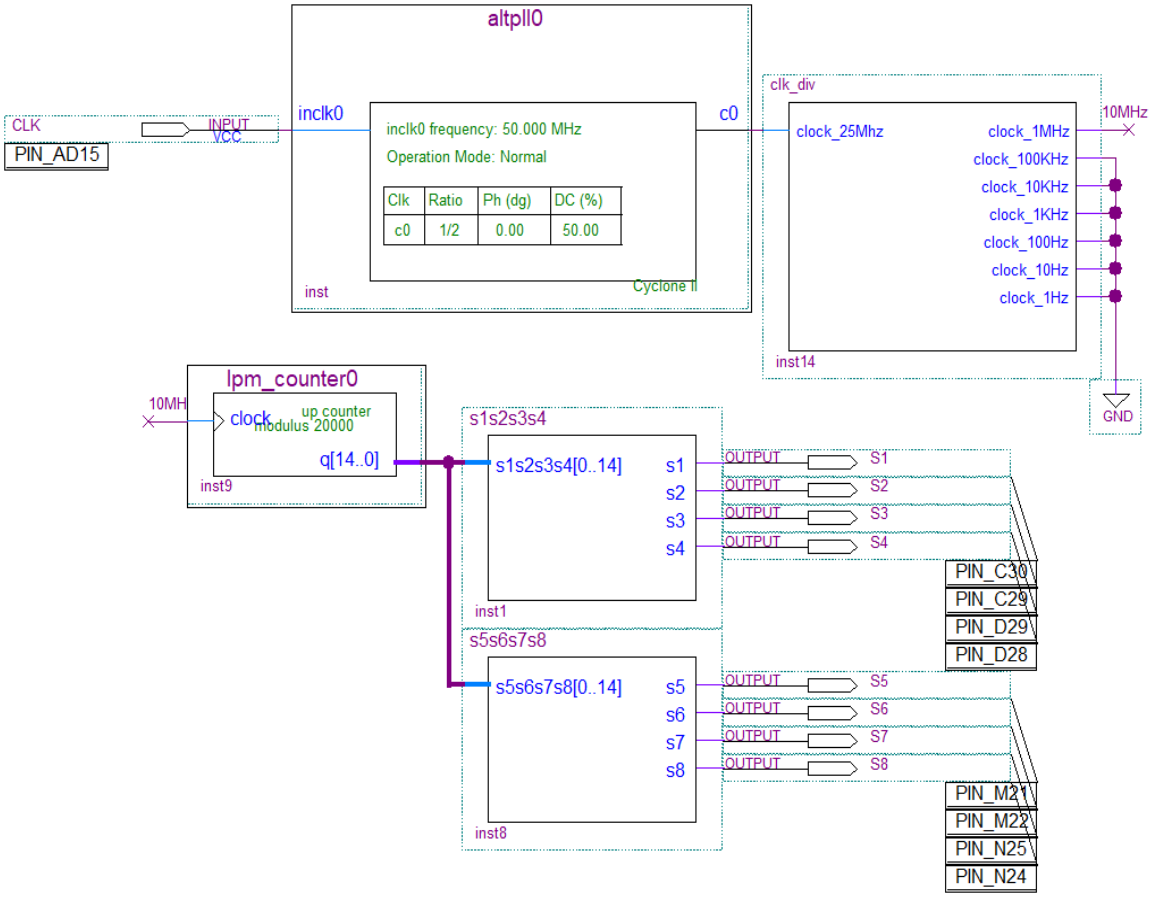


Figure 6. PWM switching design of 7-level cascade asymmetric MLI in Quartus II software

5.3. Hardware prototype

In Table 2, the quantity and rating of each component that is used in the 7-level cascade asymmetric MLI have been listed. The rating of the components was chosen based on the power rating. All component ratings are selected based on the design requirements for the 7-level cascade asymmetric MLI. Inductance and capacitance values of 22 mH and 220 µF are used for filtering the output waveform, smoothing out voltage ripples, and ensuring stable operation of the inverter. Figure 7 shows the complete experimental prototype. The equipment used in this experiment included a DC power supply, TDS3024B Digital Oscilloscope, multimeter, gate driver units, 120 V/10 A programmable DC power supply, 7-level cascade asymmetric MLI, and Intel Altera DE2-115.

Table 2. Specification, parameter, and rating for experimental prototype

Components/device	Rating
FPGA board	Intel Altera DE2-115
MOSFETs	IRFZ44N
Gate driver	5 V to 15 V
Battery 1	12 V_{dc}
Battery 2	6 V_{dc}
Inductor	22 mH
Capacitor	220 µF
Input voltage, 2 V_{dc}	12 V
Input voltage, V_{dc}	6 V
Output voltage, V_{out}	18 V
Output current, I_{out}	12 A
Output power, P_{out}	200 W

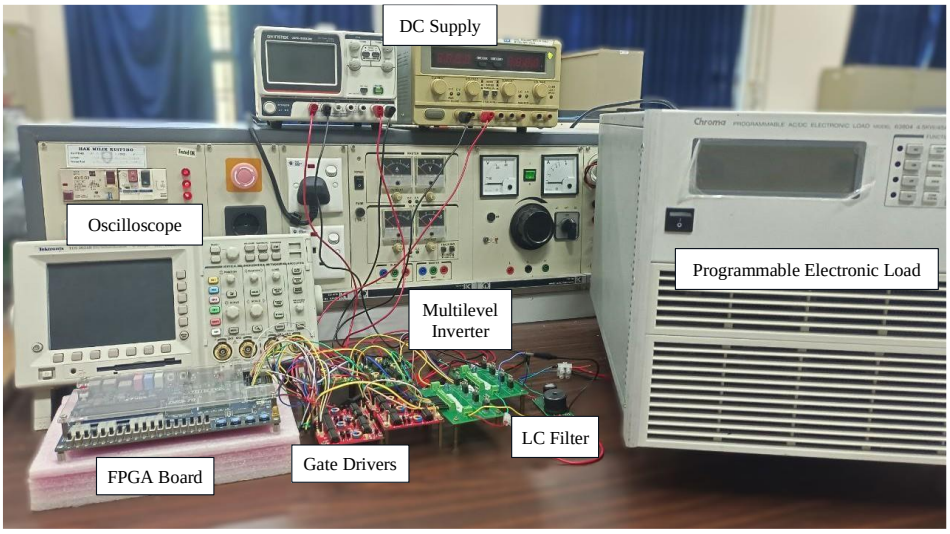


Figure 7. Experimental prototype

6. RESULT AND DISCUSSION

This section compares the 7-level cascade asymmetric MLI THD to evaluate the performance with and without the inclusion of filters in simulation and experimental results. Since the load is pure resistance, the THD for current and voltage will be equal.

6.1. Simulation result of 7-level cascade asymmetric MLI

The 7-level cascade asymmetric MLI is a power electronic converter that combines both independent DC inputs to produce a desired output voltage. Figure 8 shows the unfiltered and filtered output voltage waveform for a 7-level multilevel inverter (MLI). It also shows the inverter produces seven distinct voltage steps ranging from positive to negative symmetrically with an appropriate switching signal. The symmetrical output waveform indicates a balanced output, which is crucial for effective inverter operation. It also shows that the LC filter effectively smooths the stepped waveform. This demonstrates a significant reduction in harmonics and confirms that the chosen value of inductance and capacitance enhances the quality of the inverter output.

Figure 9(a) shows the simulation result for FFT analysis of the 7-level output without an LC filter, simulated using MATLAB/Simulink software. The fundamental frequency component at 50 Hz dominates the spectrum; however, a significant number of harmonic components still exist. The measured THD is 21.31%, exceeding the acceptable standard and indicating that the waveform still contains substantial non-fundamental content. The high THD value emphasizes the importance of employing a passive filter to attenuate the harmonic frequencies and improve the quality of the output voltage. Figure 9(b) illustrates the FFT analysis result of the filtered output voltage after the LC filter is applied. Compared to the unfiltered result, the higher-order harmonic components are significantly attenuated, resulting in a smoother output waveform. The measured THD of the filtered output voltage is 3.81%, demonstrating the LC filter's effectiveness in suppressing harmonics.

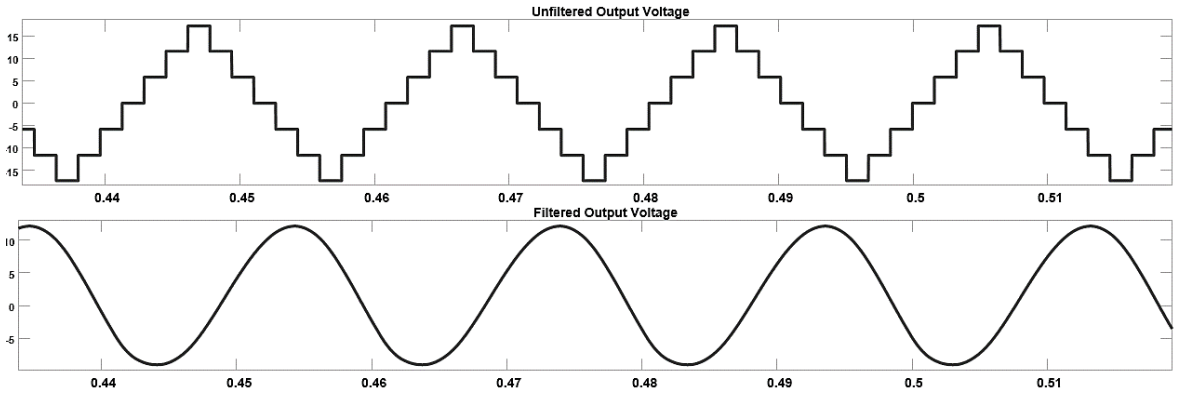
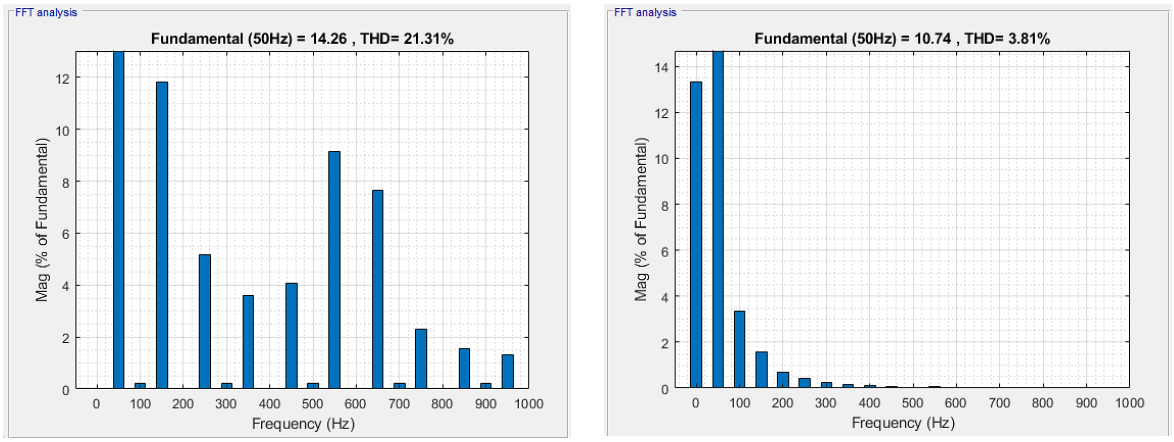


Figure 8. Simulation result of 7-level output voltage for unfiltered and filtered



(a) (b)

Figure 9. 7-level THD voltage result: (a) without and (b) with a filter in MATLAB/Simulink

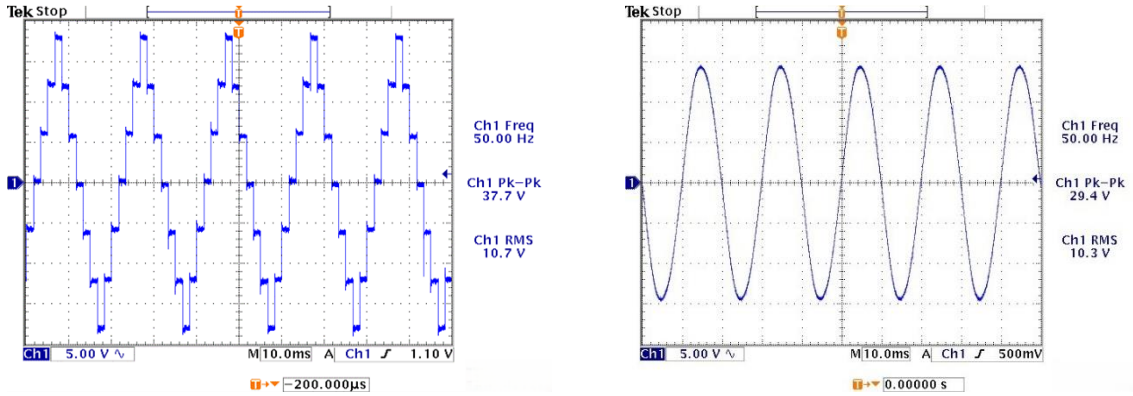
6.2. Experiment result of 7-level cascade asymmetric MLI

The THD for experimental analysis was measured using a programmable AD/DC electronic load by Chroma 68000. Figures 10(a) and 10(b) show the experimental peak-to-peak before and after applying a filter. In Figure 10(a), the unfiltered output exhibits distinct steps corresponding to the 7-level inverter topology, the same as the simulation result in Figure 8. The measured peak-to-peak voltage and RMS are 37.7 V and 10.3 V, respectively. Although the theoretical peak-to-peak voltage using 12 V and 6 V asymmetric sources is 36 V, the experimental result in Figure 10 shows a slightly higher value of 37.7 V. This discrepancy may be attributed to tolerances in the DC sources, switching transients, or measurements overshoot captured by the oscilloscope. Figure 10(b) shows the filtered output, where the waveform becomes sinusoidal with a slightly reduced peak-to-peak voltage of 29.4 V but a higher RMS voltage of 10.3 V. The effective harmonic suppression by the filter has improved power quality. The experimental results validate the simulation analysis, demonstrating the importance of filtering in multilevel inverters. Meanwhile, the measured THD without and with the filter was 21.61% and 1.5%, respectively.

Figure 11(a) illustrates the experimental result of a 7-level FFT without a filter, which gets an amplitude value of 67.58 dB. The vertical axis represents the magnitude of the harmonic components in decibels (dB). Higher peaks indicate stronger harmonic components. The horizontal axis shows the frequency components of the output waveform. The fundamental frequency is visible at 50 Hz. For the harmonic spectrum, the tallest spike corresponds to the fundamental frequency (50 Hz), while the smaller peaks appearing at harmonic frequencies such as 150 Hz, 250 Hz, and 350 Hz represent higher-order harmonic components with reduced magnitudes. These harmonics are caused by the inverter's switching operation and the absence of a filter.

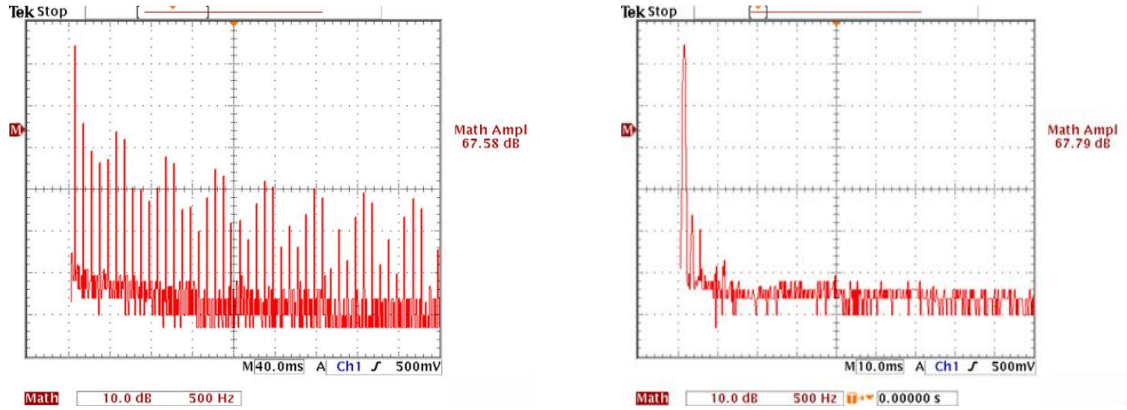
Figure 11(b) illustrates the result of a 7-level FFT with the application of a filter, which gets an amplitude value of 67.79 dB. It is similar to the unfiltered case; the tallest spike represents the fundamental frequency component at 50 Hz. Compared to the unfiltered result, the higher-frequency harmonics like

150 Hz, 250 Hz, and subsequent harmonics are significantly attenuated. The harmonic spikes that were prominent in the unfiltered spectrum are now much smaller, indicating the filter's effectiveness in suppressing harmonics. The overall spectrum shows a cleaner signal, with the fundamental frequency dominating and reduced distortion components.



(a) (b)

Figure 10. Experiment result of 7-level peak to peak with (a) unfiltered and (b) filtered output voltage



(a) (b)

Figure 11. Experimental FFT results for (a) unfiltered output voltage and (b) filtered output voltage

7. DISCUSSION

The values of the THD observed in the simulation without a filter which was approximately 21.4%. The THD measured during the experimental setup without a filter was 21.61%, which means experimental results are higher by 0.21% compared to simulation results. The THD observed in the simulation with a filter was approximately 3.81%. The THD measured during the experimental setup a filter was 1.5%, which means experimental results are lower by 2.31% compared to simulation results. The difference in THD between simulation and experimental results is likely due to dead-time effects, non-ideal components, filter design, and switching losses. Switching devices use dead-time to stop complementary switches in the inverter from conducting at the same time. This can distort the output waveform and increase THD. In simulations, components like switches, diodes, and capacitors are often considered ideal, while real components have imperfections such as parasitic capacitance, resistance, and switching losses.

Variations in THD may result from differences between the theoretical design utilized in the simulation and the actual implementation of the filter. Experimental filters might not perform exactly as modelled. Switching devices in the experimental setup may result in losses, which cannot be accounted for in simulations, and can affect the harmonic content of the output. Previous work often achieved THD reduction by inserting or using complex control algorithms. The FPGA implementation provides precise timing control and reduces the switching overlap, which results in THD reduction.

The performance of the proposed FPGA-controlled modulation was compared with two established methods: Sinusoidal PWM (SPWM) and phase-disposition PWM (PDPWM). These conventional techniques are known for their straightforward implementation, but in most 7-level inverters, their THD remains around

3 to 5%. In this paper, the sequential switching pattern performed by the FPGA produced an experimental THD of 1.5%, displaying a noticeably smoother waveform. Because the pulse timing was generated directly in the prototype, each device switched less times per cycle roughly 30% less than in SPWM thereby significantly reducing switching losses and thermal stress.

To examine device reliability, the drain–source voltage V_{DS} of each MOSFET was recorded with a Tektronix TDS3024B oscilloscope under rated load. The measured peak stresses were 12 V for the upper bridge and 6 V for the lower bridge, equal to their corresponding DC-source voltages. From the observation, no overshoot beyond these limits, confirming safe-operating conditions. Voltage stress remained symmetric over positive and negative half-cycles, specifying that the asymmetric modulation and gating sequence maintained balanced sharing among all switches throughout the cycle.

8. CONCLUSION

In this paper, the 7-level cascaded asymmetric MLI represents a significant leap in power electronics. The proposed system is able to produce an output waveform that is almost sinusoidal with fewer harmonics and better efficiency. The THD obtained from simulation was reduced from 21.31% (unfiltered) to 3.81% (filtered), while the experimental THD was reduced from 21.61% to 1.5%, confirming the effectiveness of the proposed inverter design. Due to this, it can be used as an energy source in renewable energy systems such as electric vehicle drives as well as in medium-voltage industrial drives. However, implementation of CHB-MLI also presents some challenges, such as difficulty associated with control strategies and the need for several isolated DC sources. Future work may focus on implementing advanced modulation techniques, such as selective harmonic elimination or AI-based modulation, to further reduce the THD.

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AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

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C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

The authors confirm that the data supporting the findings of this study are available within the article and its figures. Additional details can be obtained from the corresponding author upon request.

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