

Performance evaluation of cascaded H-bridge multilevel inverter with hybrid controller based PV system

C. Dinakaran¹, T. Padmavathi²

¹Department of Electrical and Electronics Engineering, GITAM School of Technology, GITAM (Deemed to be University), Visakhapatnam, India

²Department of Electrical, Electronics and Communication Engineering, GITAM School of Technology, GITAM (Deemed to be University), Visakhapatnam, India

Article Info

Article history:

Received Aug 9, 2025

Revised Oct 18, 2025

Accepted Dec 11, 2025

Keywords:

Ant-lion optimization cascaded
Fuzzy logic controller
H-bridge multilevel inverter
Maximum power point tracking
Pulse width modulation
Single phase inverter
Solar photovoltaic
Total harmonic distortion

ABSTRACT

Rising concerns about global warming demand renewable growth, which in turn needs efficient converter topologies to integrate renewable power. This article presents a single-phase, nine-level inverter to improve the performance of non-conventional power systems. Here, the foremost aim, based on the advanced techniques, to diminish the representation of switches with sources has been executed. This influences the appended preservation of generating energy against non-conventional power resources. This conquest during the statistic of switch refuses every switching loss, counting the cardinal-like driving circuit that details a minimization within convolution based on supervision track, consequently depreciating the disturbances with scope. The proposed inverter has a diminished production voltage total harmonic distortion (THD) with an ideal power factor. The cascaded H-bridge multilevel inverter (CHBMLI) topology is intended for the proposed method in support of the design, added ant-lion optimization (ALO) tuned fuzzy logic controller (FLC) methodical assessment for compensation. The presented arrangement is refined to diminish the energy losses, just as it is unified among reproducing systems that boost the smooth output voltage with reduced %THD. In addition, contraction in energy losses and amplification in efficiency are accomplished by producing transitional levels for the level elaboration system. Indeed, every completion related to the suggested arrangement is evaluated over the reproduction of MATLAB/Simulink and PROTEUS applications.

This is an open access article under the [CC BY-SA](https://creativecommons.org/licenses/by-sa/4.0/) license.



Corresponding Author:

C. Dinakaran

Research Scholar, Department of Electrical and Electronics Engineering

GITAM School of Technology, GITAM (Deemed to be University)

Visakhapatnam, Andhra Pradesh, India

Email: dina4karan@gmail.com

1. INTRODUCTION

The cascaded H-bridge multilevel inverter (CHBMLI) topology subsists based on H-shaped bridges coupled in sequence among each alternative, with respective H-shaped bridges carrying their own separate DC voltage source. Consequently, the alternative DC source can remain powered in distinction to solar photovoltaic (SPV) systems appropriate for the indicated nature of topology, including accuracy and expansion [1]. By adopting the CHBMLI topology, the ultimate energy assessment and higher output voltage levels can also be produced as per the essential [2].

Solar PV and wind are equitable, a minor illustration of the frequent non-conventional resources. SPV cells generally transform SPV power into electrical energy [3]. SPV power transformation systems

consist of converters, including a control unit, to allocate the extent based on the energy the SPV cell can generate. To improve the performance of SPV cells, the forward-end phase DC-DC converter must be personalized to adapt to energy fluctuations with augmented productivity [4].

Multilevel Inverters can be specified within three essential associations relative to the statistics of DC connections used in modern inverters, NPC, FC, and CHB endure every ultimate universal topologies in the industry to date [5]. Though CHBMLI subsists, extended convenience is considered when SPV utilization is considered, considering that a specific SPV array is an isolated DC source [6]. A CHBMLI compromise persists in support of the utmost schedule. The maximum power point tracking (MPPT) approach among DC-DC converters remains widely used to attain huge potential and enhance the SPV arrangement's efficiency, as illustrated in Figure 1.

An MPPT has been designed to track the MPPT's successive variation in the illumination or temperature. Absolute MPPT executives are worn amidst SPV panel constraints at respective DC links to decide the complication about a sectional shading position of panels in SPV pattern [7] suitable to shading acquired with static as well as effective substance, comparable to trees, buildings, birds, aggregate dirt over panels, as a substitute cloud. SPV arrangement associated with an array among a DC-DC expansion converter through a limitation of its ultimate voltage through computing a bypass diode laterally by the entire SPV unit [8], consequently avoiding circumstance development [9]. Though this access causes several crests in the energy of the SPV arrangement, restraining the operation of the MPPT approach also leaves researchers focused on illuminating innovative performance [10]. The fuzzy logic controller (FLC), a dissimilar traditional executive, doesn't desire a mathematical representation of the arrangement being composed. Despite a perception that the arrangement, including the restraint demands, remains significant.

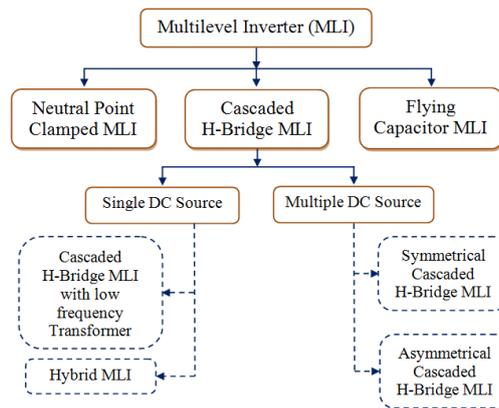


Figure 1. Multilevel inverter topology

Multi-SPV arrays, among an interleaved advanced converter, condense every ripple current, enhance power quality, adapt DC system voltage, and consequently permit considering the operation of a self-reliant MPPT supervision [11] in support of each SPV array to acquire immense production energy along with better efficiency [12]. Modernized power systems employ CHBMLI as their low THD with electromagnetic interference (EMI), with their capability to augment power quality with rating necessity [13]. Correlated to typical two-level inverters that adopt tremendous switching frequency pulse width modulation (PWM), a CHBMLI carries considerable preference [14]. One of the imperative preferences of an MLI is the limited intensity of the filter, along with its low expenditure related to a two-level inverter. A CHBMLI diminishes THD connected through two-level inverters by adopting different DC connections [15]. Alternative recognition carries reduced switching frequency, minor charge, over-switching acceleration, and diminished voltage switches compared to the consistently enforced two-level inverters, ensuring diminished switching expense, tremendous voltage formation, depressed EMI levels, and acceptable energy nature [16].

To boost power conditions due to effective attainment based on exhausting systems, CHBMLI directly examines technical results [17], [18]. Due to their inferior THD output waveform, they also controlled appliance valuation. CHBMLI produces an accomplished and immense voltage strategy [19]. SPV utilization, wind turbine connections, and fuel cells can be combined with multilevel converters [20], [21]. Due to the operation, the PWM supervision method CHBMLI typically impacts their efficiency and power

ratings [22], [23]. Over the past few decades, indefinite modules have carried expected varied MLI topologies for fewer switches [24].

An investigation has been conducted on dynamic automation accumulating efficiency through CHBMLI [25]. The advanced arrangement can operate in a stand-alone and load-integrated mode [26], [27]. The significant recognition of the expected sequence is the blocking voltage based on the entire switches endure distinct along with fewer than the absolute voltage as a few switches also the essential global switches with expert intention survive less, assist as this whole modern minimization of losses, expanding the efficiency moreover superior nature based on output as well as its extent persist modest as a consequence it remains competitive correlate through the traditional CHBMLI. Here, the simulation obtains exhaust for nine levels with the advice of MATLAB/Simulink.

2. PROPOSED TOPOLOGY

The designed 1-φ, 9-level inverter persists over the 7-level inverter. It constitutes a 1-φ traditional CHBMLI, with three bidirectional switches including a capacitor voltage segment created over C_a , C_b , C_c , & C_d within activities presented in Figure 2. The CHBMLI topology ensures compensation of minor power switches and power diodes, along with a reduction of the capacitor compared to the traditional inverters. The enhanced converter, i.e., DC/DC, correlates with SPV and load.

The energy produced through the inverter is conveyed to the energy complex, so the adequacy load is relatively low. The DC/DC advanced converter is appropriate for every SPV array, taking a more depressed energy than the load voltage. Immense DC voltages are desired to facilitate the energy stream from the SPV arrays toward the load. A filter was worn to filter the current delivered to the load adopting inductance (L_f) and practically accomplished THD from simulation results as indicated in Table 1. Convenient inverter switching can achieve nine output voltage levels (V_{dc} , $3V_{dc}/4$, $V_{dc}/2$, $V_{dc}/4$, 0 , $-V_{dc}$, $-3V_{dc}/4$, $-V_{dc}/2$, $-V_{dc}/4$) against the DC source.

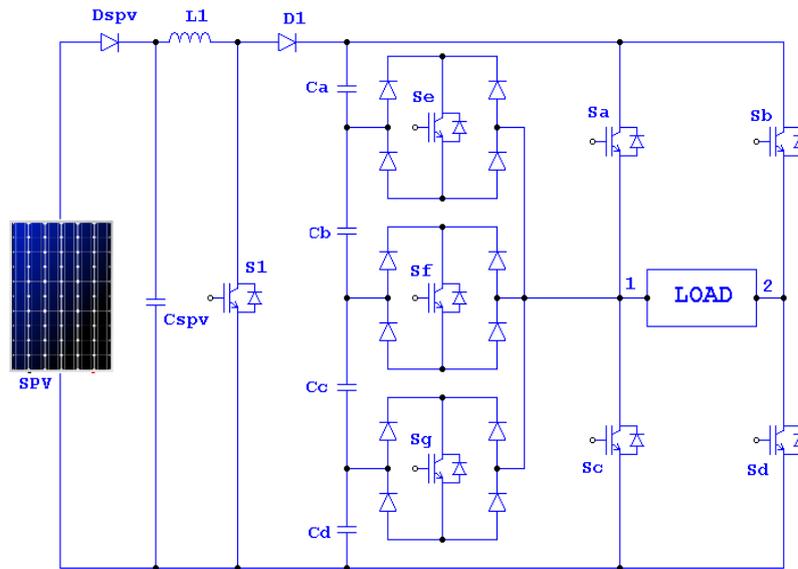


Figure 2. Prospective 1-φ 9-level inverter being SPV arrangement

Table 1. The output voltage corresponds to the switches' ON-OFF position

V_o	S_a	S_b	S_c	S_d	S_e	S_f	S_g
V_{dc}	√	-	-	√	-	-	-
$3V_{dc}/4$	-	-	-	√	√	-	-
$V_{dc}/2$	-	-	-	√	-	√	-
$V_{dc}/4$	-	-	-	√	-	-	√
0	-	-	√	√	-	-	-
0*	√	√	-	-	-	-	-
$-V_{dc}/4$	-	√	-	-	√	-	-
$-V_{dc}/2$	-	√	-	-	-	√	-
$-3V_{dc}/4$	-	√	-	-	-	-	√
$-V_{dc}$	-	√	√	-	-	-	-

3. SPV ARRANGEMENT AND DC-DC CONVERTER BY MPPT TECHNIQUE

To boost the achievement of the SPV structure and acquire tremendous energy, the SPV panel remains connected to a DC-DC converter through MPPT automation that performs an extensive role during SPV operation by adjusting the production voltage based on the SPV array. Performance based on the MPPT executive is the essential recognition of a DC-DC converter enhancement variation. Accordingly, a DC-DC expansion converter by MPPT automation prevails in the indicated effort to produce the optimal voltage, the suggested MLI. Furthermore, it yields the ultimate energy against the SPV pattern passing through the altered cumulative delivery MPPT approach. Different conductance is among the most widely used MPPT techniques, including adopting a fluctuating step size.

4. MODES OF PROCESS

It consists of a single-phase traditional CHBMLI, three bidirectional switches among a capacitor voltage divider produced with C_a , C_b , C_c , and C_d , as shown in Figure 3. The updated CHBMLI topology is substantially more beneficial than alternative topologies, i.e., limited energy switches, biased diodes, and limited capacitors as inverters, concerning the corresponding statistic of levels. SPV pattern remains associated with every inverter with a DC/DC advanced converter.

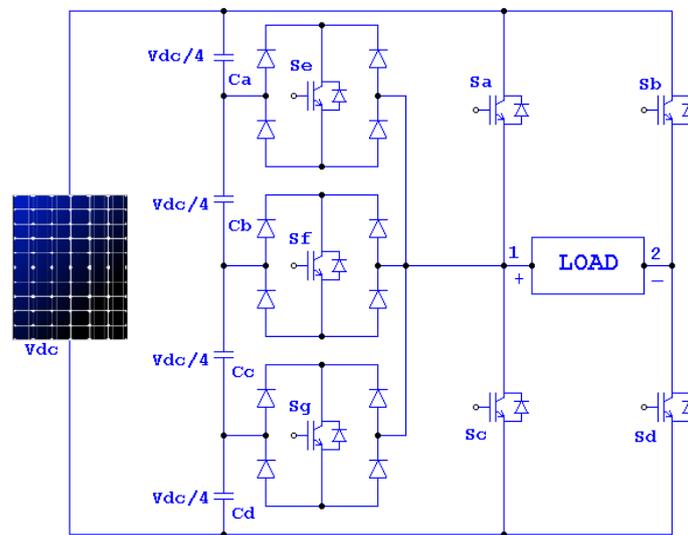


Figure 3. Nine-level inverter for switching sequence

Energy composed through the inverter is held to be conveyed to the load. A DC/DC advanced converter is essential, considering the SPV design takes a voltage reduced to the 1- ϕ voltage. Immense DC bus voltages are imperative for producing specific energy flows against the SPV pattern toward loads. The filter is designed to adopt L and C to bring pure sine waves and, consequently, is inclined to AC loads. The considered inverter's processes can persist in nine switching states.

Power switching attributed to the inverter can achieve nine output voltage levels (V_{dc} , $3V_{dc}/4$, $V_{dc}/2$, $V_{dc}/4$, 0 , $-V_{dc}$, $-3V_{dc}/4$, $-V_{dc}/2$, $-V_{dc}/4$) against the DC supply voltage. The novel topology inverters process can be split into nine switching circumstances.

The appropriate nine levels of production voltage remain induced as follows.

- Ultimate +Ve output Voltage (V_{dc}): S_a is against merged the load +Ve incurable over V_{dc} , including S_d remains approaching involved the load -Ve incurable over the ground. Integrated, that composed switch has vanished. The voltage energized over the load is incurable V_{dc} .
- Three-fourths +Ve output Voltage ($3V_{dc}/4$): The bi-directional control S_e is ON, involving the load +Ve incurable over V_{dc} , and S_d is ON, almost applied the load -Ve incurable over the ground. The integrated other composed switch has vanished. The voltage energized over the load destructive is ($3V_{dc}/4$).
- Half of the +Ve production Voltage ($V_{dc}/2$): The bi-directional switch S_f persists for involving the load +Ve destructive over V_{dc} , including S_d is ON, almost involving the load -Ve incurable over the ground. Integrated that the composed switch remains absent. The voltage energized over the load is incurable $V_{dc}/2$.

- One-fourth of the +Ve production Voltage ($V_{dc}/4$): The bi-directional switch S_g is ON, and almost every load +Ve incurable along with S_d is ON, practically applying the limitation -Ve incurable to ground. Integrated different composed switches remain OFF the energy adapted near the load fatal is $V_{dc}/4$.
- Zero output Voltage (0 & 0*): The designated steady state can prevail over binary switching arrangements. Switches S_c and S_d are ON (or) S_a , and S_b remains ON, with the other complete switch absent. The incurable "12" endures a short circuit also. Moreover, the voltage energized toward the inductive load remains zero.
- One-fourth -Ve output Voltage ($-V_{dc}/4$): The bi-directional switch S_e is ON, associating the load +Ve incurable. Also, S_b is ON against the load -Ve incurable to V_{dc} . Natural alternative composed switches endure OFF every energy adapted near the incurable load $-V_{dc}/4$.
- Half of the -Ve production Voltage ($-V_{dc}/2$): The switch S_b is ON, almost involved the load +Ve incurable over V_{dc} , including the bi-directional control S_f is ON, involving the load -Ve terminal over the ground. Integrated alternative composed switches have vanished. The voltage energized over the capacity is $-V_{dc}/2$.
- Three-fourths -Ve output Voltage ($-3V_{dc}/4$): The bi-directional switch S_g is ON, associating the load +Ve incurable along with S_b is ON, associating the load -Ve incurable to ground. Integrated different composed controls are OFF, and the voltage adapted through the load incurable is $-3V_{dc}/4$.
- Maximum -Ve output Voltage ($-V_{dc}$): S_b is ON, associating the load -Ve incurable to V_{dc} along with S_c is ON, associating the load +Ve fatal through the ground. Perfect alternative composed switches are OFF, and the voltage is adapted to the load is $-V_{dc}$.

Table 1 shows the switching arrangement commencing the nine output voltage levels ($V_{dc}, \frac{3V_{dc}}{4}, \frac{V_{dc}}{2}, \frac{V_{dc}}{4}, 0, \frac{-V_{dc}}{4}, \frac{-V_{dc}}{2}, \frac{-3V_{dc}}{4}, -V_{dc}$) among switching arrangements considering a single-phase nine-level inverter as presented in Figure 4.

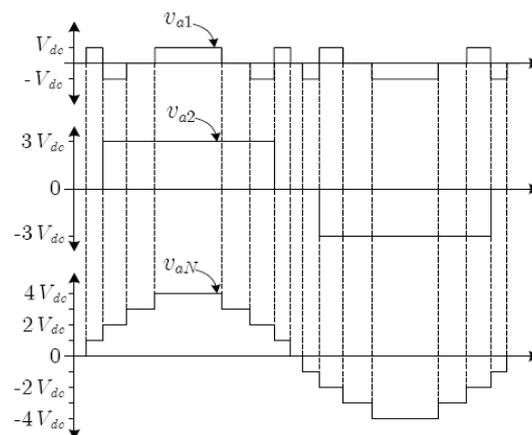


Figure 4. Switching arrangement for single phase nine level inverter

5. CLOSED-LOOP CONTROL SYSTEM

The supervision arrangement constitutes an MPPT supervisor, a DC voltage producer, and an inverter supervisor, as demonstrated in Figure 5. Based on the indicated sequence, the intention is essentially to achieve the ultimate volume of power together against SPV to load by diminishing THD. An innovative algorithm that draws inspiration from nature was introduced by Mirjalili [21]. The ALO imitates the way that ant lions hunt in the wild. An ant lion larva excavates a cone-shaped hole in the sand by moving in a circle and expelling sand with its enormous jaw. The larva digs the trap and then hides beneath the cone's base to wait for insects to fall into the hole and become trapped. Since the cone's edge is so sharp, insects can easily fall to the bottom of the trap. The ant lion starts to catch its prey as soon as it realizes it is in the trap. After that, it gets sucked up by the ground and eaten. In order to make room for the next hunt, ant lions dump the leftover prey outside the pit after eating it.

Here, a hybrid technique, an ALO-tuned fuzzy rule base structure, is adopted in the MPPT approach for its many networks. It systematically presents an ALO-fuzzy rule observer structure as exposed in Figure 6. The SPV maximum voltage, along with production energy, correlates with a particular preceding FRB algorithm. If the efficacy is growing P_{limit} , the performing approach activity near $P_{spv} \geq P_{limit}$ FRB coordination is extended in a similar guidance. Otherwise, in later revolutions, $P_{spv} < P_{limit}$ the guiding desire is transposed.

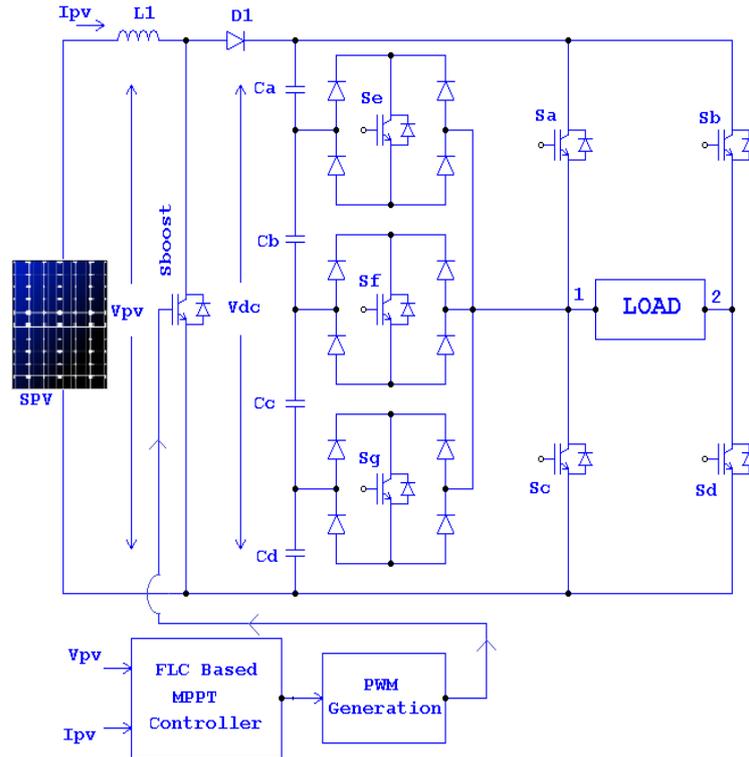


Figure 5. Nine-level inverter for closed-loop restraint algorithm



Figure 6. The fuzzy rule viewer is intended for a closed-loop system

FRB arrangement is exhausted in the DC-DC advanced converter. In essence, the ultimate harvest energy of MPPT is accomplished against the duty cycle responsibility. As the DC power V_{dc} prevailed adapted in 9-level inverter, the production utilities of SPV variation situated scheduled duty cycle transformation. SPV-associated DC/DC advanced converters with load-over surge diverters are the certainty of an integrated arrangement. The input connection of SPV (I_{SPV} , V_{SPV}) is inclined to MPPT among the PWM

advanced converters as shown in Figure 7. The input source is V_{dc} & V_{dcref} inclined to the FRB arrangement. Measure the productivity voltages of SPV along with MPPT employing a trial-and-error mechanism. Indeed, the output voltage is V_{dc} & V_{dc}^* controlled by the inverter over the gating pulses of switches ($S_a - S_g$) with feed toward the load through the filter.

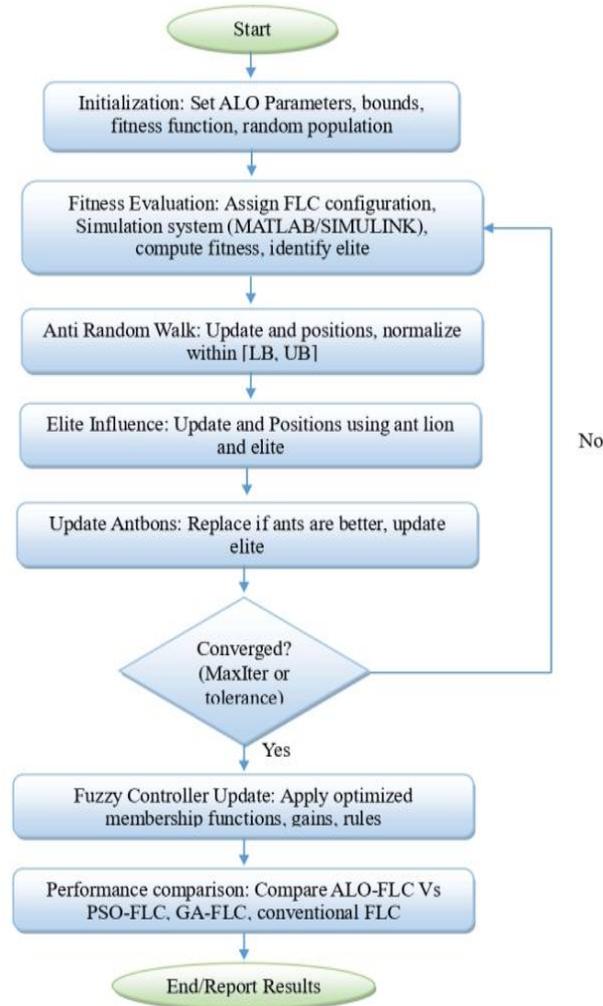


Figure 7. Fuzzy rule viewer is intended for a closed-loop system

6. RESULTS AND DISCUSSION

6.1. Simulation result

The designed technique was previously proven with simulation outcomes in Figures 8 to 14. This representative has been furnished with MATLAB/Simulink circumstances by the SIMPOWER system toolbox. The MATLAB/Simulink-based CHB nine-level inverter controlled with an ALO-fuzzy MPPT system effectively integrates hybrid optimization and intelligent control for photovoltaic power regulation. The cascaded H-bridge topology generates nine distinct voltage levels with reduced switching stress, while the fuzzy-based MPPT enhanced by the ant lion optimizer adapts efficiently to environmental changes to ensure maximum power extraction. The PWM subsystem produces multi-carrier signals that synthesize a near-sinusoidal output, achieving substantial THD reduction from 7.77% to 4.25% comparison THD table indicated in Table 2. This hybrid control approach demonstrates superior power quality and dynamic performance over conventional controllers, and its modular structure allows straightforward scalability for higher voltage applications. Future work can explore FPGA-based real-time deployment and AI-enhanced optimization for adaptive THD minimization in renewable grid systems.

Table 2. Identification of CHBMLI

Voltage levels	No. of switches recommended	% THD with ALO-fuzzy based MPPT controller	% THD without ALO-fuzzy based MPPT controller
Five	Five	12.36	25.39
Seven	Six	9.54	18.67
Nine	Seven	4.25	7.77

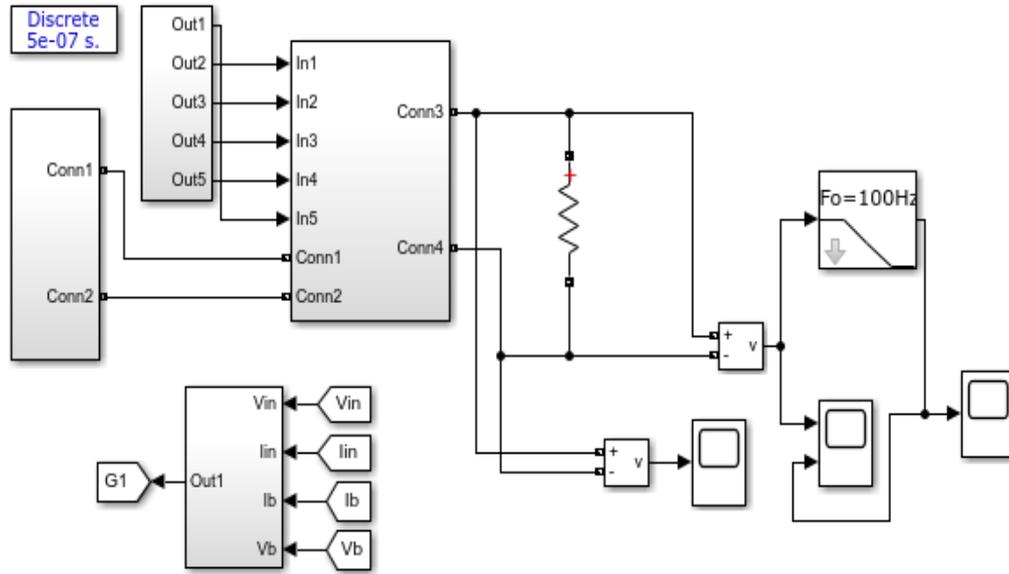


Figure 8. Simulation circuit for CHB nine-level inverter

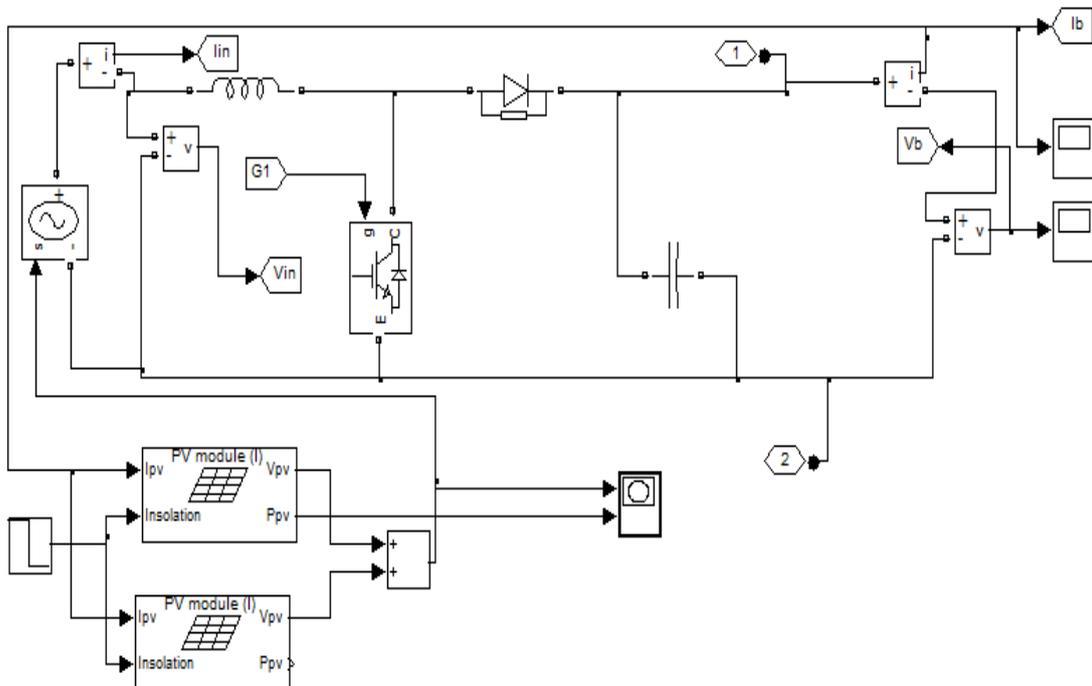


Figure 9. Sub circuit for MPPT advanced controller

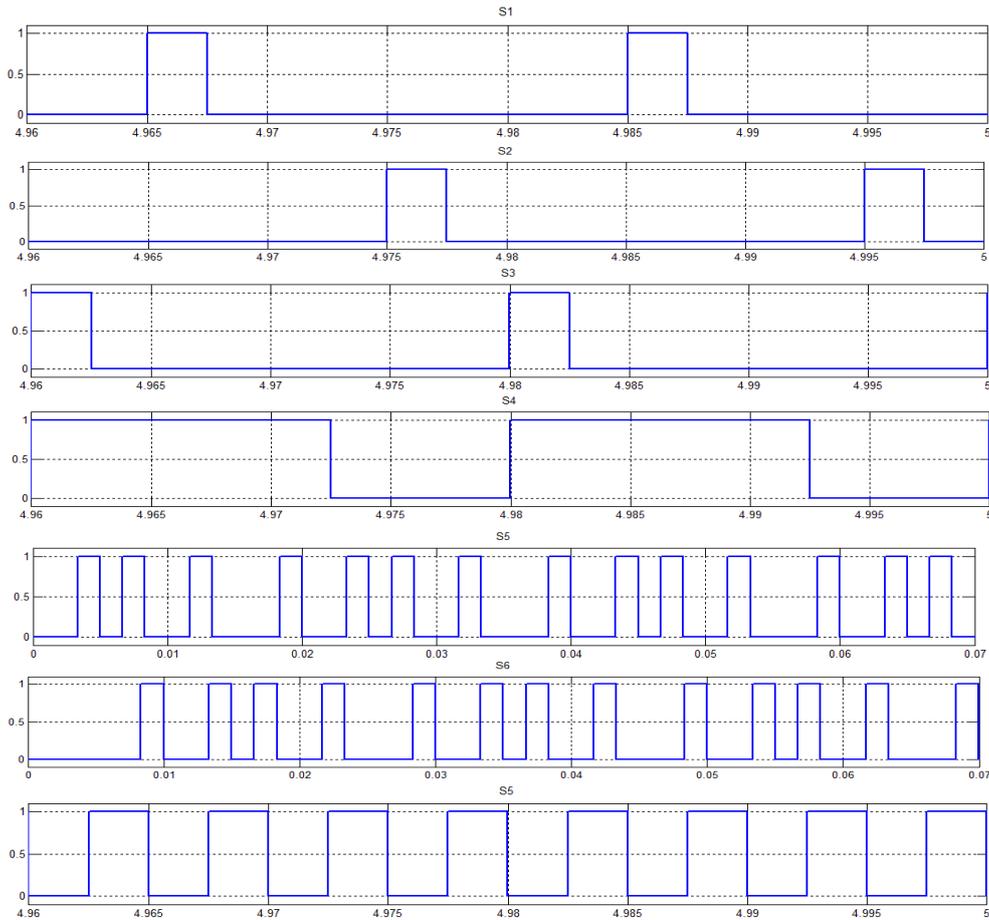


Figure 10. PWM signal being a CHB nine-level inverter

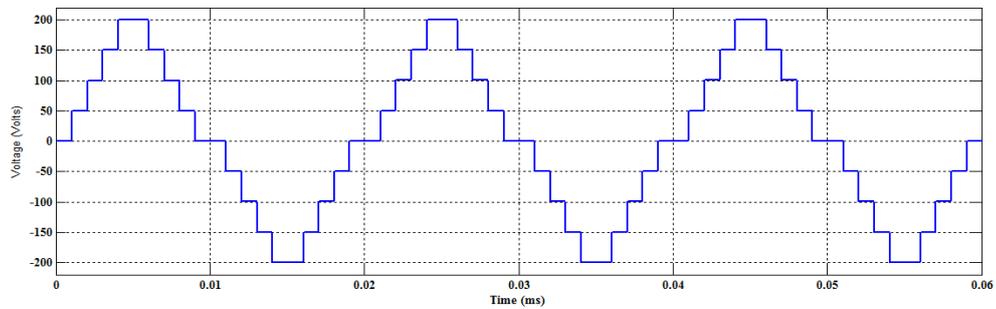


Figure 11. The production voltage of the CHB nine-level inverter

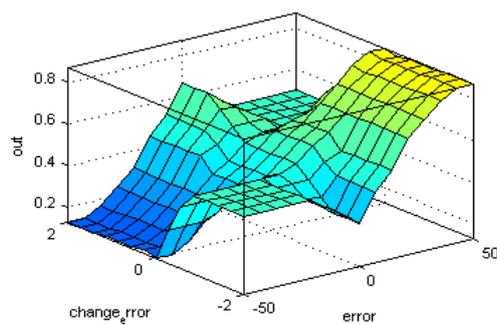


Figure 12. Surface viewer of fuzzy-based MPPT

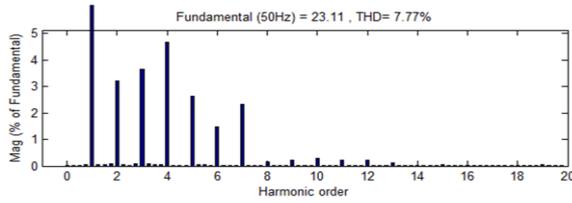


Figure 13. THD for CHB 9-level inverter without ALO-fuzzy

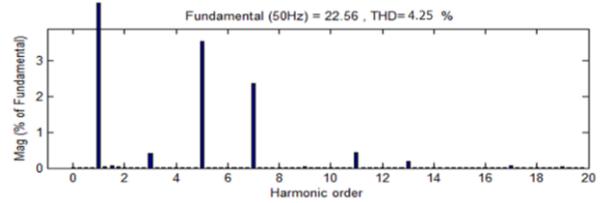


Figure 14. THD for CHB 9-level inverter with ALO-fuzzy

6.2. PROTEUS representation

Proteus is particularly attributed to the ultimate outstanding simulators. It can survive and reproduce essentially without exception in stimulating fields. It is accessible near the utility considering the GUI, which acts appropriately relevant to the prototype board in the process represented in Figures 15 to 17. Furthermore, it can be worn to model printed circuit boards. The future scope of current research focuses on two aspects. One is to extend the topologies' performance for higher levels and performance evaluation with different hybrid optimization techniques, which leads to further improving the harmonic profile, i.e., reduction in %THD of voltage within IEEE standards. The second aspect is to design a hardware model to validate the proposed system using DSP based controller with a hybrid optimization technique.

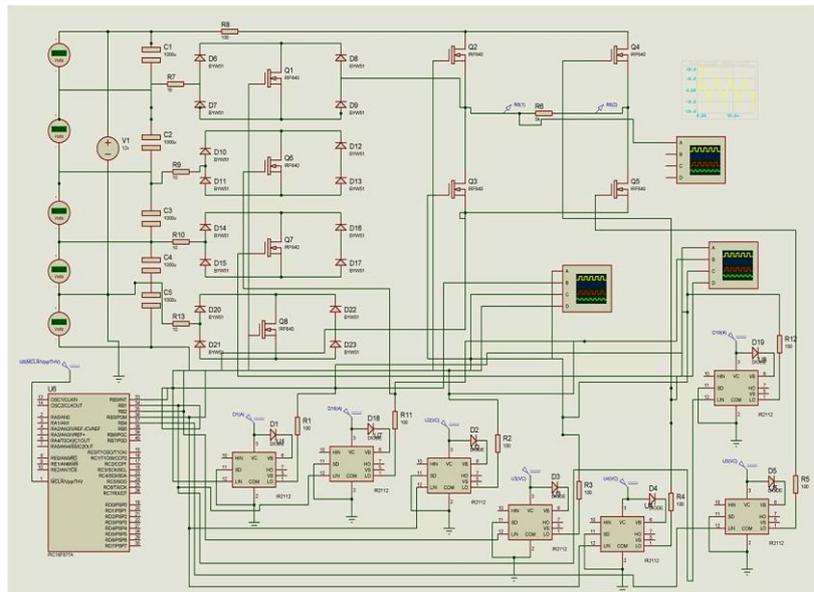


Figure 15. Expansion of nine-level CHBMLI in PROTEUS software



Figure 16. Output pulse of CHB nine-level inverter

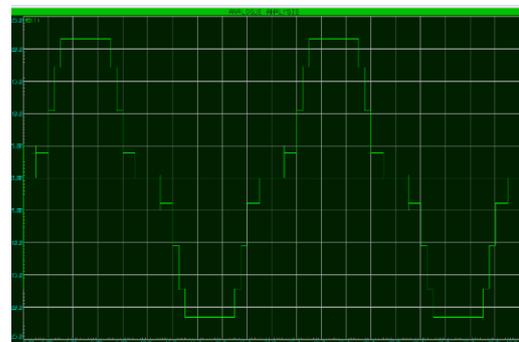


Figure 17. Output voltage of CHB nine-level inverter

7. CONCLUSION

In the present work, we conferred a nine-level CHBMLI among seven switches advanced with imported through the design of the integrated circuits in MATLAB/SIMULINK reproduction with an effective, fair stepped nine-level waveform. The proposed model is straightforward in appearance, along with a condensed quantity of apparatus correlated to typical symmetric and asymmetric topologies. The designed 9-level CHBMLI declined THD through an adequate standard and achieved 4.25% THD compared to the traditional model illustrated in the research. Hence, the proposed power inverter endeavors an innovative explanation considering an extensive range of utilization, such as non-conventional power propagation systems to facilitate the desired % THD in voltage along with depressed voltage stresses, although enduring reduced switch enumeration. In particular, SPV connections necessitate a lot of isolated SPV panels in an array to achieve immense energy. % THD in voltage is within IEEE standards in 9-level CHB inverter compared to the 7-level, along with 5-level inverter topologies, persists as a dominating topology for solar PV inverter with ALO tuned fuzzy-based MPPT. Finally, MATLAB/SIMULINK and PROTEUS Software supports the dominant performance of proposed 9-level inverter.

FUNDING INFORMATION

Authors state no funding involved.

AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
C. Dinakaran	✓	✓	✓	✓	✓	✓		✓	✓	✓				✓
T. Padmavathi		✓				✓		✓	✓	✓	✓	✓		

C : Conceptualization

M : Methodology

So : Software

Va : Validation

Fo : Formal analysis

I : Investigation

R : Resources

D : Data Curation

O : Writing - Original Draft

E : Writing - Review & Editing

Vi : Visualization

Su : Supervision

P : Project administration

Fu : Funding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

Data availability is not applicable to this paper as no new data were created or analyzed in this study.

REFERENCES

- [1] C. Bharatiraja, K. Lakshmikhandan, M. S. Kamalesh, D. Rajasekaran, and B. Twala, "A non-isolated high-gain dc to dc converter connected multi-level inverter for photo-voltaic energy sources," *Journal of Applied Science and Engineering*, vol. 24, no. 3, pp. 415–422, 2021, doi: 10.6180/jase.202106_24(3).0017.
- [2] Q. Huang, A. Q. Huang, R. Yu, P. Liu, and W. Yu, "High-efficiency and high-density single-phase dual-mode cascaded buck-boost multilevel transformerless PV inverter with GaN AC switches," *IEEE Transactions on Power Electronics*, vol. 34, no. 8, pp. 7474–7488, 2019, doi: 10.1109/TPEL.2018.2878586.
- [3] A. Lashab *et al.*, "Cascaded multilevel PV inverter with improved harmonic performance during power imbalance between power cells," *IEEE Transactions on Industry Applications*, vol. 56, no. 3, pp. 2788–2798, May 2020, doi: 10.1109/TIA.2020.2978164.
- [4] A. Lewicki, C. Odeh, and M. Morawiec, "Space vector pulsewidth modulation strategy for multilevel cascaded H-bridge inverter with DC-Link voltage balancing ability," *IEEE Transactions on Industrial Electronics*, vol. 70, no. 2, 2023, doi: 10.1109/TIE.2022.3158005.
- [5] A. Sheir and V. K. Sood, "Cascaded modular converter with reduced output voltage ripple," in *2019 IEEE Electrical Power and Energy Conference (EPEC)*, Oct. 2019, pp. 1–7. doi: 10.1109/EPEC47565.2019.9074787.
- [6] S. Suroso and T. Noguchi, "A single-phase multilevel current-source converter using H-Bridge and DC current modules," *International Journal of Power Electronics and Drive Systems (IJPEDS)*, vol. 4, no. 2, Jun. 2014, doi: 10.11591/ijpeds.v4i2.5603.
- [7] C. Dhanamjayulu, D. Prasad, S. Padmanaban, P. K. Maroti, J. B. Holm-Nielsen, and F. Blaabjerg, "Design and implementation of seventeen level inverter with reduced components," *IEEE Access*, vol. 9, pp. 16746–16760, 2021, doi: 10.1109/ACCESS.2021.3054001.
- [8] A. K. Pradhan, S. K. Kar, M. K. Mohanty, and N. Behra, "Design and simulation of cascaded and hybrid multilevel inverter with reduced number of semiconductor switches," *International Journal of Ambient Energy*, vol. 42, no. 8, pp. 950–960, Jun. 2021, doi: 10.1080/01430750.2019.1583127.
- [9] T. V. V. S. Lakshmi, N. George, S. Umashankar, and D. P. Kothari, "Cascaded seven level inverter with reduced number of switches using level shifting PWM technique," *Proceedings of 2013 International Conference on Power, Energy and Control, ICPEC 2013*, pp. 676–680, 2013, doi: 10.1109/ICPEC.2013.6527742.

- [10] M. D. Siddique, S. Mekhilef, N. M. Shah, A. Sarwar, and M. A. Memon, "A new single-phase cascaded multilevel inverter topology with reduced number of switches and voltage stress," *International Transactions on Electrical Energy Systems*, vol. 30, no. 2, 2020, doi: 10.1002/2050-7038.12191.
- [11] S. H. L. Majareh, F. Sedaghati, M. Hosseinpour, and S. R. Mousavi-Aghdam, "Design, analysis and implementation of a generalised topology for multilevel inverters with reduced circuit devices," *IET Power Electronics*, vol. 12, no. 14, pp. 3724–3731, 2019, doi: 10.1049/iet-pel.2019.0405.
- [12] Z. Sarwer, M. D. Siddique, A. Iqbal, A. Sarwar, and S. Mekhilef, "An improved asymmetrical multilevel inverter topology with reduced semiconductor device count," *International Transactions on Electrical Energy Systems*, vol. 30, no. 11, 2020, doi: 10.1002/2050-7038.12587.
- [13] S. Majumdar, B. Mahato, and K. C. Jana, "Analysis of most optimal multi-unit multi-level inverter having minimum components and lower standing voltage," *IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India)*, vol. 38, no. 5, pp. 520–536, 2021, doi: 10.1080/02564602.2020.1799874.
- [14] A. Seifi, M. Hosseinpour, and A. Dejamkhooy, "A switch-source cell-based cascaded multilevel inverter topology with minimum number of power electronics components," *Transactions of the Institute of Measurement and Control*, vol. 43, no. 5, pp. 1212–1225, 2021, doi: 10.1177/0142331220974137.
- [15] X. Wang *et al.*, "A half-bridge IGBT drive and protection circuit in dielectric barrier discharge power supply," *Circuit World*, vol. 48, no. 4, pp. 586–593, 2022, doi: 10.1108/CW-11-2020-0329.
- [16] K. Muralikumar and P. Ponnambalam, "Analysis of cascaded multilevel inverter with a reduced number of switches for reduction of total harmonic distortion," *IETE Journal of Research*, vol. 69, no. 1, pp. 295–308, 2023, doi: 10.1080/03772063.2020.1819450.
- [17] A. Salem, H. Van Khang, I. N. Jiya, and K. G. Robbersmyr, "Hybrid three-phase transformer-based multilevel inverter with reduced component count," *IEEE Access*, vol. 10, pp. 47754–47763, 2022, doi: 10.1109/ACCESS.2022.3171849.
- [18] S. S. Lee, "Single-stage switched-capacitor module (S 3 CM) topology for cascaded multilevel inverter," *IEEE Transactions on Power Electronics*, vol. 33, no. 10, pp. 8204–8207, Oct. 2018, doi: 10.1109/TPEL.2018.2805685.
- [19] M. D. Siddique, A. Iqbal, M. A. Memon, and S. Mekhilef, "A new configurable topology for multilevel inverter with reduced switching components," *IEEE Access*, vol. 8, pp. 188726–188741, 2020, doi: 10.1109/ACCESS.2020.3030951.
- [20] R. K. Kumawat and D. K. Palwalia, "A comprehensive analysis of reduced switch count multilevel inverter," *Australian Journal of Electrical and Electronics Engineering*, vol. 17, no. 1, pp. 13–27, Jan. 2020, doi: 10.1080/1448837X.2019.1693884.
- [21] S. Mirjalili, "The ant lion optimizer," *Advances in Engineering Software*, vol. 83, 2015, doi: 10.1016/j.advengsoft.2015.01.010.
- [22] M. Petronijević, J. Mitić, M. Vuković, N. Plemić, and A. Miljković, "The ant lion optimization algorithm for flexible process planning," *Journal of Production Engineering*, vol. 18, no. 2, pp. 65–68, 2015.
- [23] D. Prasad and C. Dhanamjayulu, "Solar PV-fed multilevel inverter with series compensator for power quality improvement in grid-connected systems," *IEEE Access*, vol. 10, pp. 81203–81219, 2022, doi: 10.1109/ACCESS.2022.3196174.
- [24] K. K. Mahto, P. K. Pal, P. Das, S. Mittal, and B. Mahato, "A new design of multilevel inverter based on T-type symmetrical and asymmetrical DC sources," *Iranian Journal of Science and Technology - Transactions of Electrical Engineering*, vol. 47, no. 2, pp. 639–657, 2023, doi: 10.1007/s40998-022-00568-4.
- [25] A. Hassan, X. Yang, and W. Chen, "A multi-cell 21-level hybrid multilevel inverter synthesizes a reduced number of components with voltage boosting property," *IEEE Access*, vol. 8, pp. 224439–224451, 2020, doi: 10.1109/ACCESS.2020.3044268.
- [26] A. D. E. Dutra, M. A. Vitorino, and M. B. D. R. Correa, "A survey on multilevel rectifiers with reduced switch count," *IEEE Access*, vol. 11, pp. 56098–56141, 2023, doi: 10.1109/ACCESS.2023.3283215.
- [27] D. Kang, S. Badawi, Z. Ni, A. H. Abuelnaga, M. Narimani, and N. R. Zargari, "Review of reduced switch-count power cells for regenerative cascaded H-Bridge motor drives," *IEEE Access*, vol. 10, pp. 82944–82963, 2022, doi: 10.1109/ACCESS.2022.3196659.

BIOGRAPHIES OF AUTHORS



C. Dinakaran    is a research scholar in the Electrical and Electronics Engineering Department at the GITAM School of Technology, GITAM (Deemed to be University), Visakhapatnam. He received his B.Tech. and M.Tech. degrees in Electrical and Electronics Engineering from Jawaharlal Nehru Technology University, Anantapur, Andhra Pradesh, India, in 2011 and 2014, respectively. His research interests include the field of power electronics applications in renewable energy systems, power electronic drives, and machines. He can be contacted at email: dina4karan@gmail.com.



T. Padmavathi    is an assistant professor in the Department of Electrical, Electronics, and Communication Engineering, GITAM School of Technology, GITAM (Deemed to be University), Visakhapatnam. She received her Ph.D. in Electrical and Electronics Engineering from Jawaharlal Nehru Technology University, Kakinada, Andhra Pradesh, India. She completed M.E and B.E. degrees from GITAM, Visakhapatnam. She has over 20 years of academic experience. Her areas of interest include power quality, electrical distribution systems, and power electronic applications in renewable energy systems. She is a certified Behavior and Mentoring Analyst (CBMA). She can be contacted at email: ptadi@gitam.edu.