International Journal of Power Electronics and Drive System (IJPEDS)
Vol. 17, No. 2, June 2026, pp. 1118~1129
ISSN: 2088-8694, DOI: 10.11591/ijpeds.v17.i2.pp1118-1129

High step-up interleaved multilevel hybrid boost converter with switched-capacitor multiplier

Andi M. Nur Putra[1,2], Adrianti[1], Muhammad Imran Hamid[1]
[1]Department of Electrical Engineering, Faculty of Engineering, Universitas Andalas, Padang, Indonesia
[2]Department of Electrical Engineering, Faculty of Engineering, Institut Teknologi Padang, Padang, Indonesia

Article Info

Article history:

Received Sep 30, 2025
Revised Mar 30, 2026
Accepted Apr 23, 2026

Keywords:

DC-DC power converter
High gain
Interleaved converter
Multilevel converter
Switched-capacitor
Voltage multiplier

ABSTRACT

The global integration of renewable energy sources like photovoltaics requires efficient high-step-up DC-DC converters. Conventional boost converters exhibit inherent limitations in achieving high voltage gain efficiently, particularly under high duty cycle operation, where switching losses, device stress, and output voltage ripple become significant. This paper proposes a novel hybrid DC-DC converter that integrates a four-phase interleaved input stage with a five-level switched-capacitor (SC) multiplier network. The proposed topology introduces a modular and structurally decoupled architecture, in which current conditioning and voltage boosting functions are independently realized. This enables scalable voltage gain through modular expansion without requiring extreme duty cycles or additional magnetic components. The interleaved stage reduces input current ripple and improves current sharing, while the multilevel SC network provides a high voltage conversion ratio and balanced voltage stress across components. Comprehensive simulations using PSIM software validate the converter's performance. With a 25 V input, the proposed converter achieves an output voltage of approximately 250 V (gain of 10), a high efficiency of 95.2%, output voltage ripple below 2%, and balanced capacitor voltages. The results confirm that the proposed converter offers an efficient, scalable, and high-performance solution for high step-up applications.

Corresponding Author:

Adrianti
Department of Electrical Engineering, Faculty of Engineering, Universitas Andalas
Limau Manis St., Limau Manis, Pauh, Padang, West Sumatra 25163, Indonesia
Email: adrianti@eng.unand.ac.id

1. INTRODUCTION

The increasing penetration of renewable energy systems, particularly photovoltaic (PV) generation, has intensified the need for efficient and reliable power conversion technologies [1], [2]. One of the primary challenges in integrating low-voltage sources, such as PV modules, into high-voltage DC systems is the requirement for substantial voltage amplification. Although conventional boost converters are widely adopted, their voltage gain capability is inherently constrained, especially at high duty cycles where efficiency degradation becomes unavoidable [3]-[5]. Additionally, these converters often experience high voltages on semiconductor devices and significant output voltage ripples, making them unsuitable for modern high-voltage boost applications [6].

To overcome these limitations, various advanced topologies have been explored. Converters based on connected inductors and switched-capacitor (SC) networks can achieve high gain, but often at the cost of complex magnetic designs, high component voltages, and increased current ripple [7], [8]. Quadratic and multilevel boost converters offer higher gain through staged operation, but this causes cumulative voltage

increases on the switches and a decrease in overall efficiency [9]-[11]. Interleaved boost converter techniques effectively reduce input current ripples and improve heat distribution by utilizing multiple phases [12]. In contrast, multilevel topologies distribute stress voltage across multiple components and can achieve multiplicative gain, improving efficiency and power quality [13], [14]. Recent studies have proposed hybrid high step-up converters by combining these concepts. For example, the topology in [15] integrates a boost converter with a voltage multiplier and SC cells to achieve high voltage gain and efficiency. However, its structure remains configuration dependent and is not inherently designed for modular scalability, limiting flexibility in extending the voltage gain. Similarly, the converter in [16] enhances voltage gain using hybrid switched inductor and capacitor techniques, but it operates with simultaneously driven switches and does not incorporate interleaved operation or a modular multilevel structure. As a result, scalability and current sharing capability remain limited.

This work introduces a hybrid DC-DC converter topology that combines a multiphase interleaved front end with a modular switched-capacitor network. Unlike conventional hybrid configurations, the proposed design explicitly separates current shaping and voltage boosting functions, enabling independent optimization of both processes. The interleaved stage ensures low input current ripple and better thermal management by distributing power among phases, while the multilevel SC network enables high voltage conversion ratios without requiring extreme duty cycles or complex connected inductors. This configuration effectively reduces the voltage stress on each switching device, enabling the use of lower-rated and more efficient semiconductor components. Unlike conventional hybrid converters that merely combine interleaved structures with switched-capacitor networks, the proposed topology introduces a structurally decoupled architecture in which current conditioning and voltage boosting functions are independently realized through the interleaved stage and modular switched-capacitor network, respectively. This separation enables true scalability of the voltage gain through modular expansion without affecting the input stage operation or requiring additional magnetic components. In contrast to existing interleaved SC-based converters, which typically exhibit fixed configurations and limited scalability, the proposed design allows flexible adjustment of the voltage gain by simply extending the number of capacitor modules, while maintaining balanced current sharing and reduced ripple characteristics.

The main innovation in this research lies in its modular hybrid architecture, designed to achieve high step-up voltage gain with high efficiency and low output voltage ripple. The proposed converter addresses the identified research gap by offering a scalable solution that optimizes the trade-off between performance, component count, and control simplicity. Although this study focuses on simulation-based validation to establish the feasibility and performance characteristics of the proposed topology, the design has been developed with practical implementation considerations. Experimental validation using a hardware prototype will be conducted in future work to further confirm its applicability under real operating conditions.

2. PROPOSED TOPOLOGY AND THEORETICAL ANALYSIS

2.1. Fundamental concept and operating principle of the hybrid modular topology

The proposed topology represents a synergistic integration between an interleaved converter and a multilevel SC network, designed to overcome the limitations of conventional boost converters in high voltage step-up applications. This approach leverages the complementary advantages of both structures, where the interleaved stage improves current characteristics, while the switched-capacitor network enables high voltage gain through voltage stacking.

As shown in Figure 1(a), the interleaved configuration employs four identical phases operated with a 90° phase shift. Each phase consists of an inductor (L_1–L_4), a MOSFET switch (S_1–S_4), and a diode (D_1–D_4). This structure provides two key advantages: first, even distribution of the input current across all phases, which reduces thermal stress on semiconductor components; second, a significant ripple cancellation effect on the input current due to phase-shifted operation. In the 4-phase configuration, the theoretical input current ripple can be reduced by up to 75% compared to a single-phase converter [17], [18].

Figure 1(b) illustrates the SC network, which operates as a voltage multiplier based on the principle of staged voltage addition. The network consists of five capacitors (C_1–C_5) arranged in a modular structure. Each capacitor is alternately charged and discharged through a controlled switching sequence, resulting in a gradual buildup of voltage across the capacitor stack. The output voltage is therefore formed by the summation of the voltages across each capacitor in the SC network [19], [20]. This modular arrangement also enables even distribution of voltage stress across components, allowing the use of lower voltage-rated devices.

The integration of these two subsystems into a hybrid topology is shown in Figure 2, which illustrates the detailed circuit configuration of the proposed hybrid interleaved multilevel boost converter with a switched-capacitor network. In this configuration, the interleaved stage serves as the primary energy processing unit, while the SC network acts as the voltage multiplication stage. During the ON interval (S_1–S_4 closed), energy is stored in inductors L_1–L_4, while the capacitors redistribute the charge internally. During the

OFF interval (S_1–S_4 open), the energy stored in the inductors is transferred to the SC network along with energy directly from the input source, resulting in a voltage increase across the capacitor stack.

To further highlight the modular and scalable nature of the proposed topology, the converter can be represented using a block-based abstraction as shown in Figure 3. In Figure 3, the interleaved stage is represented as a unified energy processing block, while the multilevel switched-capacitor network is decomposed into identical modular cells connected in series at the output. This representation clearly demonstrates that the voltage gain can be increased by adding more modules without modifying the core converter structure.

The main novelty of the proposed topology lies in the introduction of a modular hybrid architecture that enables scalable voltage gain through structural expansion of switched-capacitor cells, while simultaneously decoupling the voltage boosting mechanism from current conditioning. Unlike previously reported hybrid interleaved switched-capacitor converters, where voltage boosting and current sharing mechanisms are tightly coupled within a fixed structure [21], the proposed topology explicitly separates these two functions. The interleaved stage is dedicated to current distribution and ripple reduction, while the modular switched-capacitor network independently determines the voltage gain. This decoupled configuration enables independent optimization of electrical performance and provides a scalable design framework, which is not achievable in conventional hybrid topologies.

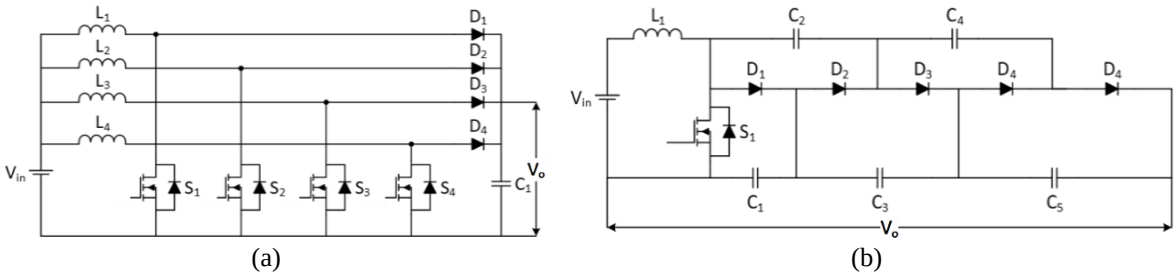

Figure 1. Fundamental configurations: (a) four-phase interleaved boost converter and (b) switched-capacitor (SC) voltage multiplier network

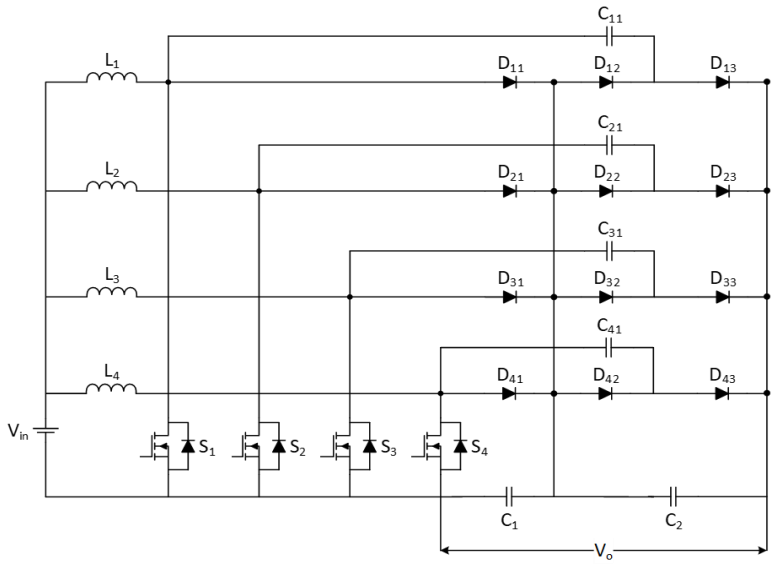

Figure 2. Detailed circuit configuration of the proposed hybrid four-phase interleaved multilevel boost converter with switched-capacitor network

Furthermore, the hybrid structure inherently separates the roles of each subsystem, where the interleaved stage is responsible for current sharing and ripple reduction, while the multilevel SC network

determines the voltage gain. This separation provides greater flexibility in design and forms the basis of the modular scalability of the proposed converter.

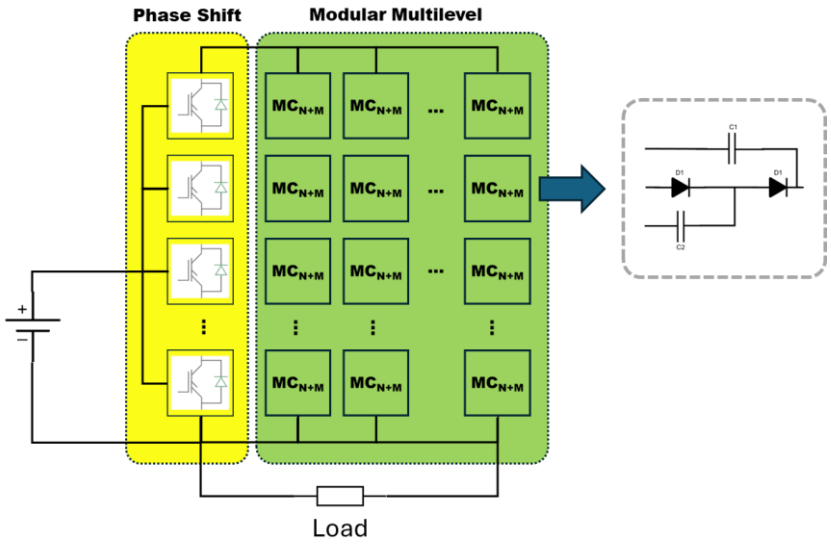

Figure 3. Block representation of the proposed hybrid modular converter showing the interleaved stage and the scalable switched-capacitor modules

2.2. Mathematical modeling and voltage conversion ratio derivation

To analytically validate the proposed topology, the voltage conversion ratio is derived using the inductor volt-second balance principle combined with charge balance analysis under steady state conditions. The analysis assumes that the converter operates in continuous conduction mode (CCM). Within one switching period *T*, the interleaved converter operates with phase-shifted switching signals, where each phase is activated sequentially with a 90° phase difference. Therefore, the switches do not turn ON simultaneously in practice. However, for the purpose of voltage gain derivation, an equivalent averaged model is adopted, where the combined effect of all phases is represented by an equivalent switching function. During the ON state, the inductors are directly connected to the input source, resulting in energy storage in each phase. During this interval, the inductor voltage is equal to the input voltage where V_{in} denotes the input DC voltage. During the OFF state, the switches are turned OFF, and the stored energy in the inductors is transferred to the output through the switched-capacitor network. In this condition, the inductor voltage is defined by the difference between the input voltage and the output voltage where V_o represent the output voltage of converter.

Let *D* denote the duty cycle of the switching signal, defined as the ratio of the ON time to the switching period *T*. The voltage conversion relationship is derived based on the inductor volt-second balance under steady state conditions, assuming CCM operation.

$$D.V_{in} + (1 - D)(V_{in} - V_o) = 0 \quad (1)$$

Rewriting the (2).

$$DV_{in} + (1 - D)V_{in} - (1 - D)V_o = 0$$
$$V_{in} - (1 - D)V_o = 0 \quad (2)$$

Thus, the basic boost relationship is obtained as (3).

$$V_o = \frac{V_{in}}{1-D} \quad (3)$$

In the proposed topology, the output voltage is generated through a multilevel switched-capacitor network. The voltage across each capacitor is determined by the charge and discharge processes governed by the diode capacitor network, as shown in Figure 2. During the OFF state, each capacitor is charged by a combination of the input source and the stored energy in the inductors, forming a cascaded voltage buildup mechanism.

Under steady state operation, each capacitor satisfies the charge balance condition, where the net charge variation over one switching period is zero. This condition can be expressed as (4).

$$i_{C_k}^{avg} = 0 \tag{4}$$

Where $i_{C_k}^{avg}$ denotes the average current of the k-th capacitor over one switching period, and k = 1, 2, …, M, with M representing the number of switched-capacitor modules. This condition ensures that the charge gained during the charging interval is equal to the charge released during the discharging interval. As a result, all capacitor voltages converge to approximately the same value (5).

$$V_{C_1} = V_{C_2} = \cdots = V_{C_M} \tag{5}$$

Where V_{C_k} denotes the voltage across the k-th capacitor.

Since each capacitor is charged to a voltage approximately equal to the boosted input voltage, it can be expressed as (6):

$$V_{C_k} \approx \frac{V_{in}}{1-D} \tag{6}$$

Therefore, the total output voltage becomes (7).

$$V_o = \sum_{k=1}^{M} V_{C_k} = M.\frac{V_{in}}{1-D} \tag{7}$$

Thus, the voltage conversion ratio of the proposed hybrid modular converter is given by (8).

$$\frac{V_o}{V_{in}} = \frac{M}{1-D} \tag{8}$$

Where M denotes the number of switched-capacitor modules.

This result confirms that the voltage gain increases linearly with the number of switched-capacitor modules M, which directly reflects the scalability characteristic illustrated in Figure 3. The conversion ratio can be interpreted as the combination of a conventional boost factor $\frac{1}{1-D}$ and a modular multiplication factor M, indicating that the proposed topology achieves high voltage gain through structural scaling rather than extreme duty cycle operation.

In an N-phase interleaved configuration, the input current is equally distributed among all phases, such that each phase carries approximately $\frac{I_{in}}{N}$, resulting in reduced current stress on switching devices. Furthermore, due to the phase-shifted operation of the interleaved structure, the input current ripple is significantly reduced. The net input current ripple can be approximated as (9).

$$\frac{\Delta I_{in,total}}{\Delta I_{L,single}} \approx \frac{1}{N} \tag{9}$$

Where $\Delta I_{L,single}$ represents the ripple current of a single phase. This ripple cancellation effect becomes more significant as the number of phases increases, improving input current quality and reducing filtering requirements. For the four-phase implementation (N = 4), this translates to a 75% reduction in input current ripple compared to a single-phase converter.

3. SIMULATION METHOD AND VALIDATION SETUP

In this study, an open-loop control scheme is adopted to evaluate the fundamental performance of the proposed converter topology. A fixed duty cycle is applied to generate the pulse-width modulation (PWM) signals based on the theoretical voltage gain derived in section 2. This approach allows direct validation of the converter operating principle without the influence of a feedback controller. The use of an open-loop configuration is intended to isolate and assess the intrinsic performance of the proposed topology under steady-state conditions.

Converter performance validation was conducted through comprehensive simulation using PSIM, enabling detailed analysis of steady state and dynamic characteristics before physical prototype implementation. The complete simulation model of the proposed converter is shown in Figure 4. The model

incorporates all essential components, including the four-phase interleaved boost stage, the modular SC network, PWM signal generation, and measurement blocks. The interleaved stage consists of four identical phases, each comprising an inductor (L1–L4), a MOSFET switch (S1–S4), and a diode (D1–D4). The switches are driven by phase-shifted PWM signals with a 90° phase difference to ensure proper interleaved operation and input current ripple reduction. The switching frequency is set to 10 kHz, and the duty cycle is fixed at 0.5 according to the theoretical gain requirement. The switched-capacitor network is configured as a multilevel modular structure consisting of five capacitors (C1–C5). These capacitors operate through sequential charging and discharging processes via diode-controlled paths, forming a voltage multiplication mechanism. This modular configuration enables scalable voltage gain and balanced voltage stress distribution across the capacitors.

The simulation parameters are selected based on the theoretical design to ensure CCM operation and stable steady-state performance. The input voltage is set to 25 V, and the load is modeled as a resistive load of 10 Ω. Each inductor (L1–L4) is set to 200 µH, while the switched-capacitor values (C1–C5) are set to 100 µF. The phase shift between interleaved PWM signals is maintained at 90°. The simulation parameters used in this study are summarized in Table 1.

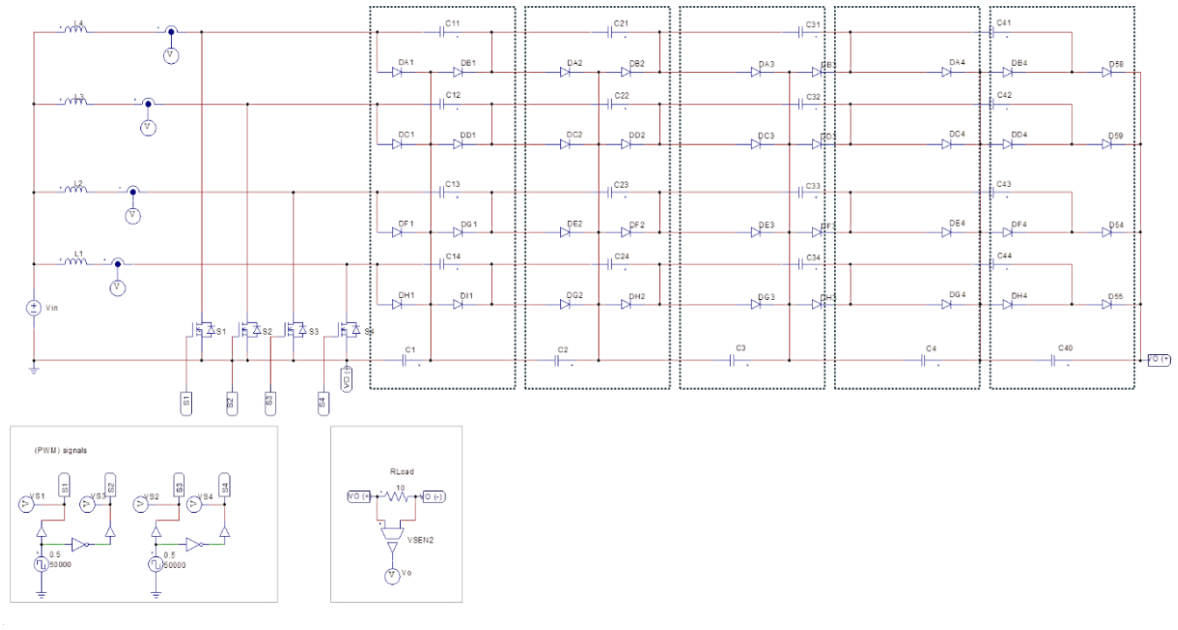

Figure 4. Simulation model of the proposed four-phase interleaved multilevel hybrid boost converter with switched-capacitor network

Table 1. PSIM simulation parameters

Parameter	Value	Unit	Parameter	Value	Unit
Input voltage	25	V	Inductor L_1-L_4	200	uH
Output voltage	250	V	Switched-capacitors C_1-C_5	100	uF
Switching frequency	10	kHz	Output capacitors	110	uF
Duty cycle	0.5		Phase shift	90	
Number of phases	4				

Validation focused on multiple key performance metrics to thoroughly assess the converter's operational characteristics. These metrics included the actual voltage conversion ratio achieved during operation, overall power conversion efficiency, output voltage ripple characteristics, voltage balancing performance across the switched-capacitor network, current distribution among the interleaved phases, and transient response behavior under dynamic load conditions. All performance parameters were monitored and recorded using virtual measurement probes within the simulation environment, allowing for comprehensive data collection and analysis. The validation process began with steady state analysis, where the converter successfully achieved 250 V output voltage from 25 V input, confirming the 10:1 conversion ratio. Voltages across all five SC capacitors measured balanced at approximately 50 V, validating the multilevel voltage

distribution principle. Currents through the four inductors showed identical magnitude and waveform with 90° phase shift, confirming proper interleaved operation.

Validation focuses on multiple key performance metrics to thoroughly assess the proposed converter's operational characteristics. These metrics include the voltage conversion ratio, power conversion efficiency, output voltage ripple, voltage balancing across the switched-capacitor network, current distribution among interleaved phases, and transient response under dynamic loading conditions. All performance parameters are monitored using virtual measurement probes within the PSIM simulation environment, enabling systematic data acquisition and analysis. The validation procedure consists of two main stages: steady-state evaluation and dynamic response analysis. In the steady-state evaluation, the converter performance is assessed under nominal operating conditions to verify the theoretical voltage gain, voltage balancing capability, and current sharing behavior. In the dynamic analysis, controlled load variations are applied to examine the transient response and stability of the converter under changing operating conditions. This structured validation approach ensures that the proposed topology is evaluated comprehensively in terms of both steady-state performance and dynamic behavior.

4. RESULTS AND DISCUSSION

To validate the performance of the proposed four-phase interleaved five-level hybrid boost converter with switched-capacitor multiplier, comprehensive simulations were conducted using PSIM software. The simulation parameters are consistent with those listed in Table 1 in the Method section. The simulation results confirm the capability of the proposed converter to achieve high voltage gain while maintaining stable operation and effective current sharing across phases.

To further highlight the advantages and positioning of the proposed topology, a comparative analysis with recently reported high step-up hybrid DC–DC converters is presented in Table 2. As shown in Table 2, several existing high step-up converters employ switched-capacitor or voltage multiplier techniques to achieve high voltage gain. However, these topologies are generally implemented in fixed configurations or exhibit limited scalability. In addition, most of them do not incorporate interleaved operation, which limits their current-sharing capability and increases input current ripple.

Table 2. Comparison of the proposed converter with recently reported hybrid high step-up DC–DC converters in terms of voltage gain, efficiency, structural characteristics, and limitations

Topology	Gain	Efficiency (%)	Key feature	Limitation
Nx interleaved multilevel boost [21]	8.4×	96.1	Multilevel + interleaved	Fixed structure
Hybrid three-level boost [22]	>10×	93.1	Simple structure	Limited scalability
MMC-based hybrid [23]	>10×	~95	Modular structure	High complexity
Hybrid boost + multiplier [16]	High	~95	High gain	Fixed structure
Hybrid boost + SC cell [15], [24]	High	~98	High efficiency	Not scalable
Hybrid interleaved modular SC (proposed)	$\frac{M}{1-D}$	95.2	Scalable + modular	Simulation-based

In contrast, the proposed converter integrates a modular switched-capacitor structure with an interleaved architecture, enabling both scalable voltage gain and effective current sharing. The voltage gain can be flexibly adjusted through the number of capacitor modules, while maintaining balanced voltage stress and reduced ripple. This feature clearly distinguishes the proposed topology from existing approaches.

The output voltage waveform of the proposed converter is shown in Figure 5(a). The converter successfully elevates the input voltage of 25 V to an output voltage of approximately 250 V, achieving a voltage gain of 10. This result is consistent with the theoretical voltage conversion ratio derived in section 2, thereby validating the analytical model of the proposed topology. The output voltage exhibits a fast transient response during start-up, reaching the steady state value with minimal overshoot and settling time. The steady state output voltage ripple is measured to be less than 2%, which is acceptable for high-gain applications and underscores the advantage of the multilevel configuration in reducing output voltage ripple [25], [26]. Figure 5(b) illustrates the comparison between the obtained output voltage (*Vo*) and the expected theoretical value. The deviation remains within a small range (±1 V), corresponding to approximately 0.4%, confirming the accuracy of the analytical model under open-loop operation. This small deviation can be attributed to non-ideal effects such as switching losses, parasitic resistances, and capacitor equivalent series resistance (ESR). The results demonstrate that the proposed topology is capable of achieving the desired voltage gain with high accuracy under steady-state conditions [27], [28].

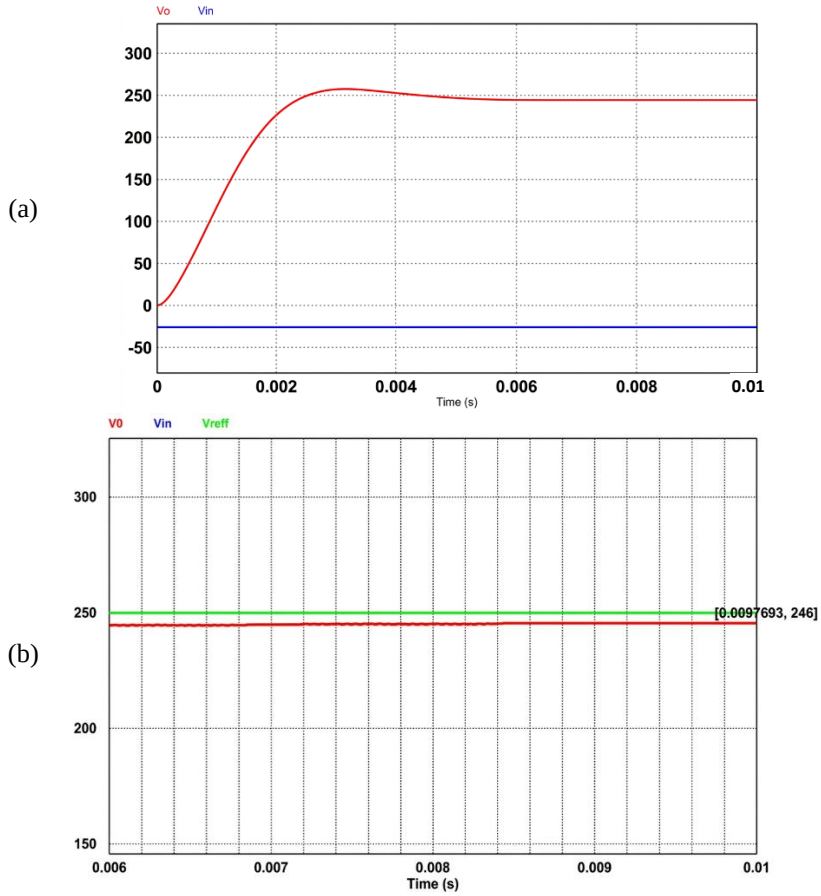

Figure 5. Output voltage waveform demonstrating: (a) step-up from 25 V input to 250 V output and (b) illustrates the comparison between the obtained output voltage and the expected theoretical value

The voltage balancing across the five switched-capacitor cells (*VC1* to *VC5*) is shown in Figure 6(a). The voltages across each capacitor are well balanced, with each capacitor sustaining approximately 50 V, which is one-fifth of the total output voltage (250 V). This equal voltage distribution validates the modular multilevel operation of the SC network and prevents excessive voltage stress on individual components. The small ripple observed (less than 1 V peak-to-peak) on each capacitor voltage is consistent with the switching frequency and indicates effective charge redistribution within the network. This balanced voltage profile enhances reliability and allows the use of lower voltage-rated components, contributing to improved system efficiency and reduced cost [29], [30].

On the other hand, the current waveforms of the four interleaved inductors (L1 to L4) are shown in Figure 6(b). The currents in each phase are nearly identical in magnitude and waveform, with a 90° phase shift between adjacent phases. This confirms proper interleaved operation and demonstrates effective current sharing among all phases. The measured current ripple in each phase is approximately 1.2 A peak-to-peak, while the net input current ripple is reduced to about 0.3 A peak-to-peak, representing a 75% reduction due to the interleaving effect. This significant ripple reduction contributes to lower electromagnetic interference (EMI), reduced input filter requirements, and improved overall converter performance. Furthermore, balanced current distribution ensures uniform thermal stress across switching devices, enhancing system reliability [23], [31]. The measured efficiency of the converter under full load condition is approximately 95.2%, which can be attributed to the reduced conduction losses thanks to the even current sharing and the low voltage stress on the switches.

Figure 7 presents the PWM modulation signals (VSA1 to VSA4) for the four interleaved phases. The signals exhibit a precise 90° phase shift and operate at a switching frequency of 10 kHz with a consistent duty cycle of approximately 50%. This phase-shifted PWM operation is essential for achieving current ripple cancellation and balanced power distribution among phases. The synchronization of the PWM signals confirms correct implementation of the interleaving strategy [32].

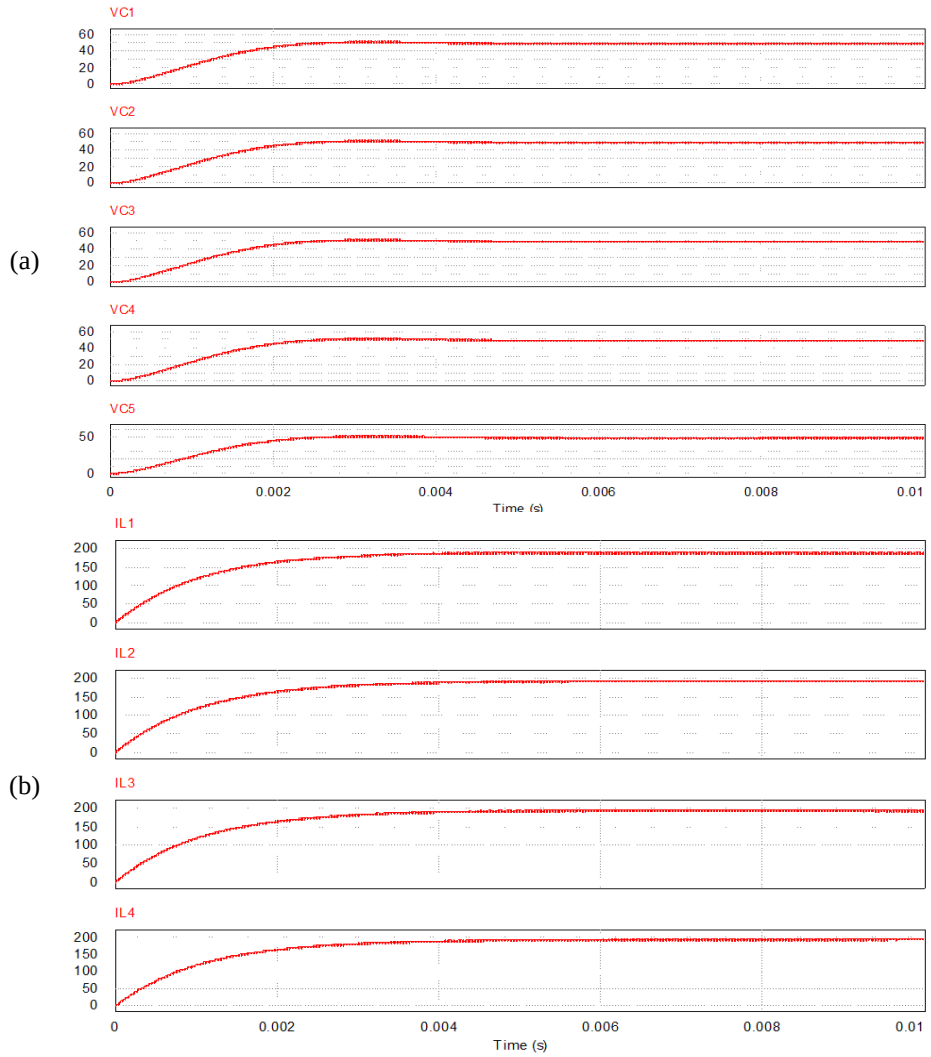

Figure 6. Steady-state performance of the proposed converter: (a) voltage distribution across the switched-capacitor cells (VC1 to VC5) and (b) current waveforms of the interleaved inductors (L1 to L4)

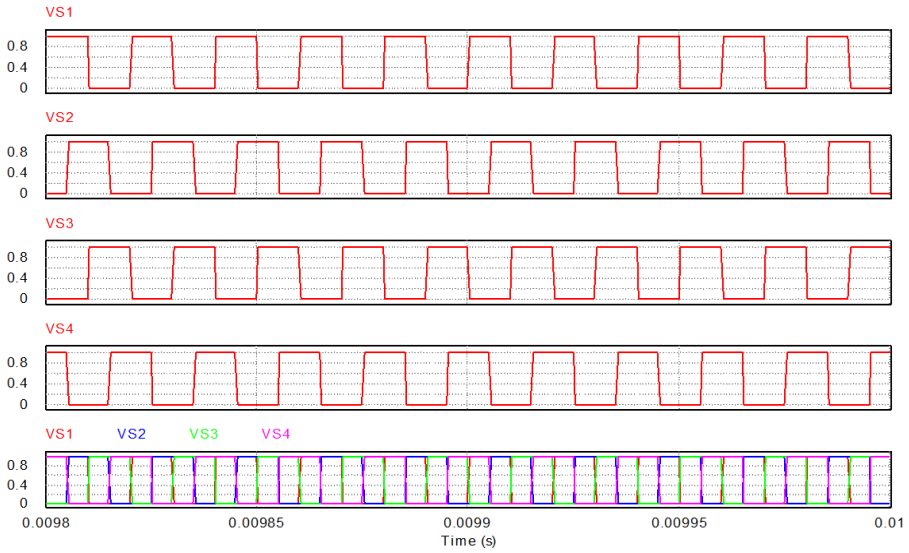

Figure 7. PWM modulation signals for the four interleaved phases (VSA1 to VSA4) showing precise 90° phase-shift and consistent duty cycle operation

All four modulation signals maintain identical duty cycles under steady-state operation, consistent with the theoretical requirement for achieving the targeted voltage gain. This uniform duty cycle contributes to balanced power processing and supports the equal current distribution observed in the interleaved inductors. The simulation results comprehensively validate the proposed hybrid modular converter topology. Compared to conventional boost converters and other high-gain topologies such as coupled inductor converters [33] and quadratic boost converters [34], the modular structure enables flexible expansion of voltage gain, while the interleaved configuration enhances current handling capability and thermal performance. The small voltage deviation (0.4%) and low output ripple (<2%) indicate that the converter is suitable for high step-up applications requiring stable and efficient operation. Future work will focus on experimental validation using a hardware prototype and further investigation of the converter performance under wide input voltage variations and unbalanced loading conditions.

5. CONCLUSION

This study has presented the design and simulation-based evaluation of a hybrid four phase interleaved multilevel boost converter incorporating a switched-capacitor multiplier. The proposed topology demonstrates its ability to achieve high voltage gain while maintaining efficiency, low ripple, and balanced electrical stress across components. The results confirm that the converter can step-up a 25 V input to an output voltage of approximately 250 V, achieving a voltage gain of 10 with high efficiency (95.2%), low output voltage ripple (<2%), and a small deviation of approximately 0.4% from the expected theoretical value. The interleaved structure ensured balanced current sharing and reduced input current ripple, while the modular multilevel SC network facilitated equal voltage stress distribution across components, enhancing reliability and allowing for the use of lower rated devices. Furthermore, the proposed converter introduces a decoupled architectural approach, in which current conditioning and voltage boosting functions are independently realized through the interleaved stage and the modular switched-capacitor network. This feature provides improved design flexibility and enables scalable voltage gain without modifying the core converter structure. The research objectives set forth were met, demonstrating that the proposed hybrid architecture offers a favorable balance between high performance, component stress, and control simplicity compared to conventional and recent high gain converter topologies. Although this study is based on simulation results, the findings demonstrate the feasibility and effectiveness of the proposed converter for high step-up applications. The simulation results provide a strong foundation for future experimental validation and practical implementation. Future work will focus on the development of a hardware prototype to experimentally verify the converter performance, evaluate efficiency under practical operating conditions, and investigate its behavior under wide input voltage variations and unbalanced loading conditions.

FUNDING INFORMATION

The authors would like to express their sincere gratitude to the Ministry of Education, Culture, Research, and Technology of the Republic of Indonesia for the financial support provided through the research grant under contract number 124/UN16.19/PT.01.03/PL/2025. This support has been essential in the completion of this research work.

AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
Andi M. Nur Putra	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
Adrianti	✓	✓			✓	✓		✓	✓	✓	✓	✓		✓
Muhammad Imran Hamid	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓				

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper. Authors state no conflict of interest.

DATA AVAILABILITY

The authors confirm that the data supporting the findings of this study are available within the article and its supplementary materials. Additional data are available from the corresponding author upon reasonable request.

REFERENCES

[1] Adrianti, H. H. Yama, and M. Nasir, "Electric demand forecast of Padang city considering effect of global warming," *AIP Conference Proceedings*, vol. 2891, no. 1, 2024, doi: 10.1063/5.0201000.

[2] Adrianti, T. K. Agung, M. Nasir, and P. Anugrah, "A 48-MW floating photovoltaic design and integration to a grid," *Indonesian Journal of Electrical Engineering and Computer Science*, vol. 30, no. 3, pp. 1331–1338, 2023, doi: 10.11591/ijeecs.v30.i3.pp1331-1338.

[3] A. M. N. Putra, T. D. Rachmildha, Y. Haroen, and A. P. Sadono, "The effect of safe ball size changes on boost converter using hybrid control," in *2016 3rd Conference on Power Engineering and Renewable Energy (ICPERE)*, 2016, pp. 19–23, doi: 10.1109/ICPERE.2016.7904841.

[4] M. Kumar, M. Ashirvad, and Y. N. Babu, "An integrated Boost-Sepic-Ćuk DC-DC converter with high voltage ratio and reduced input current ripple," *Energy Procedia*, vol. 117, pp. 984–990, Jun. 2017, doi: 10.1016/j.egypro.2017.05.219.

[5] F. M. Shahir, E. Babaei, and M. Farsadi, "Extended topology for a boost DC–DC converter," *IEEE Transactions on Power Electronics*, vol. 34, no. 3, pp. 2375–2384, Mar. 2019, doi: 10.1109/TPEL.2018.2840683.

[6] A. Allehyani, "Analysis of a symmetrical multilevel DC-DC boost converter with ripple reduction structure for solar PV systems," *Alexandria Engineering Journal*, vol. 61, no. 9, pp. 7055–7065, Sep. 2022, doi: 10.1016/j.aej.2021.12.049.

[7] M.-K. Nguyen, T.-D. Duong, and Y.-C. Lim, "Switched-capacitor-based dual-switch high-boost DC–DC converter," *IEEE Transactions on Power Electronics*, vol. 33, no. 5, pp. 4181–4189, May 2018, doi: 10.1109/TPEL.2017.2719040.

[8] A. Ajami, H. Ardi, and A. Farakhor, "A novel high step-up DC/DC converter based on integrating coupled inductor and switched-capacitor techniques for renewable energy applications," *IEEE Transactions on Power Electronics*, vol. 30, no. 8, pp. 4255–4263, Aug. 2015, doi: 10.1109/TPEL.2014.2360495.

[9] S.-W. Lee and H.-L. Do, "Quadratic Boost DC–DC converter with high voltage gain and reduced voltage stresses," *IEEE Transactions on Power Electronics*, vol. 34, no. 3, pp. 2397–2404, Mar. 2019, doi: 10.1109/TPEL.2018.2842051.

[10] R. Hu, J. Zeng, J. Liu, Z. Guo, and N. Yang, "An ultrahigh step-up quadratic boost converter based on coupled-inductor," *IEEE Transactions on Power Electronics*, vol. 35, no. 12, pp. 13200–13209, Dec. 2020, doi: 10.1109/TPEL.2020.2995911.

[11] Y. N. Abdelaziz, M. Mansour, F. Alsokhiry, K. H. Ahmed, A. S. Abdel-khalik, and A. Abdulwhab, "A new hybrid multilevel thyristor-based DC-DC converter," *Alexandria Engineering Journal*, vol. 85, pp. 320–332, Dec. 2023, doi: 10.1016/j.aej.2023.11.029.

[12] H. Ye, G. Jin, W. Fei, and N. Ghadimi, "High step-up interleaved DC/DC converter with high efficiency," *Energy Sources, Part A: Recovery, Utilization, and Environmental Effects*, vol. 46, no. 1, pp. 4886–4905, Dec. 2024, doi: 10.1080/15567036.2020.1716111.

[13] J. C. Rosas-Caro, J. M. Ramirez, F. Z. Peng, and A. Valderrabano, "A DC–DC multilevel boost converter," *IET Power Electronics*, vol. 3, no. 1, pp. 129–137, Jan. 2010, doi: 10.1049/iet-pel.2008.0253.

[14] X. Zhang and T. C. Green, "The modular multilevel converter for high step-up ratio DC–DC conversion," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 8, pp. 4925–4936, Aug. 2015, doi: 10.1109/TIE.2015.2393846.

[15] A. Andrade, T. Faistel, R. Guisso, and A. Toebe, "Hybrid high voltage gain transformerless DC–DC converter," *IEEE Transactions on Industrial Electronics*, vol. 69, no. 3, pp. 2470–2479, Mar. 2022, doi: 10.1109/TIE.2021.3066939.

[16] B. Wu, S. Li, Y. Liu, and K. Ma Smedley, "A new hybrid boosting converter for renewable energy applications," *IEEE Transactions on Power Electronics*, vol. 31, no. 2, pp. 1203–1215, Feb. 2016, doi: 10.1109/TPEL.2015.2420994.

[17] H. Bahrami, S. Farhangi, H. Iman-Eini, and E. Adib, "A new interleaved coupled-inductor nonisolated soft-switching bidirectional DC–DC converter with high voltage gain ratio," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 7, pp. 5529–5538, Jul. 2018, doi: 10.1109/TIE.2017.2782221.

[18] S. Kascak, M. Prazenica, M. Jarabicova, and R. Konarik, "Four phase interleaved boost converter: Theory and applications," *WSEAS Transactions on Power Systems*, vol. 13, pp. 272–282, 2018.

[19] B. Axelrod, Y. Beck, and Y. Berkovich, "High step-up DC–DC converter based on the switched-coupled-inductor boost converter and diode-capacitor multiplier: steady state and dynamics," *IET Power Electronics*, vol. 8, no. 8, pp. 1420–1428, Aug. 2015, doi: 10.1049/iet-pel.2014.0785.

[20] L. Schmitz, D. C. Martins, and R. F. Coelho, "Comprehensive conception of high step-up DC–DC converters with coupled inductor and voltage multipliers techniques," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 6, pp. 2140–2151, Jun. 2020, doi: 10.1109/TCSI.2020.2973154.

[21] M. S. Bhaskar, D. J. Almakhles, S. Padmanaban, F. Blaabjerg, U. Subramaniam, and D. M. Ionel, "Analysis and investigation of hybrid DC–DC non-isolated and non-inverting Nx interleaved multilevel boost converter (Nx-IMBC) for high voltage step-up applications: hardware implementation," *IEEE Access*, vol. 8, pp. 87309–87328, 2020, doi: 10.1109/ACCESS.2020.2992447.

[22] Y. Zhang, J.-T. Sun, and Y.-F. Wang, "Hybrid boost three-level DC–DC converter with high voltage gain for photovoltaic generation systems," *IEEE Transactions on Power Electronics*, vol. 28, no. 8, pp. 3659–3664, Aug. 2013, doi: 10.1109/TPEL.2012.2229720.

[23] M. Diab, A. A. Elserougi, and A. S. Abdel-Khalik, "A hybrid DC-DC modular multilevel converter with capacitors parallel connectivity for arm energy balancing," *Alexandria Engineering Journal*, vol. 83, pp. 286–297, Nov. 2023, doi: 10.1016/j.aej.2023.10.050.

[24] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Switched-capacitor/switched-inductor structures for getting transformerless hybrid DC–DC PWM converters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 2, pp. 687–696, Mar. 2008, doi: 10.1109/TCSI.2008.916403.
[25] A. Zakaria, M. I. Marei, and H. M. Mashaly, "A hybrid interleaved DC-DC converter based on buck-boost topologies for medium voltage applications," *e-Prime - Advances in Electrical Engineering, Electronics and Energy*, vol. 6, p. 100301, Dec. 2023, doi: 10.1016/j.prime.2023.100301.
[26] S. Sarani, A. Nikbahar, H. A. Zarchi, and X. Liang, "An isolated high boost ratio DC–DC converter with very low input current ripples," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 71, no. 9, pp. 4331–4335, Sep. 2024, doi: 10.1109/TCSII.2024.3386158.
[27] A. Khosroshahi, M. Abapour, and M. Sabahi, "Reliability evaluation of conventional and interleaved DC–DC boost converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5821–5828, Oct. 2015, doi: 10.1109/TPEL.2014.2380829.
[28] M. Fekri, N. Molavi, E. Adib, and H. Farzanehfard, "High voltage gain interleaved DC–DC converter with minimum current ripple," *IET Power Electronics*, vol. 10, no. 14, pp. 1924–1931, Nov. 2017, doi: 10.1049/iet-pel.2016.0675.
[29] M.-K. Nguyen, T.-D. Duong, and Y.-C. Lim, "Switched-capacitor-based dual-switch high-boost DC–DC converter," *IEEE Transactions on Power Electronics*, vol. 33, no. 5, pp. 4181–4189, May 2018, doi: 10.1109/TPEL.2017.2719040.
[30] X. Zhu, B. Zhang, Z. Li, H. Li, and L. Ran, "Extended switched-boost DC-DC converters adopting switched-capacitor/switched-inductor cells for high step-up conversion," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 3, pp. 1020–1030, Sep. 2017, doi: 10.1109/JESTPE.2016.2641928.
[31] M. S. Bhaskar *et al.*, "A new hybrid zeta-boost converter with active quad switched inductor for high voltage gain," *IEEE Access*, vol. 9, pp. 20022–20034, 2021, doi: 10.1109/ACCESS.2021.3054393.
[32] J. I. Y. Ota, Y. Shibano, N. Niimura, and H. Akagi, "A phase-shifted-PWM D-STATCOM using a modular multilevel cascade converter (SSBC)—Part I: Modeling, analysis, and design of current control," *IEEE Transactions on Industry Applications*, vol. 51, no. 1, pp. 279–288, Jan. 2015, doi: 10.1109/TIA.2014.2326079.
[33] S.-W. Lee and H.-L. Do, "High step-up coupled-inductor cascade boost DC–DC converter with lossless passive snubber," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 10, pp. 7753–7761, Oct. 2018, doi: 10.1109/TIE.2018.2803731.
[34] A. Gupta, N. Korada, and R. Ayyanar, "Quadratic-extended-duty-ratio boost converters for ultra high gain application with low input current ripple and low device stress," *IEEE Transactions on Industry Applications*, vol. 59, no. 1, pp. 938–948, Jan. 2023, doi: 10.1109/TIA.2022.3207132.

BIOGRAPHIES OF AUTHORS

Andi M. Nur Putra received his Bachelor of Engineering degree in electrical engineering from Institut Teknologi Padang, Indonesia, in 2012. He obtained his Master of Engineering degree in Electrical Engineering from Institut Teknologi Bandung, Indonesia, in 2016. In 2017, he completed a professional certification program in power system applied competencies at the Southern Alberta Institute of Technology (SAIT), Canada. He is currently pursuing his Ph.D. degree in electrical engineering at Universitas Andalas, Indonesia. He is an assistant professor at the Department of Electrical Engineering, Institut Teknologi Padang, Indonesia. His research interests include power electronics, renewable energy systems, electric drives, distributed generation, and smart grid technologies. He can be contacted at email: andimnurputra@gmail.com.

Adrianti received her Bachelor of Engineering degree in electrical engineering from Universitas Andalas, Indonesia. She obtained her Master of Engineering degree in electrical engineering from Institut Teknologi Bandung in 2000, and later earned her Ph.D. degree in Electrical Engineering. She is currently a faculty member at the Department of Electrical Engineering, Faculty of Engineering, Universitas Andalas, Indonesia, where she serves as an associate professor. Her research interests include power systems and electrical energy distribution. She can be contacted at email: adrianti@eng.unand.ac.id.

Muhammad Imran Hamid received his Bachelor of Engineering degree in electrical power engineering from Universitas Hasanuddin, Indonesia. He obtained his Master of Engineering degree in electrical engineering from Institut Teknologi Bandung, Indonesia, in 2001, and later earned his Ph.D. in electrical energy conversion from Universiti Teknologi Malaysia. He is currently a faculty member at the Department of Electrical Engineering, Faculty of Engineering, Universitas Andalas, Indonesia. His research interests include renewable energy, power electronics, energy conversion systems, and power quality. He can be contacted at email: imran@eng.unand.ac.id.