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Optimal selection of current control technique in multiphase DC-DC converters for dynamic load variations

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ABSTRACT

Multiphase DC-DC converters are widely adopted in high-power applications such as electric vehicles (EVs) and renewable energy systems due to their ability to reduce current ripple, improve efficiency, and distribute thermal stress across multiple phases. However, under dynamic load variations, mismatches in passive components, device parameters, parasitic elements, and thermal effects can result in phase current imbalance. This imbalance degrades transient performance, increases circulating currents, and reduces overall system reliability. Therefore, selecting an appropriate current control strategy is essential to ensure accurate current sharing and stable output voltage regulation under varying operating conditions. This paper presents a comparative study and selection methodology for current control techniques for MCU-based interleaved DC-DC converters. Various current control strategies are evaluated in terms of dynamic response, steady-state current sharing accuracy, implementation complexity, and embedded feasibility. A 1 kW, 36 V-12 V three-phase interleaved buck converter using Gallium Nitride devices is modeled in MATLAB/Simulink and validated through hardware experimentation. The comparative results highlight the trade-offs among transient performance, current balancing accuracy, scalability, and embedded implementation complexity, providing a structured basis for selecting an appropriate current control technique as per application requirements.

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1. INTRODUCTION

The rapid electrification of transportation, driven by stringent emission regulations and the global transition toward sustainable energy, has significantly increased the demand for high-efficiency and high-power-density conversion systems. In electric vehicles and hybrid energy platforms, DC-DC converters play a critical role in stepping down high-voltage battery levels to regulated low-voltage buses, supplying auxiliary loads, and managing bidirectional energy flow between storage elements and power electronic subsystems. As these applications require improved efficiency, high power density, and fast transient response under dynamic load conditions, interleaved multiphase DC-DC converters have emerged as a preferred solution [1]. By distributing the load current across multiple phases with phase-shifted operation, these converters

achieve reduced input and output current ripple, lower filtering requirements, improved thermal distribution, enhanced dynamic performance, and reliable power delivery under varying operating conditions [2]–[4].

Such converters typically employ a hierarchical control architecture consisting of an outer voltage loop for output regulation and an inner current loop for inductor current control and phase current sharing. Current control in DC-DC converters is commonly realized using techniques such as peak current mode control (PCMC) and average current mode control (ACMC). PCMC is widely adopted in single-phase buck and boost converters, where it enables direct inductor current regulation and cycle-by-cycle current monitoring [5]. ACMC is frequently implemented in multiphase converters, power factor correction (PFC) systems, and battery charging applications, where average inductor current regulation supports controlled power delivery and coordinated phase operation [6], [7]. Within ACMC-based multiphase systems, various strategies such as unified control, individual phase control, and sensorless current control techniques have been proposed to regulate and distribute phase currents effectively [8]–[11]. These approaches provide structured frameworks for implementing current sharing and regulation in digitally controlled multiphase converters.

With the adoption of wide-bandgap (WBG) devices, control design considerations are challenging to accommodate their high-speed switching capabilities. The material properties of WBG devices enable operation in the MHz switching frequency range, offering high efficiency, fast transient response, reduced passive component size, and increased power density [12]–[14]. These characteristics necessitate appropriately designed current regulation strategies capable of operating at elevated switching frequencies with precise timing coordination. Digital control of WBG-based converters can be implemented using platforms such as field programmable gate arrays (FPGAs), microcontrollers (MCUs), and digital signal processors (DSPs). FPGA-based solutions facilitate high-speed control execution and flexible digital architecture design [15], [16]. MCU and DSP-based implementations provide integrated peripherals, programmable control loops, and streamlined system integration, making them widely adopted in industrial power electronic applications. Careful design of digital current control algorithms, sampling strategies, interrupt management, and peripheral configuration plays a key role in achieving effective implementation in WBG-based multiphase converters.

In practical implementations, mismatches in passive components, parasitic resistances, device characteristics, gate driver timing, and PCB layout asymmetry can lead to non-uniform phase currents. Sampling delays, digital control discretization, and dynamic load variations can further exacerbate this imbalance. Persistent current mismatch results in localized thermal hotspots, uneven switching and conduction stress, accelerated device ageing, reduced efficiency, and compromised long-term reliability of the converter system. To mitigate the current imbalance, several ACMC-based strategies have been proposed in the literature, demonstrated through analytical studies, simulations, or FPGA-based digital implementations, where flexible control architecture and parallel processing capabilities can be realized. In contrast, industrial multiphase DC-DC converters are predominantly implemented using MCUs and DSPs, owing to their integrated peripherals, compact architecture, streamlined firmware development, and suitability for cost-effective deployment. However, a systematic experimental evaluation of different ACMC-based current balancing strategies implemented on a resource-constrained MCU platform under identical operating conditions has not been comprehensively reported. This study aims to demonstrate the advantages and potential drawbacks of each approach in practical applications, providing insights into their implementation and impact on the converter performance.

To systematically address the current imbalance in practical implementations, this paper investigates unified, individual, and decoupled current imbalance control techniques in a three-phase interleaved buck converter using an MCU-based digital signal controller. The study focuses on mitigating the current imbalance under both steady-state and dynamic load conditions. Comprehensive simulation and experimental validation are conducted on a 1 kW, 36 V-12 V GaN-based prototype to evaluate current sharing performance and real-time digital implementation aspects of each control strategy.

2. METHOD

This section presents the detailed mathematical modeling of the three-phase interleaved DC-DC converter. A state-space approach is employed to derive the small-signal transfer function. Current control strategies for improving dynamic and steady-state performance are analyzed. The overall system design and control implementation are described. For real-time realization, the MCU-based current sampling and control algorithm execution flow is presented.

2.1. Mathematical modelling of interleaved converter

In an interleaved buck topology, multiple buck converters operate in parallel with a phase shift between the switching signals, thereby distributing the load current among the phases. The circuit diagram of the three-phase interleaved synchronous buck converter considering parasitic elements is shown in Figure 1(a). In the interleaved topology, the phase angle between each phase was determined by the number of phases. Using the relationship 360 °/N (where N is the number of phases) for a three-phase interleaved topology, the phase angle difference between each phase is 120°. For converter analysis, uniform loss components and equal per-phase inductances are considered as given in (1)-(3). For the switching period T_s, the converter operates in six distinct modes, as depicted in Figure 1(b) with two top-switches and an opposite phase bottom switch ON in 3 modes and any one top switch and the other two phases bottom switches ON in the remaining 3 modes of operation.

$$L_1 = L_2 = L_3 = L \tag{1}$$

$$R_{L1} = R_{L2} = R_{L3} = R_L \tag{2}$$

$$R_{ds1T} = R_{ds2T} = R_{ds3T} = R_{ds1B} = R_{ds2B} = R_{ds3B} = R_{ds} \tag{3}$$

The state equations for inductor and capacitor and output equation in mode 1, 3 and 5 (any two top switches are ON) could be written as in (4)-(6).

$$L\frac{di_L(t)}{dt} = 2V_g(t) - \left(R_{ds} + R_L + \frac{3RR_c}{R+R_c}\right) i_L(t) - \left(\frac{3R}{R+R_c}\right) v_c(t) \tag{4}$$

$$C\frac{dv_c(t)}{dt} = \left(\frac{R}{R+R_c}\right) i_L(t) - \left(\frac{1}{R+R_c}\right) v_c(t) \tag{5}$$

$$v(t) = \left(\frac{RR_c}{R+R_c}\right) i_L(t) + \left(\frac{R}{R+R_c}\right) v_c(t) \tag{6}$$

The state equations for inductor and capacitor, and output equations in mode 2, 4 and 6 (only one of the top switch is ON) could be written as in (7)-(9).

$$L\frac{di_L(t)}{dt} = V_g(t) - \left(R_{ds} + R_L + \frac{3RR_c}{R+R_c}\right) i_L(t) - \left(\frac{3R}{R+R_c}\right) v_c(t) \tag{7}$$

$$C\frac{dv_c(t)}{dt} = \frac{R}{(R+R_c)} i_L(t) - \left(\frac{1}{R+R_c}\right) v_c(t) \tag{8}$$

$$v(t) = \left(\frac{RR_c}{R+R_c}\right) i_L(t) + \left(\frac{R}{R+R_c}\right) v_c(t) \tag{9}$$

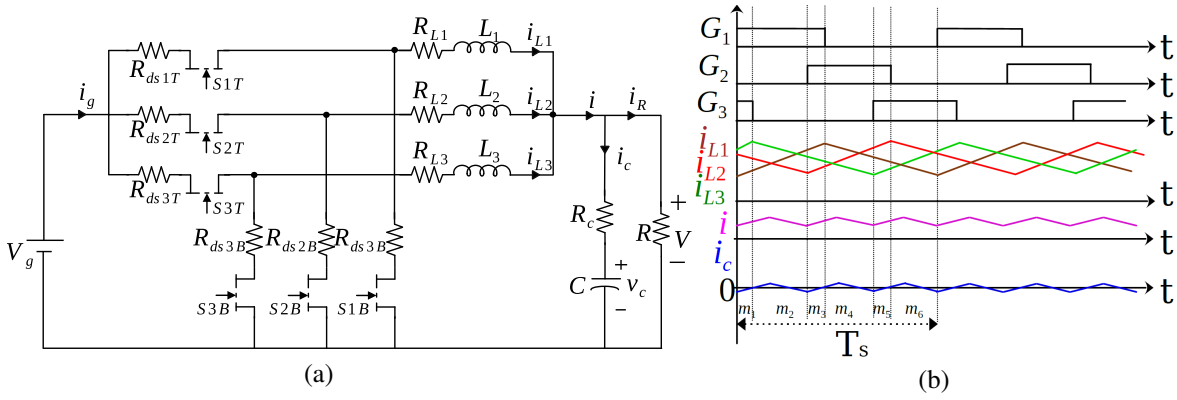


Figure 1. Three-phase interleaved buck converter: (a) mathematical model and (b) timing diagram

From the timing diagram, the converter operates in modes 1, 3, and 5 for a duration of $(\frac{2}{3} - d')$, and in modes 2, 4, and 6 for a duration of $(d' - \frac{1}{3})$, where $d' = 1 - d$. Using the state-space averaging technique, the steady-state equations can be obtained as in (10)-(13) [17].

$$A = A_1 (2 - 3d') + A_2 (3d' - 1) \tag{10}$$

$$B = B_1 (2 - 3d') + B_2 (3d' - 1) \tag{11}$$

$$C = C_1 (2 - 3d') + C_2 (3d' - 1) \tag{12}$$

$$E = E_1 (2 - 3d') + E_2 (3d' - 1) \tag{13}$$

The state space and output equation in the ON state is given as in (14) and (15).

$$\begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix} \begin{bmatrix} \frac{di_L(t)}{dt} \\ \frac{dv_c(t)}{dt} \end{bmatrix} = \begin{bmatrix} -\left(R_{ds} + R_L + \frac{3RR_c}{R+R_c}\right) & -\frac{3R}{R+R_c} \\ \frac{R}{R+R_c} & -\frac{1}{R+R_c} \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix} + \begin{bmatrix} 2 \\ 0 \end{bmatrix} v_g(t) \tag{14}$$

$$\begin{bmatrix} v(t) \\ i_L(t) \end{bmatrix} = \begin{bmatrix} \frac{RR_c}{R+R_c} & \frac{R}{R+R_c} \\ 1 & 0 \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} v_g(t) \tag{15}$$

State space and output equation in the OFF state is given as in (16) and (17).

$$\begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix} \begin{bmatrix} \frac{di_L(t)}{dt} \\ \frac{dv_c(t)}{dt} \end{bmatrix} = \begin{bmatrix} -\left(R_{ds} + R_L + \frac{3RR_c}{R+R_c}\right) & -\frac{3R}{R+R_c} \\ \frac{R}{R+R_c} & -\frac{1}{R+R_c} \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \end{bmatrix} v_g(t) \tag{16}$$

$$\begin{bmatrix} v(t) \\ i_L(t) \end{bmatrix} = \begin{bmatrix} \frac{RR_c}{R+R_c} & \frac{R}{R+R_c} \\ 1 & 0 \end{bmatrix} \begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} v_g(t) \tag{17}$$

Applying Laplace transform, open loop transfer functions could be derived using (18)-(21).

$$\hat{y}(s) = C\left(\left(sI - K^{-1}A\right)^{-1} K^{-1}F + G\right) \hat{d}(s) \tag{18}$$

$$F = (A_1 - A_2) X + (B_1 - B_2) U \tag{19}$$

$$G = (C_1 - C_2) X + (E_1 - E_2) U \tag{20}$$

$$X = -A^{-1}BU \tag{21}$$

The transfer functions, output voltage to control $G_{vd}(s)$ and inductor current to control $G_{id}(s)$ of the three-phase interleaved synchronous buck converter, considering dominant loss components, are derived and given by (22) and (23) [17].

$$G_{vd}(s) = \frac{\hat{v}(s)}{\hat{d}(s)} = \frac{RR_cCV_gs + RV_g}{Den} \tag{22}$$

$$G_{id}(s) = \frac{\widehat{i_L}(s)}{\hat{d}(s)} = \frac{(RCV_g + R_cCV_g)s + V_g}{Den} \tag{23}$$

Where,

$$Den = (RLC + R_cLC)s^2 + (L + 3RR_cC + RR_LC + R_cR_{ds}C + R_cR_LC + RR_{ds}C)s + (3R + R_L + R_{ds})$$

The transfer function between inductor current and output voltage $G_{vi}(s)$ can be derived using (22) and (23) and given as in (24).

$$G_{vi}(s) = \frac{\hat{v}(s)}{\widehat{i_L}(s)} = \frac{RR_cCV_gs + RV_g}{(RCV_g + R_cCV_g)s + V_g} \tag{24}$$

2.2. Current control techniques

Effective current control techniques in multiphase converters play a vital role in enhancing efficiency, reliability, and overall system performance. Advanced control strategies minimize current ripple and EMI, ensuring signal integrity in high-speed applications. Furthermore, accurate current control facilitates optimal converter operation under varying load conditions, supports compact component sizing, simplifies thermal design, and enables scalable and cost-effective system architectures. The following section explores the widely adopted current control methods and their impact on the multiphase converter performance, highlighting MCU implementation aspects.the

2.2.1. Unified current controllers

In the unified current control technique, a single current controller governs all converter phases by generating a common duty cycle d. The system typically employs a cascaded structure, consisting of an outer voltage regulation loop PI_v and an inner current compensator loop PI_i as shown in Figure 2(a). This approach requires only a single current sensor independent of the number of phases. However, as a common duty cycle is applied to each of the phases, this method cannot actively compensate for current mismatches arising from device parameter variations, parasitic elements, or dynamic load transients that may lead to unequal current sharing among phases. Furthermore, in the unified control structure, a fault in any individual phase affects the entire system, potentially degrading overall system performance.

2.2.2. Individual current controllers

Individual current control technique incorporates a dedicated current controller to each phase PI_1, PI_2,...PI_N as shown in Figure 2(b). The outer controller PI_v regulates the overall output voltage and generates a total current reference (I_{ref}), which is distributed across N phases. Each phase controller then regulates the respective inductor current independently. This ensures precise current sharing, enhances fault tolerance as the faulty phase can be isolated, and improves robustness under dynamic load or component parameter variation. However, it adds complexity due to the need for multiple current sensors, synchronized current sampling, and an increased number of current controllers, leading to higher computational complexity as the number of phases increases. Despite being computationally expensive and complex, this method is superior in applications demanding tight current balancing and resilience to phase faults.

2.2.3. Unified current controller with PI-based imbalance compensators

In this method, inductor current of each phase (i_{L1}, i_{L2} ...i_{LN}) is continuously monitored, and a proportional-integral controller (PI_{comp}) computes the correction duty cycle of each phase in real-time based on the deviation from the average phase current (i_{avg}). This correction loop operates at the same rate as the current controller, allowing it to quickly balance phase currents during transients or dynamic load variations. The duty cycle correction factor of each phase is computed through a dedicated correction loop thus ensuring balanced current across the loop. While it ensures excellent transient and steady-state current sharing, additional PI control tuning and execution add to the control complexity. The system model is as in Figure 3(a).

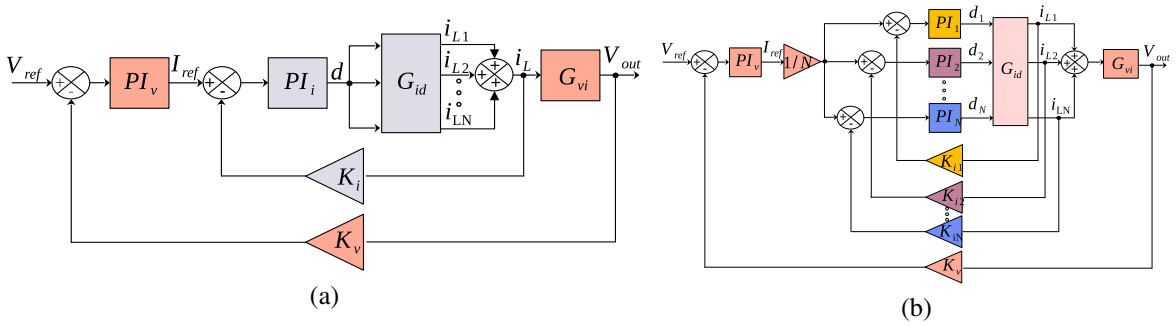


Figure 2. System model with (a) unified current controller and (b) individual current controller

2.2.4. Unified current controller with correction factor-based imbalance compensators

This method utilizes a correction factor (K) to adjust each phase's duty cycle based on imbalance, enabling steady-state accuracy with lower computational demand [18]. This control technique can be

implemented as in Figure 3(b). The per-phase inductor currents are measured and fed to the corresponding correction factor loop that compares the average current $i_{avg} = \frac{I_{ref}}{N}$, where N is the total number of phases. Then the deviation from reference current is computed using (25).

$$\Delta I_N = I_N - I_{avg} \tag{25}$$

The duty cycle correction factor is computed using (26).

$$\Delta D_N = \Delta D_N + K * \Delta I_N \tag{26}$$

The correction factor K can be selected based on the speed of compensation required. The per-phase duty cycle is computed using (27).

$$D_N = D_{base} - \Delta D_N \tag{27}$$

Since duty cycle adjustment must be applied to each phase individually, this method may add computational overhead to the MCU and may affect real-time performance. To mitigate this, duty correction is executed at a slower rate than the main current and voltage control loop execution rate. Thus, this method incorporates the advantages of a unified current controller at a lower CPU resource requirement and the steady state current balancing capability of the individual current controller. This technique might introduce a slight response lag during rapid load transients, and it retains the fault-tolerant benefits of individual current controllers. Moreover, only the total current sensor requires high bandwidth, while phase current sensors can operate at lower bandwidths, reducing overall system cost.

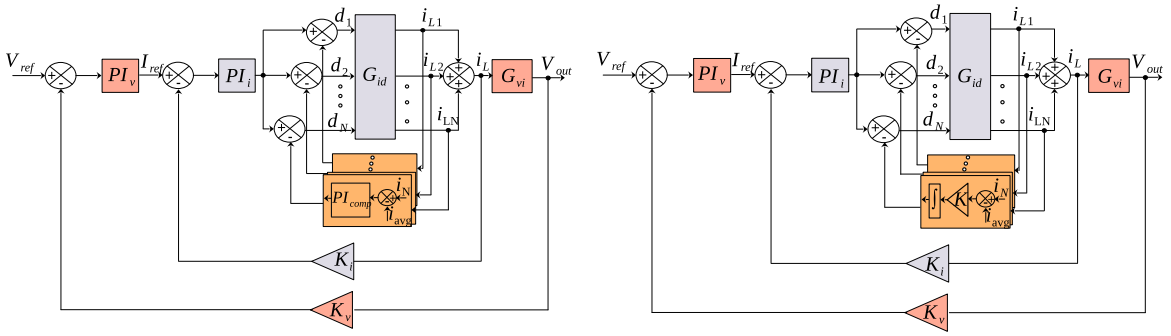


Figure 3. System model with (a) PI-based current imbalance compensator and (b) correction-factor-based current compensator

2.3. System description

The system employs a three-phase interleaved buck converter with GaN switches (S1T, S2T, S3T, S1B, S2B, and S3B). The control signals for the switches are generated using an NXP MC56F84789 DSC. The DSC houses two multichannel fast 12-bit ADCs that enable accurate current and voltage measurement. Its integrated peripherals and ample computational resources facilitate efficient real-time control in a compact and cost-effective implementation [19]. A block diagram of the proposed system is as in Figure 4.

The design specifications of the converter for the desired ratings are given in Table 1. The inductor and capacitor values are calculated according to standard design procedure [20], [21]. To support high-frequency operation with minimal core losses, inductors are wound on MP3310MPFC Metglas amorphous alloy cores, selected for their low loss characteristics up to 500 kHz, high saturation flux density, and thermal stability. Current sensing is performed using Hall-effect sensors, providing galvanic isolation, high bandwidth, and integrated fault outputs. Voltage feedback is obtained via resistor dividers, conditioned through differential amplifiers to ensure accuracy and noise immunity before ADC conversion, enabling precise control and protection of the converter.

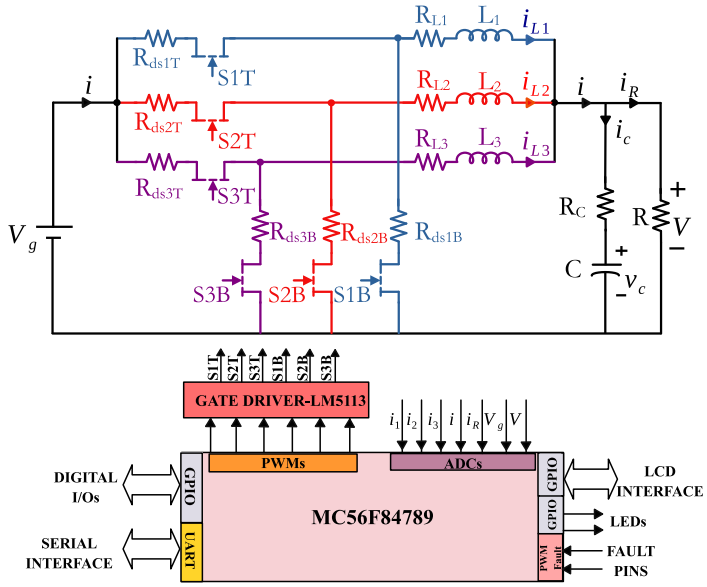


Figure 4. Block diagram of three-phase interleaved buck converter with digital controller

Table 1. Converter specifications

Symbol	Description	Desired value
P_o	Output power	1 kW
V_g	Input voltage	36 V
η	Efficiency	95% (assumed)
v	Output voltage	12 V
f_s	Nominal switching frequency	100 kHz
δ	Current ripple per phase	25% of average current
B_{max}	Maximum flux density of Metglas core	1.5 T
L_{ph}	Inductance per phase	11 μ H
C	Output capacitance	10 μ F
δV	Peak to peak ripple in output voltage	1 %
R_L	Measured DC resistance of inductor	10 mΩ
R_c	ESR of capacitor	6 mΩ

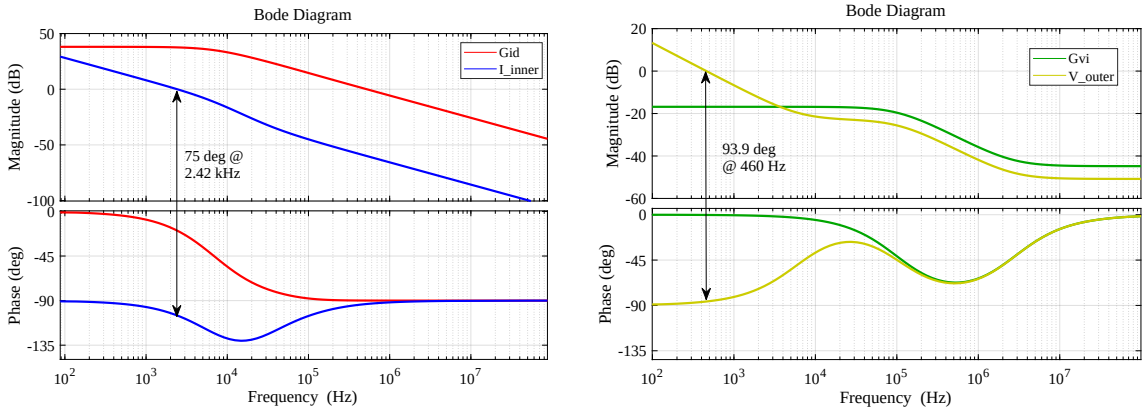
2.4. Controller design

The cascade control scheme is being adopted in this research work, with current being the inner loop and voltage as the outer loop. The standard cascade control design guidelines recommend setting the inner current loop bandwidth (BW_{cc}) up to one-tenth of the switching frequency (f_{sw}) and the outer voltage loop bandwidth (BW_{vc}) up to one-fifth of the current loop bandwidth. This hierarchical structure ensures an effective decoupling between the two control loops so that each could be individually tuned, allowing the inner loop to respond significantly faster than the outer loop. The controller parameters are selected such that the bandwidth of the inner current loop is approximately 2.42 kHz. Thus, the coefficients of the inner current regulating controller are selected as Kp = 0.001 and Ki = 200 to attain the desired phase margin of 75°. The outer voltage loop control parameters are selected as Kp = 0.5 and Ki = 20000 with a bandwidth of 460 Hz with a phase margin of 90°. The bode plot of current loop G_{id} and voltage loop G_{vi} is generated using MATLAB as in Figures 5(a) and 5(b). For digital implementation, the discrete-time transfer functions of the compensated system with a sampling period of 10 μs.

2.5. Digital implementation

The practical deployment of the proposed control strategies necessitates a robust digital implementation framework to translate theoretical control laws into real-time hardware operation. Digital implementation plays a crucial role in ensuring accurate current regulation, synchronized phase operation, and reliable performance under dynamic load conditions. However, achieving this in a multiphase converter introduces challenges such

as precise timing coordination, sampling synchronization, computational latency, and peripheral resolution constraints. This section presents the digital implementation architecture, outlining the adopted current sampling methodology, PWM generation scheme, and resolution considerations, interrupt scheduling, and software-level synchronization mechanisms required for stable and deterministic real-time control.



(a) (b)

Figure 5. Bode plot of (a) current loop and (b) voltage loop

2.5.1. Current sampling techniques

Accurate current sampling is essential for precise current control and fault detection in digitally controlled power converters, as measurement errors can affect duty cycle adjustments and improper load sharing in multiphase converters. One of the techniques is to sample the inductor current at the center of the PWM on-time, as shown in Figure 6(a). This requires separate ADC trigger pulses for each phase to capture average currents. Sensor latency introduces a delay between actual and measured currents, which can be compensated for by adjusting the sampling instant. This method requires PWM–synchronized triggering, and as the phase count increases, ADC sampling rate limitations may restrict its applicability.

The second method employs RC low-pass filters to extract the DC average inductor current, as shown in Figure 6(b). This technique lifts the board requirement of sampling instances in a switching cycle. Its key advantage is the ability to simultaneously sample all N-phase currents, making it suitable for complex multiphase systems. The ADC implementation in this paper utilizes the hardware filter scheme.

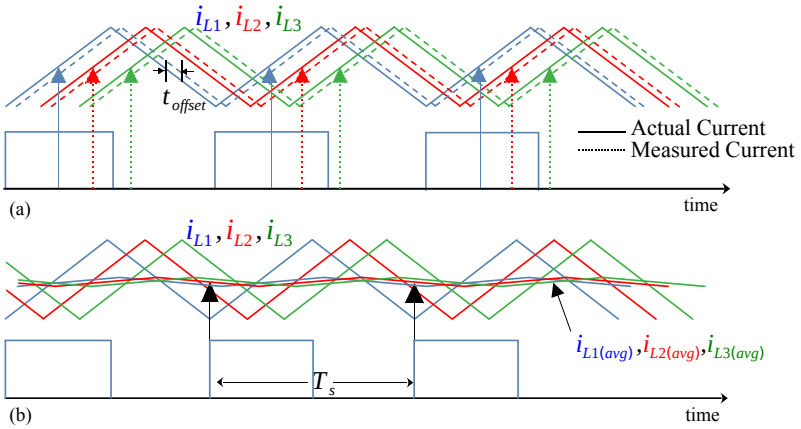


Figure 6. Current sampling techniques: (a) at center of PWM and (b) with hardware averaging

2.5.2. Software implementation

In digital control implementations, PWM resolution directly influences the granularity with which the duty cycle can be adjusted in real time. It is determined by the ratio of the timer clock frequency f_{clk} to the switching frequency f_{sw}, which defines the number of discrete timer counts available within one PWM period. For a controller with a fixed f_{clk}, the available timer counts per PWM period N decrease as f_{sw} increases, reducing the resolution. This inverse relationship limits duty cycle precision at higher switching frequencies, which is particularly critical for GaN-based converters requiring finer control. In the present implementation, the selected MCU operates with a clock frequency of 100 MHz and a switching frequency of 100 kHz, resulting in 1000 timer counts per PWM period. This defines the effective PWM resolution available for digital duty-cycle modulation in the proposed system.

In real-time control systems, precise synchronization between PWM signals, ADC sampling, and control loop execution is critical for accurate and efficient operation. The developed system employs a PWM timer counter with predefined comparison values to trigger synchronized events across all the three PWM generation modules. ADC conversions are initiated by PWM trigger signals at specific instances, followed by interrupt service routines (ISR) that process sampled data, compute control parameters, and update duty cycles. For the developed three–phase interleaved converter, three PWM submodules (SM0, SM1, SM2) of the PWMA module are used for PWM generation, with SM0 as the master submodule while SM1 and SM2 are phase-shifted by 120° and 240°, respectively, with respect to SM0 ensuring proper synchronization for interleaved operation. The VAL1 register in SM0 determines the PWM switching frequency f_{sw}, whereas VAL2 and VAL3 define the rising and falling edges respectively to control the duty cycle d(t). The VAL4 and VAL5 registers in SM0 were used to generate synchronization triggers (PWMA0_TRIG0 and PWMA0_TRIG1) for phase-shifting SM1 and SM2, ensuring an interleaved operation as indicated in Figure 7.

SM1_TRIG0 was used to trigger the ADC conversion at the center of the PWM cycle, ensuring accurate current sampling. Within the ADC ISR, parameters such as voltages and currents are measured, and the duty cycle is computed. After the computation, the updated duty cycle values are pre-loaded to the PWM value registers, which will be loaded during the next cycle. To ensure synchronized updates, the LDOK (Load OK) bits are set, allowing the updated duty cycle values to be loaded at the start of the next PWM cycle. The software is developed in NXP IDE (CodeWarrior) using embedded 'C' coding.

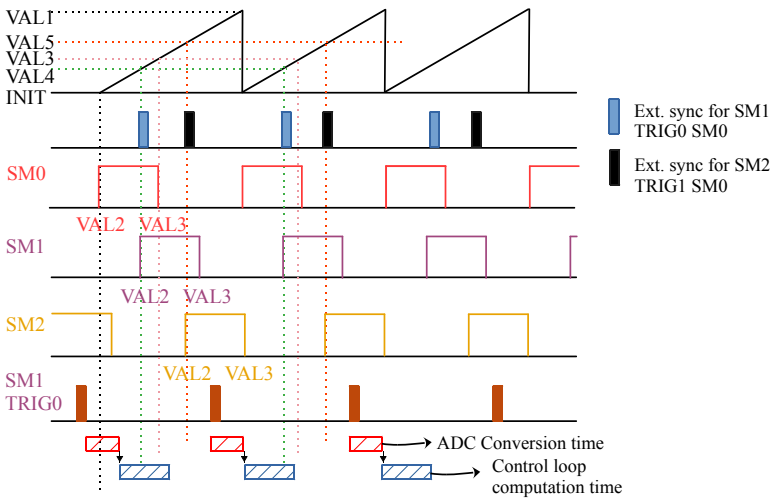


Figure 7. Timing diagram of digital control implementation

3. RESULTS AND DISCUSSION

This section evaluates the effectiveness of the proposed current balancing technique under steady-state and dynamic operating conditions, which is validated through detailed simulations and hardware experimentation. The converter performance is analyzed in terms of phase current distribution, duty cycle adaptation, and transient recovery during load variations.

3.1. Simulation results

The interleaved synchronous buck converter of Table 1 is simulated using MATLAB Simulink to evaluate the inherent current sharing capability and robustness of different current control strategies as in Figure 8. In simulation, a ±10% variation in the inductor resistance is introduced that would closely resemble hardware behavior. With unified current control, a significant current imbalance is observed across phases, with average phase currents of 19.31 A (phase 1), 17.99 A (phase 2), and 16.74 A (phase 3) against the expected 18.01 A, and a ripple current of 7.24 A as in Figure 9(a). This will lead to a higher temperature in the neighborhood of phase 1 traces compared to phase 3. Also, the stress on the phase 1 switches will be comparatively higher and the situation will worsen as the load current increases.

In contrast, the individual current control technique achieved uniform current sharing, with an average of 18.01 A per phase and a ripple current of 7.25 A as in Figure 9(b). Current balance was maintained even under transient conditions, demonstrating robustness and dynamic response. However, the implementation of this technique in the digital domain demands huge computational resources.

The decoupled current imbalance compensator exhibits transient behavior similar to unified control, but the imbalance loop corrected deviations within 2 ms, achieving balanced steady-state currents comparable to individual control as in Figure 9(c). This approach ensures current balance, avoiding thermal hotspots as the thermal time constant will be higher. Due to even temperature distribution, it is possible to achieve better system performance. This confirms its effectiveness in combining computational efficiency with accurate current balancing.

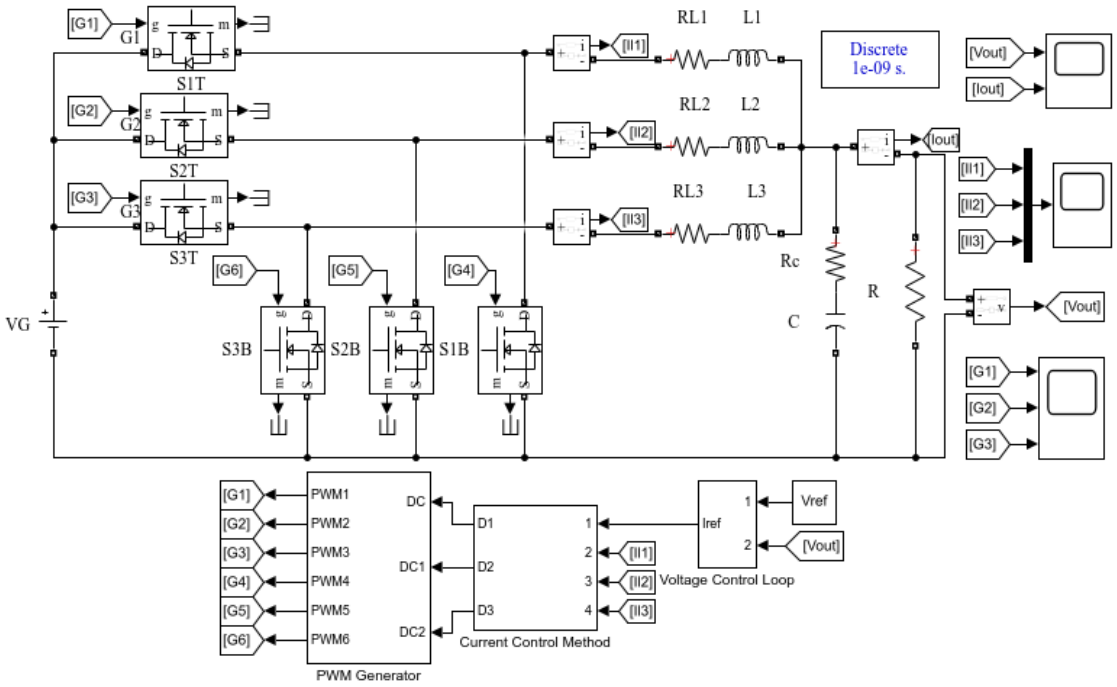


Figure 8. Simulink model of three-phase interleaved buck converter

3.2. Experimental results

The performance of various control techniques is validated on a in-house developed three-phase interleaved converter prototype featuring GaN GS61008P transistors driven by LM5113 half-bridge gate drivers [22], [23], ACS720 Hall-effect current sensors, voltage measurement circuitry, on a six-layer PCB measuring 19 cm x 39 cm. The experimental setup, including load, current/voltage probes, and digital storage oscilloscope (DSO), is shown in Figure 10. Dynamic response was tested with resistive loads, Figure 10(a), while real-time performance was validated using a 220 AH Li-polymer battery, Figure 10(b). Software development was carried out in CodeWarrior V10.4 IDE using embedded C programming, with the component inspector simplifying initialization of modules like PWM, ADC, timers, and interrupts. Controller is programmed via JTAG, enabling

efficient debugging, while FreeMASTER 3.2, integrated with CodeWarrior, provided real-time data acquisition, system analysis, and debugging [24].

When the reference is set to 8 V, the converter output is regulated to 8 V and delivers a power of 296 W. To check the transient performance, the reference is given a step from 8 V to 12 V. From Figure 11(a),the it can be observed that the output reached a steady-state value of 12 V within 1.5 ms, delivering a load of 648 W. The experiment is repeated with a sudden decrease of reference from 12 V to 8 V, and the same performance figures are observed as in Figure 11(b). This experiment helped to conclude that the outer loop is able to track and regulate the output voltage irrespective of inner current loop scheme.

To validate the inner current loop behaviour using unified, individual, and decoupled correction factor-based compensator current control techniques, all the phase currents are measured and presented in Figures 12 and 13. From Figure 12(a), it can be observed that the unified current controller results in current imbalances, and is consistent with simulation results. The measured average phase currents of 21.17 A, 18.67 A, and 20.17 A are observed against the expected 20.0 A per phase current. With the individual current controller, these imbalances are minimized, as shown in Figure 12(b), validating the simulation outcomes. The average phase current variation observed in each phase is 0.1 A ($<$0.5%), leading to the best performance. However, the computational complexity is found to be very high. Similar improvements are observed using the decoupled correction factor-based compensator current control technique, where current balancing is achieved as shown in Figure 12(c). However, the time taken for transients to die out is higher compared to an individual controller. This scheme provides a huge computational benefit against the individual controller.

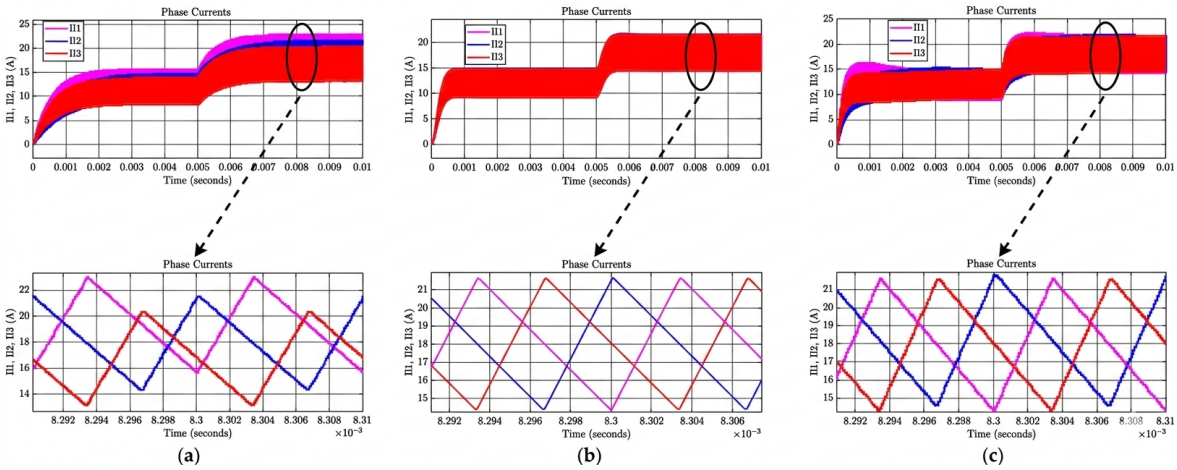
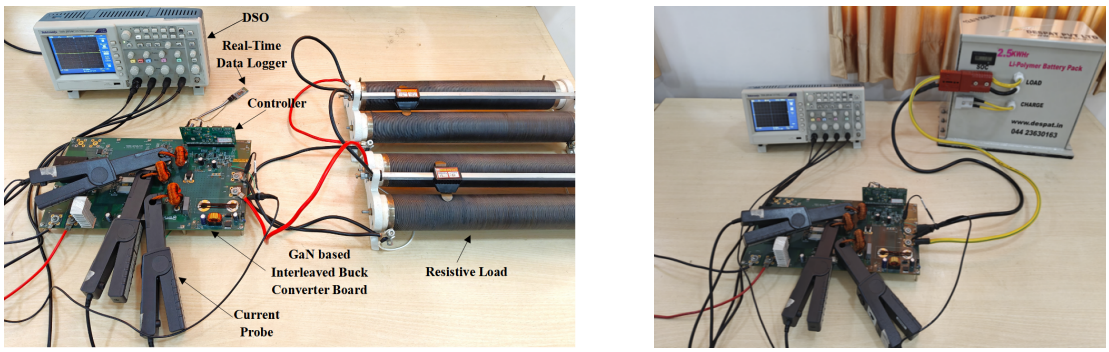
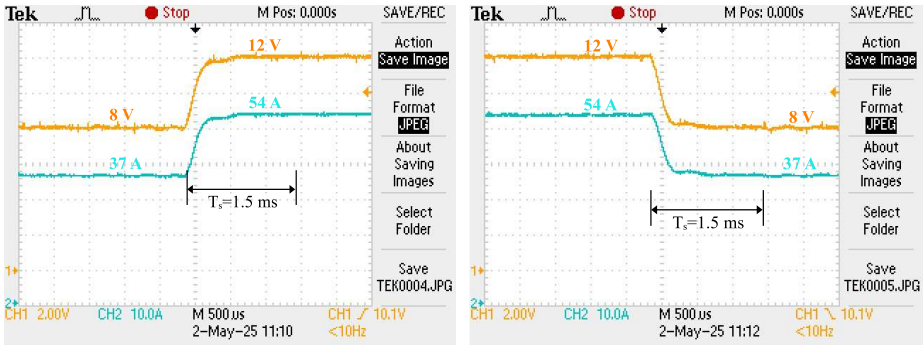


Figure 9. Inductor currents with different current control techniques: (a) unified controller, (b) individual controller, and (c) decoupled current imbalance compensator



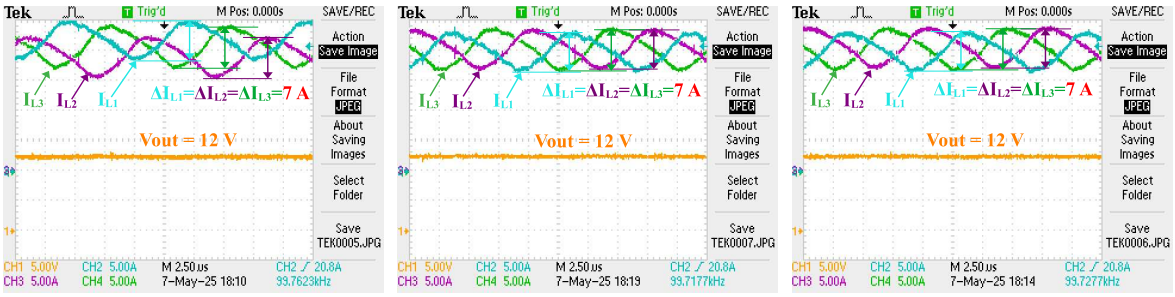
(a) (b)

Figure 10. Experimental setup with (a) resistive load and (b) battery



(a) (b)

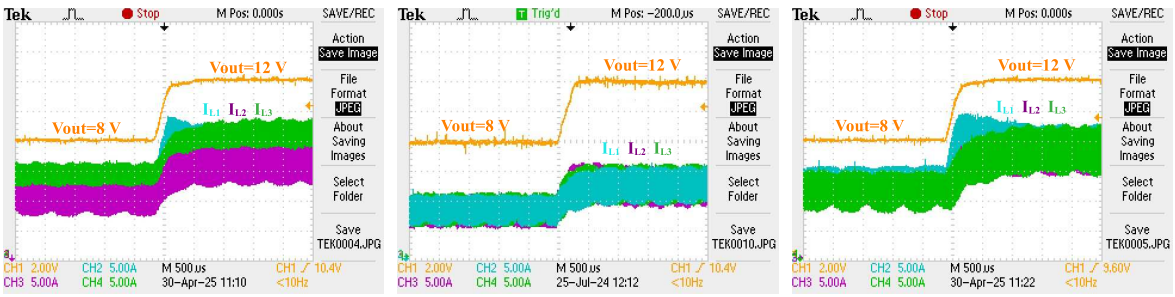
Figure 11. Output voltage and current during (a) step rise response and (b) step fall response



(a) (b) (c)

Figure 12. Steady state inductor currents with different current control techniques: (a) unified current controller with phase current imbalance, (b) individual current controller with balanced phase currents, and (c) decoupled current imbalance compensator with balanced phase currents

Figure 13(a) shows that the unified current controller exhibits current imbalance during both transient and steady-state operation. In contrast, the individual current controller maintains balanced phase currents throughout the operation, as illustrated in Figure 13(b). With the decoupled current imbalance compensator, transient imbalances similar to the unified control are observed initially; however, the controller compensates within 2 ms, achieving balanced current sharing in steady-state operation, as shown in Figure 13(c). For the same controller gain, from the measurements, it can be observed that in the individual controller, there is no overshoot. However, sufficiently high overshoot is observed in the unified control technique and slight overshoot in the decoupled compensator technique.



(a) (b) (c)

Figure 13. Transient response with different current control techniques with a voltage reference step from 8 V to 12 V: (a) unified controller, (b) individual controller, and (c) decoupled current imbalance compensator

To ensure the real-time responsiveness of the system, it is crucial to assess the computational load introduced by various current control strategies. Each control method differs in terms of the number of mathematical operations required per PWM cycle, and hence, their total execution time. The execution time for each method is derived based on the contribution of key computational steps, namely: the current scaling time (t_{cs}), voltage scaling time (t_{vs}), voltage controller execution time (t_{vc}), current controller execution time (t_{cc}), duty cycle scaling time (t_{ds}), duty correction time (t_{dc}) (in decoupled imbalance compensator technique), PWM compare value update time ($t_{PWMcomp}$), and PWM register update time (t_{update}). The execution time of each computation step, independent of the type of the current control technique, using fixed-point arithmetic, is summarized in Table 2.

The computational load and its effect on controller performance are summarized in Table 3 for a three-phase (N = 3) interleaved converter. The unified current controller results in lower CPU usage compared to running individual controllers for each phase. The decoupled current imbalance compensator approach provides a balanced solution: if the duty correction factor is updated at a slower rate than the compensation ISR, it enables effective current sharing while maintaining steady-state efficiency and reducing processor load, making it suitable for low-end DSCs. However, if the duty correction factor is updated at the ISR rate, computational demands increase, though they remain lower than that of the fully individual controller.

Table 2. DSC computation time for control loop execution step

Computation step	Execution time (ns)
Current scaling (t_{cs})	120
Voltage scaling (t_{vs})	80
Voltage control computation (t_{vc})	850
Current control computation (t_{cc})	780
Duty cycle scaling (t_{ds})	110
Duty correction (t_{dc})	982
PWM compare value update ($t_{PWMcomp}$)	160
PWM register update (t_{update})	80

Table 3. Comparison of computation time and peak efficiency for current control techniques

Current control technique	Analytical formula for computation time	Computed time (μs)	Actual time (μs)	Peak efficiency (%)
Unified	$t_{\text{unified}} = t_{cs} + t_{vs} + t_{vc} + t_{cc} + t_{ds} + t_{\text{PWMcomp}} \cdot N + t_{update}$	2.34	2.32	98.2478
Individual	$t_{\text{individual}} = t_{cs}N + t_{vs} + t_{vc} + t_{cc}N + t_{ds}N + t_{\text{PWMcomp}}N + t_{update}$	4.36	4.32	99.2514
Decoupled current imbalance compensator (Fast at Ts)	$t_{\text{decoupled fast}} = t_{cs}N + t_{vs} + t_{vc} + t_{cc} + t_{ds}N + t_{\text{PWMcomp}}N + t_{update} + t_{dc}N$	3.87	3.83	99.2514
Decoupled current imbalance compensator (Slower than Ts)	$t_{\text{decoupled slow}} = t_{cs}N + t_{vs} + t_{vc} + t_{cc} + t_{ds}N + t_{\text{PWMcomp}}N + t_{update}$	2.88	2.84	99.2514

Figure 14(a) presents the measured efficiency variation for the three current control techniques. Peak efficiencies of 99.2514% are achieved with individual controllers and a decoupled correction factor-based compensator current control technique, while the unified controller reached 98.2478%. Efficiency degradation at higher loads is primarily due to an increase in inductor DC resistance with temperature, whereas theoretical models assumed constant resistance. Additionally, GaN devices, while offering superior switching performance, experience significant reverse conduction losses as reverse current flows through the channel rather than a body diode, resulting in higher voltage drops (2–4 V). During DCM, bottom switches were disabled to prevent reverse current from the load, forcing GaN devices to conduct in freewheeling mode, where even brief reverse conduction periods at high switching frequencies contribute to notable losses, especially at light and medium loads.

The expected control loop execution times for various control strategies from N = 2 to N = 8 are plotted in Figure 14(b). It is observed that the unified control method maintains a consistently low execution time, making it highly suitable for high-phase-count systems. In contrast, the individual current control approach exhibits a linear and significant increase in execution time with the number of phases, which can impose

substantial computational burdens on the processor. The decoupled correction factor-based compensator current control strategy provides a compromise between scalability and control accuracy. When the duty cycle correction is executed in a slow ISR, the execution time variation with the number of phases is minimal. However, when duty cycle correction is implemented in fast ISR, the computational load scales with the phase count. Despite this, the increase remains considerably lower than that observed with individual current control, demonstrating a more efficient use of computational resources while still achieving improved current regulation. A comparison between different current control techniques considering control aspects, implementation complexity, and response time is discussed in detail in Table 4.

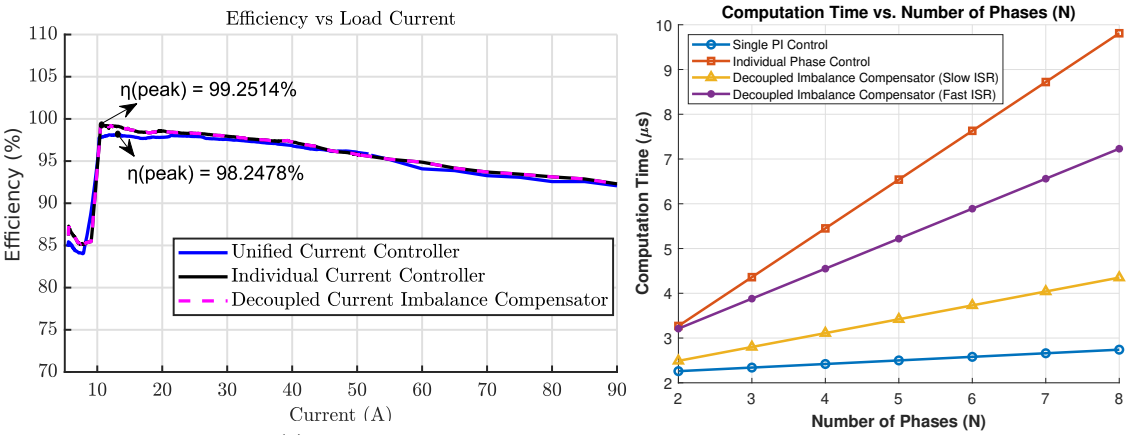


Figure 14. The performance of proposed system: (a) efficiency variation under unified, individual, and decoupled current imbalance conditions, and (b) computation time versus the number of phases

Table 4. Comparison of computation time and peak efficiency for current control techniques

Parameter	Unified current controller [25]	Individual current controller [26], [27]	Decoupled current imbalance compensator [11], [15]
Control structure	One controller regulates overall current	Each phase has its own dedicated current controller	Each phase has its own dedicated current controller
Duty cycle generation	Common duty cycle for all phases	Independent duty cycles per phase	Common base duty cycle with per-phase correction factors
Current balance	Achievable only if parasitic elements in each phase are equal	Ensures equal current distribution irrespective of circuit mismatches	Ensures equal current distribution irrespective of circuit mismatches
Dynamic response	Slower, with overshoot especially during transients	Faster, and no overshoot as each phase reacts independently	Faster than unified but slower than individual control with less overshoot
Complexity	Simple	High; requires multiple controllers and coordination	Moderate
Fault tolerance	Failure in one phase affects the entire system	If one phase fails, remaining phases continue operation	If one phase fails, remaining phases continue operation
Component count	Single current sensor is sufficient	Current sensors required for each phase	Current sensors required for each phase
Computational load	Low; suitable for low-power microcontrollers	High; requires high-performance controller	Moderate; suitable for mid-range controller
Thermal management	Uneven heating due to current imbalance	Improved due to equal power sharing	Improved due to per-phase current balancing
Cost	Low due to simple control and fewer sensors	High due to multiple current sensors	Moderate; sensors required but lower bandwidth
Computation time (three-phase)	Low (2.32 μs)	High (4.32 μs)	Moderate (2.84 μs)
Scalability	Easily scalable with minimal CPU overhead	Complexity increases significantly with phases	Scalable with slight increase in complexity

4. CONCLUSION

This paper demonstrates that the current control strategy selection has a decisive impact on current sharing accuracy, computational burden, and scalability in MCU-based multiphase DC-DC converters. Through detailed simulation and experimental validation on a three-phase interleaved buck converter, it is shown that current imbalance caused by practical non-idealities cannot be effectively mitigated using a unified current control approach, despite its low execution time. The unified current controller offers minimal computational overhead and is therefore suitable for low-cost or low-power microcontroller platforms where processor resources are severely constrained, and moderate current imbalance can be tolerated. However, its lack of per-phase regulation limits its applicability in high-reliability or high-power density systems. From the experiment, it can be observed that unified controller exhibits limitations like unequal thermal distribution and overshoot during the dynamic conditions, resulting in limited use in practical scenarios. The individual current control strategy achieves the best current sharing and transient performance, making it appropriate for applications demanding precise phase-level regulation, such as high-performance power drive systems, albeit at the expense of significantly increased computational complexity. The major observations are uniform thermal distribution and optimal dynamic performance, matching the simulation results.

The decoupled correction factor–based current imbalance compensator provides an effective compromise between performance and implementation cost. By separating voltage regulation from current imbalance correction, this approach achieves current sharing performance comparable to individual control while maintaining substantially lower processor utilization. As a result, it is particularly well-suited for mid-range MCU or DSC platforms in scalable multiphase power converters, where a balance between real-time feasibility, efficiency, and reliability is required. Also, it can be seen that the current imbalance in each phase lasts for a very short duration, resulting in uniform thermal distribution in the system. This results in a higher system efficiency along with optimal dynamic performance. Based on the presented results, unified control is recommended for cost-sensitive, low-phase systems, individual current control for high-performance applications with sufficient computational resources, and decoupled current imbalance control for practical high-power multiphase converters requiring scalability and efficient MCU implementation. As the technology is growing and miniaturization is a need of the day, it is very important to increase the converter switching frequencies. It is important to have a cost and performance balance; for lower operating frequencies (a few hundred kHz) it is optimal to choose the MCU/DSC architecture. However, when the operating frequency is increased beyond a few kHz, it is desirable to design a converter with FPGAs, resulting in a higher system cost.

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AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

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C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal Analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject Administration
Fu : **Fu**nding Acquisition

CONFLICT OF INTEREST STATEMENT

The authors declare no conflict of interest.

DATA AVAILABILITY

Data availability is not applicable to this paper as no new data were created or analyzed in this study.

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