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Grid-connected battery energy storage system using interleaved bidirectional buck/boost converter and 3-level SVPWM inverter

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ABSTRACT

This study presents a high-performance grid-connected battery energy storage system architecture designed to overcome the trade-off between DC-side current ripple and AC-side power quality. The proposed system synergistically integrates an interleaved bidirectional buck/boost converter, a three-level neutral-point clamped inverter, and an optimized LCL filter under a unified control strategy based on space vector pulse width modulation. Unlike conventional topologies that prioritize either subsystem individually, this integrated approach simultaneously minimizes battery current stress and ensures strict grid compliance. Extensive simulations in MATLAB/Simulink demonstrate that the proposed control strategy achieves a total harmonic distortion (THD) of just 2.93%, significantly outperforming the 40.25% THD of conventional two-level inverters and surpassing recent state-of-the-art benchmarks. The system exhibits robust dynamic response during rapid charging/discharging transitions and maintains stability under grid disturbances, such as 20% voltage dips. These results validate the architecture as a viable, high-efficiency solution for integrating modern renewable energy.

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1. INTRODUCTION

The overall transition to renewable energy sources (RES), such as solar and wind energy, has introduced new challenges for the stability of the power grid due to their inherent intermittency [1], [2]. To mitigate these problems, battery energy storage systems (BESS) emerged as a key technology to improve power management, improve energy quality, and provide auxiliary services such as frequency regulation and load peak shaving [3]. However, BESS integration into the power grid requires efficient electronic interfaces to facilitate bidirectional energy transfer, maintain high efficiency, and ensure compliance with grid regulations [4].

Research on BESS has extensively focused on optimizing specific subsystems rather than the entire system. For example, improvements in the DC/DC conversion stage have introduced redundancy-based architectures to ensure continuous operation under fault conditions [5], [6] and multi-port topologies integrating battery management functions for enhanced flexibility and modularity [7], [8]. While these approaches improve the reliability of the DC stage, they often overlook the challenges of interfacing with AC systems and the synergy required with multilevel inverters for efficient grid integration.

On the AC side, the three-level neutral-point clamped (NPC) inverter has become a standard solution for medium-voltage applications due to its ability to reduce harmonic distortion and improve voltage

quality [9]. Its performance is highly dependent on advanced modulation strategies such as space vector pulse width modulation (SVPWM) and fault-tolerant control methods to ensure stable operation under abnormal conditions [10], [11]. Additionally, grid code compliance typically requires the use of high-order passive filters, with the LCL filter being the preferred choice for mitigating switching harmonics. Although effective, these filters introduce resonance issues that necessitate robust design and damping strategies [12]–[14].

Despite the progress in individual subsystems, few works have addressed the integration of interleaved bidirectional DC/DC converters, NPC inverters, and LCL filters under a unified control strategy. As an example, defining the architecture where the NPC inverter is combined with a non-interleaved DC/DC converter [15] does not provide a thorough enough level of current ripple minimization at the battery, which will result in additional deterioration of the battery. However, the work done investigating the combination of an interleaved converter and a conventional two-level inverter [16] has shown to decrease ripple; however, this approach causes an increase in voltage across the switches and reduces harmonic performance when compared to multi-level topologies. The closest study to this work combines an interleaved converter with an NPC inverter for renewable applications; however, it reports a total harmonic distortion (THD) of 22.2%, indicating non-compliance with standards and a lack of coordinated control [17].

The state of the art demonstrates a specialization in research approaches, typically optimizing the DC/DC conversion stage or DC/AC stage, often at the expense of overall system performance. As a result, there remains a gap in the literature on the design and validation of a BESS architecture that synergistically integrates the four key technologies below: a bidirectional converter interleaved to minimize current ripple, a three-level NPC inverter to generate high-quality voltage, a rigorously synthesized LCL filter for grid interfacing, and a unified control strategy based on SVPWM. This work aims to fill this gap, proposing and analyzing such an integrated architecture, designed to simultaneously achieve high conversion efficiency and minimal harmonic distortion. This study provides a simulation-based, comprehensive validation to establish the theoretical benchmarks of feasibility and performance of the proposed architecture, thus establishing the essential groundwork for future prototyping and experimental analysis.

The remainder of this paper is structured as follows: section 2 presents the system architecture and modeling, section 3 details the control strategy, section 4 discusses simulation results, and section 5 concludes the study with key findings and future research directions.

2. SYSTEM DESCRIPTION

Figure 1 illustrates a BESS scheme connected to the proposed grid, featuring an interleaved bidirectional buck-boost converter, a three-level NPC inverter, and an LCL filter. The system consists of interconnected modules where the output voltage of the three-level inverter is supplied to the grid. The bidirectional converter regulates the DC link voltage and facilitates energy exchange between the battery and the grid. To ensure efficient power transfer and grid compliance, the inverter is controlled using SVPWM, which optimizes voltage utilization and minimizes harmonic distortion. The LCL filter is employed at the inverter output to attenuate high-frequency harmonics, ensuring a smooth grid current waveform. Additionally, a control strategy comprising DC-DC and inverter control loops is implemented to regulate energy flow, maintain grid synchronization, and enhance overall system stability.

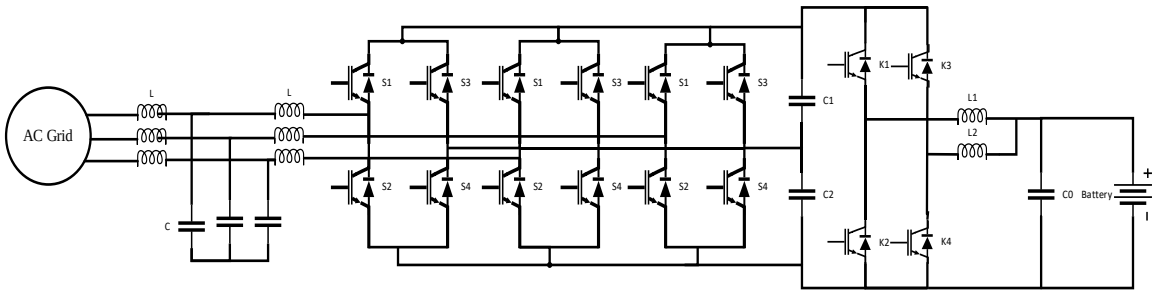


Figure 1. Schematic of the proposed grid-connected BESS with an interleaved bidirectional converter, three-level NPC inverter, and LCL filter

2.1. Interleaved bidirectional buck/boost converter

The interleaved bidirectional buck/boost converter is a pivotal component in the proposed grid-

connected BESS, facilitating efficient bidirectional energy transfer between the battery and the DC link. This converter architecture employs an interleaving technique, which involves paralleling multiple converter phases that operate with specific phase shifts relative to each other. Such a configuration offers several advantages over traditional single-phase converters, including reduced current ripple, enhanced efficiency, and improved thermal performance [18]. In the context of the proposed system, the interleaved bidirectional buck/boost converter comprises two parallel bidirectional buck/boost stages, each operating 180 degrees out of phase. This phase-shifted operation effectively reduces the input and output current ripples, minimizing the size of passive components such as inductors and capacitors. The reduction in current ripple minimizes electromagnetic interference (EMI) and results in lower conduction losses, thereby contributing to higher overall efficiency [19]. The converter operates in two primary modes:

2.1.1. Boost mode (battery discharging)

In this mode, the converter steps up the battery voltage to a higher DC link voltage, enabling power delivery from the battery to the grid. Each phase's inductor stores energy when its corresponding switch is active and releases it to the DC link when the switch is off, effectively boosting the voltage [20]. The equivalent circuit configuration and current paths for this mode are illustrated in Figure 2. In this mode, K2 & K4 are ON and K1 & K3 are OFF. D2 & D4 are reverse biased, D1 & D3 are forward biased. The current inductors L1 & L2 increase linearly. To deliver electricity to the load, the battery discharges.

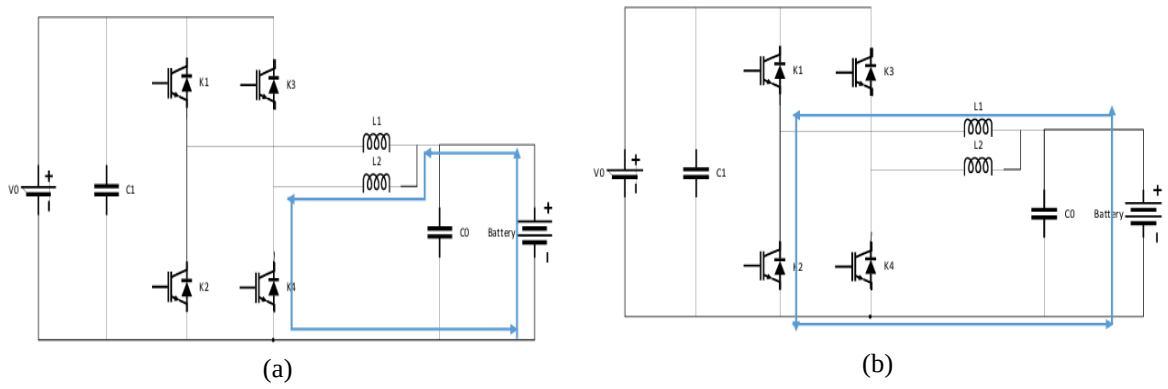


Figure 2. Boost converter voltage: (a) K4 is ON and (b) K2 is ON

2.1.2. Buck mode (battery charging)

Here, the converter steps down the DC link voltage to a lower voltage suitable for charging the battery. The energy from the DC link is transferred to the battery through the inductors, which regulate the charging current to ensure battery safety and longevity [21]. The circuit operation during the charging phase is depicted in Figure 3.

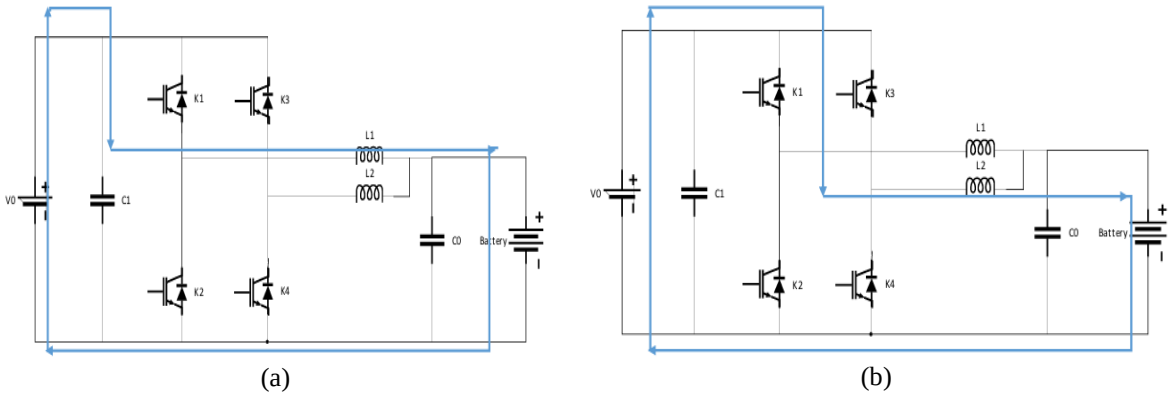


Figure 3. Boost converter voltage: (a) K1 is ON and (b) K3 is ON

In this mode, K1 and K4 are ON and K2 & K3 are OFF. D1 & D4 are reverse-biased biased and D2 & D3 are forward-biased. The power flow is reversed from the load to charge the battery. The inductor current will turn negative as the power flow reverses. The battery is charged from the load during regenerative braking in this mode. Inductor and capacitor values can be calculated using (1) and (2).

$$L_1 = L_2 = \frac{D.(1-D).V_0}{\Delta I_L.f_{sw}} \quad (1)$$

$$C_1 = \frac{D.I_0}{2.f_{sw}.\ \Delta V_{C1}} \quad (2)$$

Where D duty ratio, f_{sw} switching frequency, ΔI_L the current ripple through interleaving inductors L_1, L_2, and ΔV_{C1}, the voltage ripple across the DC-link capacitor C_1.

2.2. Three-level inverter

A three-level H-bridge inverter 3L-HBI is a power conversion topology that generates three distinct output voltage levels: +Vdc/2, 0, and -Vdc/2 [22]. This architecture is widely used in renewable energy systems, motor drives, and battery energy storage systems (BESS) due to its ability to produce a high-quality AC output. The inverter has two H-bridge legs containing four power switches (IGBTs or MOSFETs). By properly controlling these switches, three output voltage levels can be achieved: (2 → +Vdc/2; 1 → 0. V; 0 → −Vdc/2). The specific switching states corresponding to these voltage levels are detailed in Table 1 [23].

Table 1. Switching states and corresponding voltage levels in 3L-HBI

Item	Switch				Phase voltage	Leg status
	S_1	S_2	S_3	S_4		
1	ON	ON	OFF	OFF	+Vdc/2	2
2	OFF	ON	ON	OFF	0	1
3	OFF	OFF	ON	ON	-Vdc/2	0

2.3. LCL filter integration

To improve the overall performance and reduce harmonic distortion, an LCL filter is integrated into the system. This filter helps attenuate high-frequency harmonics produced during the switching operations of the inverter, thereby enhancing the power quality of the system. The LCL filter consists of a combination of inductors and a capacitor, forming a series configuration that not only filters out high-frequency noise but also minimizes the load on the grid, ensuring cleaner power delivery [24]. The LCL filter parameters are determined using well-established design methodologies to ensure optimal performance [25]. This design philosophy is based on a significant trade-off: the capacitor value is usually limited to consume a small fraction of nominal reactive power, while the inductors are shaped for adequate harmonic attenuation. The most important thing is that the components are chosen to keep the reception frequency of the filter carefully in the selected range, above the bandwidth of the controller to avoid volatility, but significantly below the switching frequency to ensure effective filtering. The values of the inductors, the capacitor, and the resistor are computed as (3) [26].

$$\begin{cases} L_i = \frac{V_{dc}V_g}{16{,}97.f_{sw}.P_0} \\ L_g = \frac{\omega V_g^2}{0{,}05.P_0.\omega_{sw}^2}\left(1+\sqrt{\frac{1}{k_\alpha^2}}\right) \\ C = \frac{0{,}05.P_0}{\omega.V_g^2} \\ r_c = \frac{\omega V_g^2}{0{,}15.P_0.\omega_0} \end{cases} \quad (3)$$

Where: $\omega_{s\omega}$ is the angular switching frequency ($\omega_{s\omega} = 2\pi f_{s\omega}$), ω is the angular fundamental frequency ($\omega = 2\pi f$), ω_0 is the angular resonance frequency ($\omega_0 = 2\pi f_0$).

3. MANAGEMENT CONTROL

The control system is organized into two main loops: i) the grid control strategy loop and ii) the battery current control strategy loop.

3.1. Battery's current control strategy

The battery power control subsystem consists of a lithium-ion (Li-ion) battery connected to a three-level buck/boost converter, which regulates the power exchange between the battery and the DC bus. Li-ion batteries are chosen in this study due to their high energy density and efficiency, outperforming alternatives such as NiMH, lead-acid, and NiCd batteries. Since the battery voltage is influenced by both nonlinear current variations and the state of charge (SoC), it is modeled as a nonlinear function. The expression for the battery voltage V_{bat} is derived using (4) [27].

$$V_{bat} = V_{op} - R_{bat} * i_{bat} - \frac{k_b * Q * i_t}{Q - i_t} - \frac{k_b * Q * i_f}{Q - it} + A_b e^{B * i_t} \quad (4)$$

Where V_{op} is the open-circuit voltage, R_{bat} is the internal resistance, i_{bat} is open-circuit current, Q is battery capacity k_b is polarization constant, A_b is an exponential voltage, B is the actual charge current of the battery, and i_f is the filtered current of the battery. The polarization voltage, given by the term $\frac{k_b * Q * i_t}{Q - i_t}$ models the influence of the SoC on the battery's performance, including voltage drops and resistive losses, which affect efficiency and stability [28]. This loop controls the battery current and the power exchange between the battery and the DC link, ensuring that the battery current stays within safe operating limits, optimizing performance and efficiency, as illustrated in Figure 4. To prevent damage to the DC-bus capacitors, a voltage balancing control mechanism is employed to generate I_{ref}. This value is used as the reference for controlling the $I_{1,2}$ current through PWM signals.

The bidirectional functionality of this converter depends on the sign of I_{ref}. When $I_{ref} \leq 0$, the batteries are charged, and the converter operates in buck mode. Conversely, if $I_{ref} > 0$, the converter switches to boost mode, causing the batteries to discharge. The control signals are phase-shifted by 180°; specifically, there is a phase difference between PWM_{K2} and PWM_{K3}, as well as between PWM_{K1} and PWM_{K4} [29].

3.2. Grid control strategy

This loop is responsible for regulating the active and reactive power exchange between the inverter and the grid, ensuring that the output voltage from the inverter aligns with grid requirements for seamless integration, as illustrated in Figure 5. The inverter is controlled using SVPWM, which enhances DC bus voltage utilization, reduces harmonic distortion, and improves output voltage regulation. A phase-locked loop (PLL) synchronizes the inverter with the grid, ensuring precise power transfer and frequency stability [30].

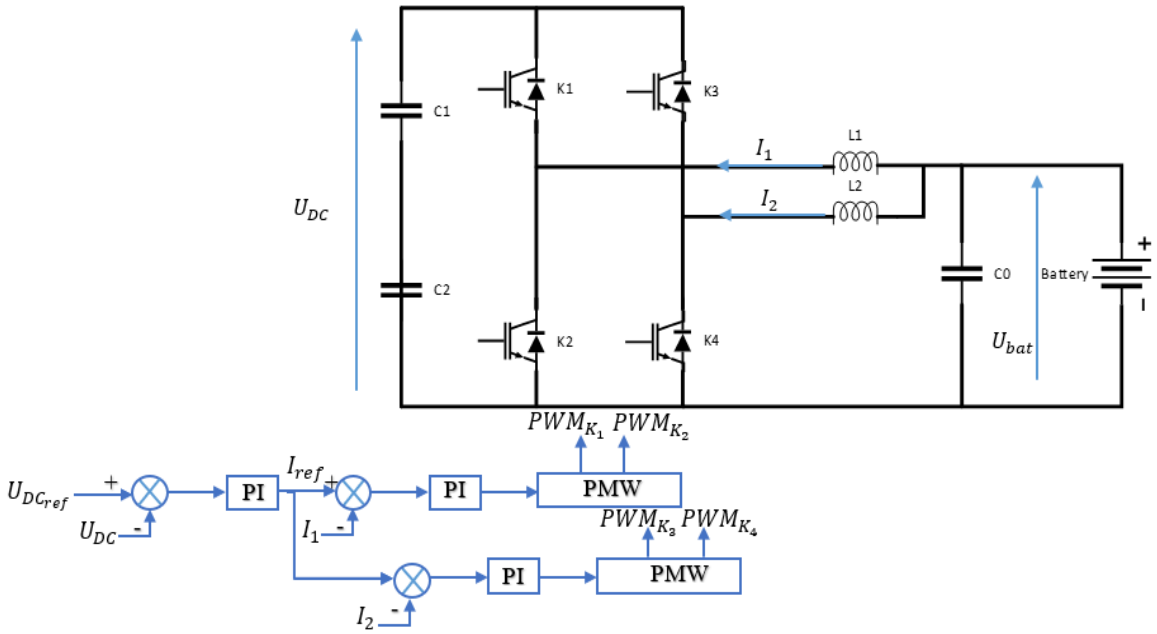


Figure 4. Battery current control and DC bus capacitor voltage balancing control method

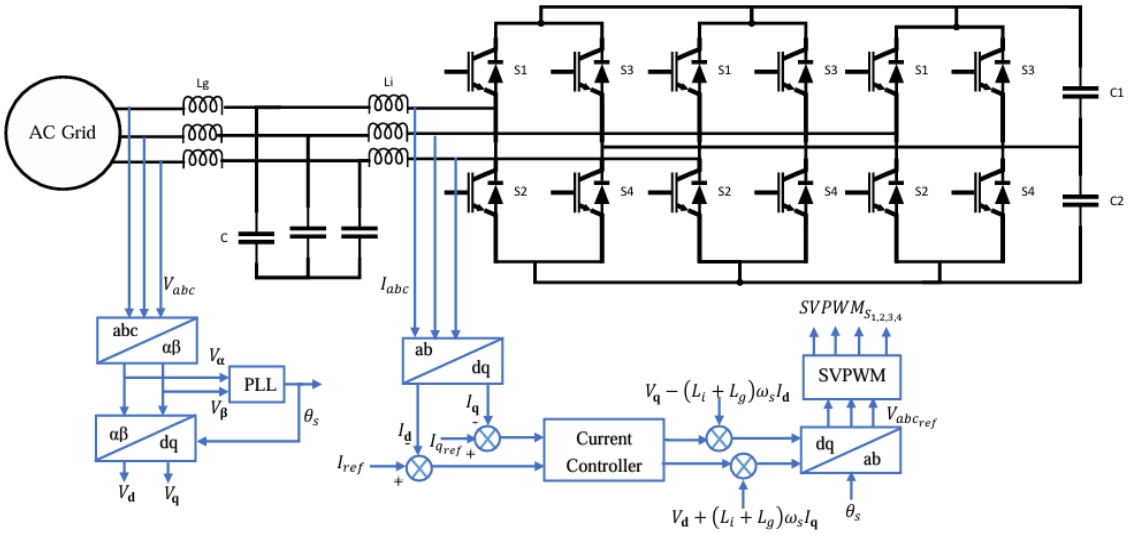


Figure 5. Grid voltage control using a three-level NPC inverter and LCL filter

3.2.1. Phase-locked loop (PLL)

The PLL is essential for grid synchronization, continuously monitoring the phase difference between the grid voltage V_g and the inverter output. It dynamically adjusts the inverter's phase to maintain synchronization, preventing phase mismatches that could degrade power quality or system efficiency [31].

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \cos \omega t & \sin \omega t \\ -\sin \omega t & \cos \omega t \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \tag{5}$$

3.2.2. SVPWM

The inverter's operation is regulated through the d-q coordinate system to control the root mean square (RMS) voltage, and the SVPWM technique is applied to generate the appropriate PWM signals for the inverter [32]. SVPWM is an advanced modulation strategy that enhances inverter performance compared to traditional sinusoidal PWM (SPWM). It improves DC bus voltage utilization, minimizes harmonic distortion, and enhances output voltage control. The output voltages of the inverter can be represented as vectors in a two-dimensional space with real (Re) and imaginary (Im) axes. Each possible switching state corresponds to a specific voltage vector in this coordinate system. The voltage space is divided into six distinct sectors. The reference voltage vector V_{ref} is positioned within one of these sectors based on its magnitude and angular position. To approximate the reference voltage, three adjacent voltage vectors are selected. A combination of active and zero vectors is then used to construct the desired output waveform. The time intervals for applying each selected vector are computed based on the reference voltage. These computed durations are then translated into PWM control signals that drive the inverter's switches [33].

3.2.3. Decoupled vector control

The decoupled vector control strategy is implemented using DQ-axis control, where the system's three-phase currents are transformed into a rotating reference frame. This approach simplifies control by independently regulating the direct (d) and quadrature (q) components of the current. As shown in Figure 6, proportional-integral (PI) regulators are used within the current control loops to ensure precise tracking of reference values. This method enhances dynamic performance, improves stability, and effectively decouples active and reactive power control, allowing for seamless grid integration. The current-loop regulators are developed based on (6) [34].

$$\begin{aligned} V_d &= -(L_i + L_g)\frac{di_d}{dt} - \omega_s(L_i + L_g)i_q + u_{gd} \\ V_q &= -(L_i + L_g)\frac{di_q}{dt} + \omega_s(L_i + L_g)i_d + u_{gq} \end{aligned} \tag{6}$$

4. RESULTS AND DISCUSSION

The proposed system was simulated using MATLAB/Simulink under various operating conditions to validate its performance, stability, and compliance with grid requirements. Given the complexity, cost, and safety considerations associated with the prototyping of high-power multilevel converter systems, a simulation-based approach provides a crucial first step in thoroughly analyzing dynamic behavior and the effectiveness of the system control strategy. The simulation framework integrates detailed models of the bidirectional interleaved buck/boost converter, three-level NPC inverter, LCL filter, and advanced control strategies, including SVPWM and decoupled DQ-axis control. To ensure accuracy, the system parameters were selected based on practical industrial standards, and the switching frequencies were optimized to balance efficiency and harmonic performance.

The results are organized to demonstrate: Dynamic response during charge/discharge transitions, highlighting DC-link voltage stability and current tracking. Grid synchronization via PLL, showing phase alignment under bidirectional power flow. The THD analysis is an effective parameter that must be considered to prove the efficiency of the multilevel inverter integration. The main parameters used for the proposed BESS architecture simulation are summarized in Table 2.

4.1. DC bus dynamic performance and stability

Figure 6 illustrates the current-time characteristics of a battery system undergoing sequential charge and discharge cycles over a 9-second timeframe. Three distinct operational phases are observable in the current waveform: During the initial charging phase (0-3 s), the battery maintains a constant -5 A current, following the standard sign convention where negative current indicates charging. The perfectly flat current profile demonstrates exceptional system stability, suggesting precise current regulation through either an advanced battery management system (BMS) or high-performance power electronics. The subsequent discharge phase (3-6 s) shows an immediate transition to +5 A (positive current denoting discharge), with the current magnitude mirroring the charging current exactly. This symmetrical behavior reveals several important system characteristics: the power converter's capability for seamless bidirectional energy flow, negligible system inductance that could cause current transients, and potentially the use of synchronous rectification techniques in the power stage. In the final charging segment (6-9 s), the current returns to -5 A, completing the full cycle. The identical current amplitude and profile between the two charging phases indicate highly reproducible electrochemical processes and stable power delivery conditions.

Table 2. Simulation parameters

Parameter	Symbol	Value
Grid voltage	V_g	480 V
Grid frequency	f_g	50 Hz
Switching frequency	f_{sw}	10 kHz
DC-link voltage reference	V_{dcref}	815 V
Interleaving inductors	L_1, L_2	1.5 mH
DC-link capacitors	C_1	4110 µF
Battery-side capacitor	C_0	120 µF
Inverter-side inductor	L_i	1.5 mH
Grid-side inductor	L_g	0.5 mH
Filter capacitor	C	22 µF
Damping resistor	r_c	0.5 Ω
Nominal voltage	V_{bat}	450 V
Nominal capacity	Q	280 Ah
Internal resistance	R_{bat}	15 mΩ

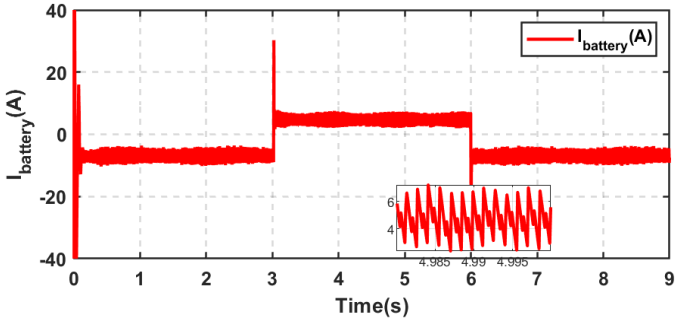


Figure 6. Current during charging and discharging

Figure 7 shows the evolution of the voltage across the battery terminals V_{bat}, which accurately reflects the electrochemical dynamics of the storage system as a function of current flow.

- Charging phase (0-3 s): During the initial charge at -5 A, the voltage is not perfectly stable. It shows a slight upward slope, rising from approximately 485.5 V to 486 V. This gradual increase is directly related to the increase in the battery's state of charge (SoC), which causes its open-circuit voltage to rise.
- Discharge phase (3-6 s): At t = 3s, when the system switches to discharge mode at +5 A, there is an immediate drop in voltage due to the internal resistance of the battery. Then, during this phase, the voltage shows a very slight downward slope. This is consistent with the gradual decrease in the battery's SoC as it supplies energy.
- Recharge phase (6-9 s): At t = 6s, the system switches back to charge mode. The voltage rises instantly due to the reversal of the current relative to the internal resistance, and resumes its slow upward slope, characteristic of the increase in SoC.

Observation of these subtle dynamics, including not only voltage jumps but also slopes related to the state of charge, confirms the excellent fidelity of the battery model used and the ability of the control system to operate on a non-linear and realistic model.

Figure 8 illustrates the regulation and stability of the DC bus voltage V_{dc}. The voltage is maintained with high precision at its set value of 815 V throughout the charge and discharge cycles. The zoomed sections highlight the transient response during power flow reversal at t = 3 s and t = 6 s. It is observed that the voltage deviation is controlled to approximately 15 V (approximately 1.8% of the nominal voltage) and is fully corrected within 150 ms, demonstrating the excellent dynamic performance and stability of the voltage regulator.

Figure 9 displays the output voltage waveform V_{CHB} of a three-level inverter utilizing SVPWM. The voltage exhibits characteristic three-level switching behavior, alternating between +500 V, 0 V, and -500 V, with the transitions occurring at high frequency to approximate the fundamental sinusoidal reference waveform. The clean, well-defined voltage levels demonstrate effective DC-link voltage utilization and proper implementation of the SVPWM algorithm, which optimally spaces the voltage vectors to minimize harmonic distortion. The time axis reveals the high switching frequency operation, with the pulse pattern carefully modulated to reduce output voltage THD while maintaining efficient switching losses. The absence of visible distortion or voltage imbalance in the waveform suggests the proper functioning of the capacitor voltage balancing mechanism and accurate implementation of the space vector modulation strategy.

Figure 10 illustrates the power exchange characteristics and voltage synchronization of a grid-connected inverter system during a 500 ms operational period. The CHB inverter voltage V_g maintains perfect phase alignment with the grid voltage throughout these power transitions, as evidenced by the undisturbed voltage waveform characteristics. This precise synchronization confirms the effectiveness of the implemented phase-locked loop (PLL) algorithm in maintaining grid phase tracking under varying power conditions.

Figure 11 demonstrates the dynamic response of a decoupled vector control system for grid-connected power converters, showing the d-axis and q-axis current components over a 9-second operational period. The d-axis current i_d closely tracks its reference $i_{d_{ref}}$ throughout the entire duration, maintaining stability during both steady-state and transient conditions. This precise tracking confirms effective regulation of the active power component, with the proportional-integral (PI) controller successfully compensating for system disturbances. The q-axis current i_q maintains near-zero values as intended ($i_{q_{ref}}$ = 0), demonstrating perfect reactive power control and achieving unity power factor operation. The precise current regulation in both axes validates the effectiveness of the park transformation and inverse transformation processes in the control scheme.

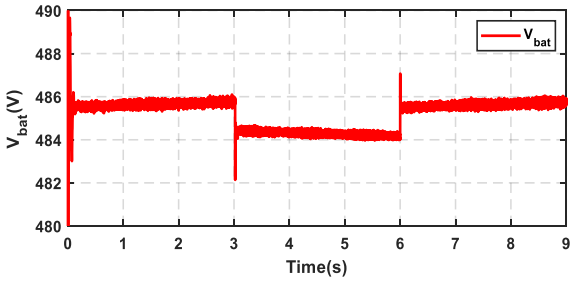


Figure 7. Battery voltage V_{bat} during charging and discharging

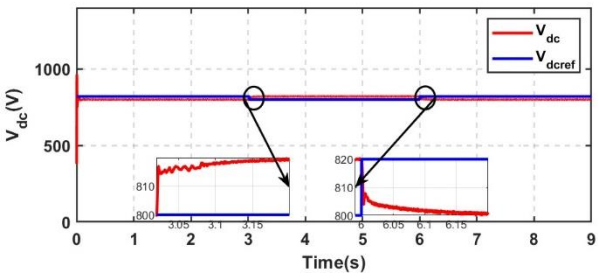


Figure 8. DC-link bus voltage V_{dc}

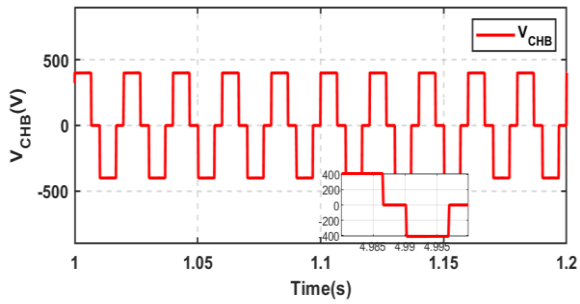


Figure 9. 3-level inverter output voltage

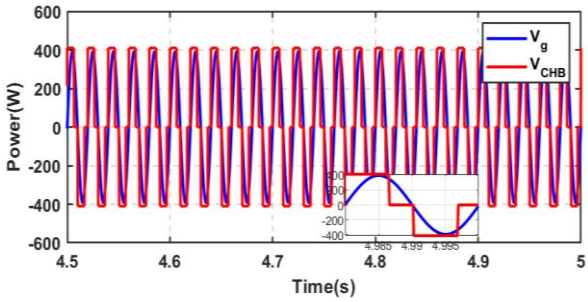
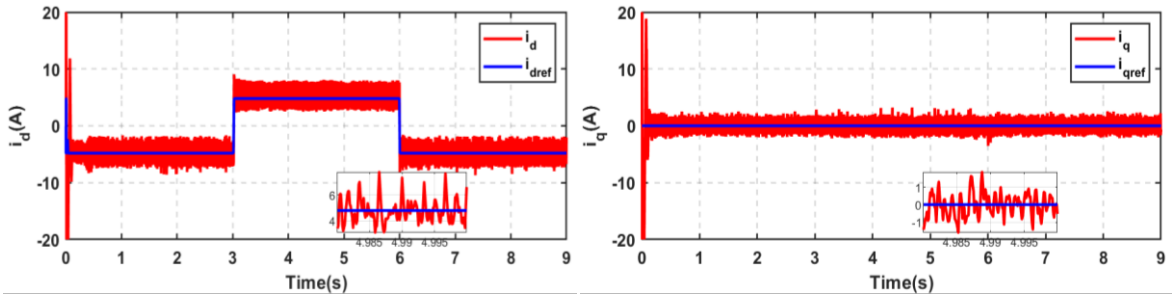


Figure 10. System synchronization with the grid via PLL

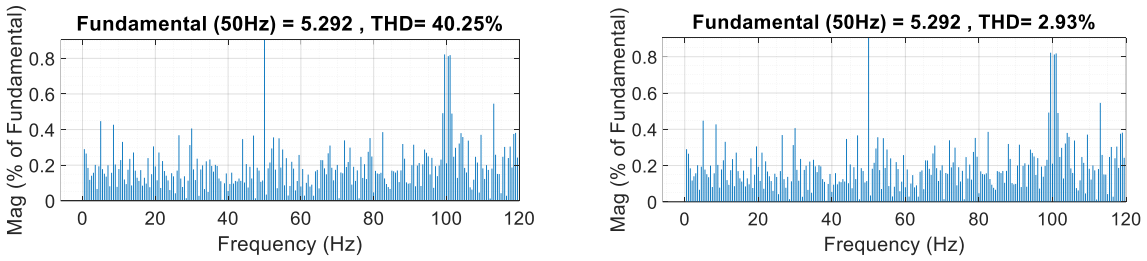


(a) (b)

Figure 11. Decoupled vector control (D-Q-axis control): (a) direct axis current i_d tracking its reference i_{dref} and (b) quadrature axis current i_a maintained at zero for a unity power factor

4.2. Comparative benchmark setup

To strictly evaluate the advantages of the proposed topology, a comparative analysis was performed with a conventional two-level inverter. To ensure a fair and scientifically valid comparison, both systems were simulated under strictly identical operating conditions. The control strategy involved both inverters (2 and 3 levels) being controlled using the same SVPWM control strategy and the same dissociated vector control. This allows the impact of the inverter topology to be isolated from the modulation algorithm. An identical 10 kHz switching frequency has been applied to both settings to ensure that harmonic switching appeared around the same frequencies. The two-level inverter was also equipped with an LCL filter. The components of this filter were sized using the same methodology and design goals as for the three-level inverter filter, adapting it to its specific DC bus voltage. The analysis of the THD of the current injected into the grid, an essential metric for evaluating power quality, was carried out for both configurations. Figure 12 presents the spectral analysis (FFT) of this current. Following the fair comparison approach defined above, the results demonstrate a clear superiority of the proposed topology. The current THD for the 3-level inverter is measured at 2.93%, while the conventional 2-level inverter has a THD of 40.25%. These measurements confirm the effectiveness of the multi-level topology in minimizing undesirable harmonic components while maintaining robust performance during operational transitions.

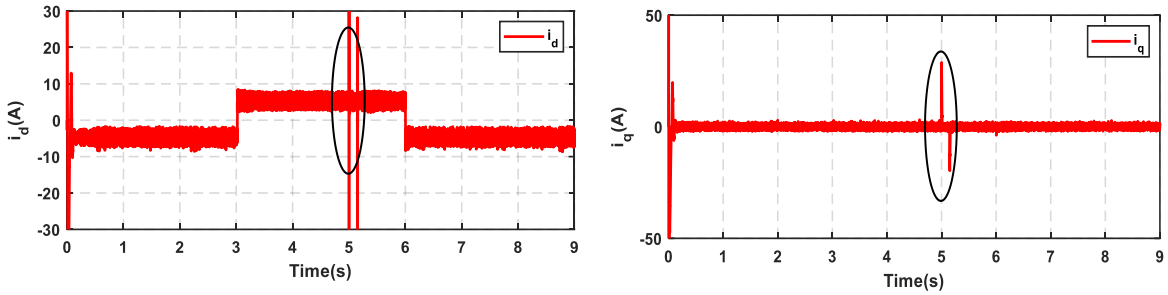


(a) (b)

Figure 12. Harmonic spectrum of grid current for a conventional and 3-level inverter: (a) conventional 2-level inverter showing 40.25% THD and (b) proposed 3-level NPC inverter exhibiting 2.93% THD

4.3. Robustness to grid disruptions

To assess the reliability and stability of the system under realistic network conditions, a robustness test was conducted. This test simulates a voltage dip, which is one of the most common disturbances on the electrical grid. The objective is to verify that the system can maintain a stable connection, precise power control, and perfect synchronization, according to the requirements of modern network codes (fault ride-through or FRT standards). A symmetrical voltage dip of 20% was applied to the voltage source at t = 5s for a duration of 150 ms. Figure 13 shows the complete response of the system during this test. Figure 13(a) illustrates the behavior of the direct axis current, id, which is responsible for controlling active power. Despite the major disturbance in the grid voltage V_g , the i_d current continues to follow its reference setpoint with excellent accuracy. The small spike visible at t = 5 s is immediately corrected by the PI controller, demonstrating its responsiveness. Similarly, Figure 13(b) shows that the quadrature axis current i_q which controls reactive power, is strictly maintained at its zero setpoint. This proves that the control is capable of ensuring unity power factor operation even under degraded conditions.



(a) (b)

Figure 13. Robustness test under a 20% symmetrical grid voltage dip: (a) direct axis current control i_d and (b) quadrature axis current control i_q

5. CONCLUSION

This study presented an advanced battery energy storage system connected to the grid, integrating an interleaved bidirectional buck/boost converter, a three-level NPC inverter, and an optimized LCL filter controlled through SVPWM enhanced techniques. The proposed architecture demonstrates significant improvements over conventional solutions, achieving a THD of 2.93% and a rapid dynamic response during operational mode transitions. The effectiveness of the control strategy in maintaining a stable DC link voltage and regulating the system requires the current validation of the technical approach. At the same time, a comparative analysis confirms the quality of the upper waveform compared to traditional two-level configurations. Based on the successful outcome of this simulation study, future work will look at three main areas of effort to help close the gap between theoretical models and their application in the industry. The priority is to validate designs for the proposed architecture through experimental testing with a laboratory hardware prototype. This step will allow for quantification of parameters that cannot yet be fully characterized by simulation alone, such as switching losses, thermal profiles, and EMI. The second area of investigation will be to develop control algorithms for the proposed architecture on actual digital control hardware (DSP or FPGA) to confirm computational performance and timing requirements. The final area of work will be to improve the resiliency of the system by examining its performance during asymmetrical grid faults and large frequency deviations, as well as assessing the performance using non-linear control techniques such as model predictive control (MPC) for additional optimization of dynamic performance.

Simulation results confirm both the theoretical feasibility and robust operation of the proposed architecture; however, there are limitations that are inherent to simulation-based validation. The first limitation is that the idealized models of the power switches used in this study fail to account for non-linear switching losses, thermal dissipation dynamics, and EMI, which will all affect the hardware implementation. The second limitation is that the battery model used is also non-linear, but it assumes uniform temperatures throughout the battery; therefore, in real-world situations, there are likely thermal runaway risks and cell balancing problems that may affect the efficiency of the overall system. The third limitation is that although the system was shown to be resilient to symmetric voltage dips, its performance during unbalanced grid faults and severe frequency deviations. These factors will be the primary focus of the future experimental prototyping phase mentioned in the conclusion.

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AUTHOR CONTRIBUTIONS STATEMENT

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C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

The authors state no conflict of interest.

DATA AVAILABILITY

The derived data supporting the findings of this study are available from the corresponding author, [OE], on request.

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