International Journal of Power Electronics and Drive System (IJPEDS)
Vol. 17, No. 2, June 2026, pp. 1142~1151
ISSN: 2088-8694, DOI: 10.11591/ijpeds.v17.i2.pp1142-1151

Improved efficiency of DC-DC converter through modified switched inductor-switched capacitor configuration using ANN optimization for photovoltaic sources

Ramalingam Seyezhai, A. S. Athish, K. Ashwathy, R. Akash Karthick
Department of Electrical and Electronics Engineering, Sri Sivasubramaniya Nadar College of Engineering, Chennai, India

Article Info

Article history:

Received Oct 17, 2025
Revised Mar 20, 2026
Accepted Apr 23, 2026

Keywords:

ANN integration
Efficiency
Levenberg-Marquardt algorithm
Ripple reduction
SISC

ABSTRACT

In photovoltaic applications, the DC-DC converters are of utmost importance, allowing for the regulation of output voltages to satisfy system needs. A preliminary analysis of several converter topologies revealed that the switched inductor switched capacitor (SISC) configuration provides better performance with lower ripple, reduced stress, and better voltage boosting. The performance of the proposed topology is compared with different SISC topologies, and it is observed that the chosen configuration is suitable for photovoltaic sources. The efficiency of the suggested topology is further enhanced by using artificial neural networks (ANN) for regulating the switching frequency and duty cycle of the switch. In this work, two ANNs are used to train both switching frequency and duty cycle. For the training process, the Levenberg-Marquardt algorithm is used to achieve fast convergence with precise predictions. A prototype model is constructed and tested to validate the simulation results. The results prove that the projected converter achieves considerable efficiency and is suited for photovoltaic (PV) systems.

Corresponding Author:

Ramalingam Seyezhai
Department of Electrical and Electronics Engineering, Sri Sivasubramaniya Nadar College of Engineering
Kalavakkam, Chennai 603110, India
Email: seyezhair12@gmail.com

1. INTRODUCTION

In photovoltaic (PV) systems, DC-DC converters play a crucial role as it enables efficient and reliable use of solar energy [1]-[3]. These converters have numerous advantages, such as adjusting the variable output voltage from solar panels to a stable, usable level required by batteries, inverters, or the grid, thereby optimizing energy transfer and system performance. Also, DC-DC converters act as an interface between PV modules and the load or the grid, ensuring compatibility and protection against over-voltage, over-current, and short circuits. Since DC-DC converters support a wide range of voltage conversion ratios, a flexible system design and integration with various types of PV arrays and energy storage is permissible [4]-[6]. Hence, for regulating voltage, maximizing energy harvest, and ensuring safe, efficient operation Across diverse environmental and load conditions, DC-DC converters are indispensable in photovoltaic systems. Among different DC-DC converters, the switched inductor-switched capacitor topology is chosen [7]-[9].

Switched inductor- switched capacitor converter (SLSC) is an advanced type of DC-DC power converter that integrates switched-inductor and switched-capacitor topologies to achieve a high voltage conversion ratio, reduced switch voltage stress, and enhanced efficiency [10]. Due to these distinct

advantages, the SLSC is well-suited for PV systems as it requires efficient voltage step-up from low PV module voltages (e.g., 24-48 V) to the high voltages required by inverters or grid interfaces (e.g., 380-400 V). Also, reduced voltage stress and voltage ripple enhance the system reliability and extend the lifespan of both PV panels and converter components [11]-[13]. In this work, a new type of SLSC is proposed where a certain modification is incorporated in the existing topology. The proposed modified single-switch switched inductor–switched capacitor (SISC) topology has an additional inductor, capacitor, and diodes, which reduces the stress across the components even at a high power conversion ratio with minimal passive components. The performance of the proposed modified converter is evaluated and compared with existing SISC topologies such as conventional single-switch SISC, cascaded SISC, multilevel ladder SISC, and hybrid interleaved SISC.

Further, to improve the converter performance, an artificial neural network (ANN) is implemented. ANN optimizes the converter performance under varying conditions, such as changes in solar irradiance or in PV load systems. In this work, a dual ANN is employed to adjust the power MOSFET frequency and duty cycle. This helps in reducing the switch voltage stress, power losses, and component sizing. Thereby, The efficiency of the converter is improved. Thus, the proposed work is well-suited for a photovoltaic system. The organization of the paper is as follows: i) Section 2 deals with the literature review; ii) SISC topologies are discussed in section 3; iii) Section 4 illustrates the analysis of SISC topologies; iv) Section 5 describes ANN optimization; and v) The circuit-level implementation is presented in section 6.

2. LITERATURE REVIEW

DC-DC converters are crucial in photovoltaic (PV) systems as it increases low DC input voltages, typically in the range of 20-48 V, to 200-400 V, which is essential for inverter operation and grid integration [14]. But the converter should be designed with low voltage ripple, reduced component stress, and minimum power losses, in order to ensure efficient converter performance. Recent studies focus on hybrid topologies that combine switched inductor (SI) and switched capacitor (SC) structures. These achieve high voltage gain without the transformers, and the design is simple [15].

2.1. Conventional topologies

The most commonly used converter in photovoltaic (PV) systems is a conventional boost converter which has limited voltage gain at low duty cycles. Also, the conventional boost converter cannot be extended for high-power PV applications as it faces the inductor saturation and significant output voltage ripple. The other existing topologies, such as buck-boost, Cuk, SEPIC, and zeta, have high voltage conversion, but they still it faces the problem of efficiency reductions under varying load conditions. These converters generate discontinuous input current, which affects PV module performance and reduces the overall lifespan of the photovoltaic system.

2.2. SI-SC hybrid advances

To overcome the limitations of conventional DC–DC converters, SISC converter topologies have been developed [16]. The converter has high voltage gain with a smaller number of components and maintains low voltage stress levels, typically in the range of 1.2-2.8. In 2023, a quasi-Z-source SISC converter was developed to step up 48 V to 650 V at a power level of 500 W and a switching frequency of 50 kHz. This design has continuous input current due to a common-ground configuration. The optimized interleaved SISC structures is developed to step up input voltages of 20-40 V to output levels of 200-400 V even at low duty cycles. The design is compact as it uses minimal inductors and capacitors while maintaining efficiencies above 90% in PV applications. To further reduce the current ripple and enhance The system reliability, many hybrid converters that combine switched capacitor and inductor cells have been reported [17].

2.3. ANN optimization role

The performance of SISC converters is improved by adopting artificial neural networks (ANN) [18], [19]. ANN enables adaptive control of duty cycle and switching frequency under varying irradiance and load conditions. Also, the rider optimization algorithm (ROA) combined with ANN is investigated in high-gain boost converters. The studies show that the ROA–ANN controllers have better voltage stabilization in standalone PV systems, and overshoot is reduced significantly when compared with standard ANN and PID control strategies. ANN-based ripple minimization techniques in interleaved converter design have real-time adjustment of operating parameters, enhance overall converter stability and performance under changing operating conditions [20].

2.4. Research gaps

Still, the SISC converters have several limitations, such as:

- At high power levels above 350 W, the component stress becomes significant, and it exhibits output voltage ripple greater than 5 V and efficiencies below 85%.
- The simultaneous control of both switching frequency and duty cycle with ANN remains limited in modified single-switch converter configurations. Also, a real-time testing of the circuit under varying PV conditions is limited.

2.5. Novelty

To overcome the existing limitations, a modified single-switch SISC converter with a dual ANN-based control strategy is introduced, where the neural network is trained using the Levenberg-Marquardt algorithm for improved performance under varying conditions. The proposed system achieves an efficiency of 82-88%, maintains a voltage ripple of around 1.5 V, and provides a voltage gain of up to ten times at 350 W. Overall, the design demonstrates an improvement of approximately 8-10% compared to conventional SISC converters.

3. SISC TOPOLOGIES

3.1. Single-switch SISC topology

The SISC topology is a hybrid of switched inductor and switched capacitor configurations. This has been the most appropriate selection for energy harvesting systems such as solar power, and the circuit diagram of the single switch SISC topology is depicted in Figure 1. The circuit portrayed in Figure 1 suffers from high component stress, and this degrades the system performance and limits it to low power levels. Therefore, to overcome this, a new modified SISC topology is proposed in this work.

3.2. Modified single-switch SISC topology

The proposed modified single-switch SISC topology has an additional inductor (L_3), capacitor (C_4), and diodes (D_6, D_7). This reduces the stress across the components even at a high-power conversion ratio with minimal passive components. Due to this, the charge-pump mechanism is enhanced, and high voltage gain and high efficiency are obtained. Thus, the proposed topology is preferred as it is extended for high-power applications. The circuit diagram of the modified single-switch SISC topology is presented in Figure 2. The modes of operation, design equations, and simulation results of the proposed topology are explained in section 3.2.1.

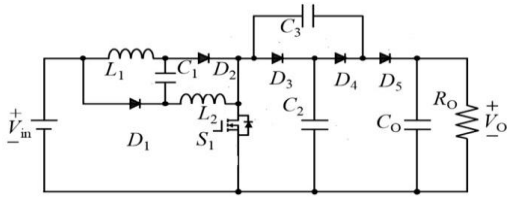

Figure 1. Single switch SISC DC-DC converter topology

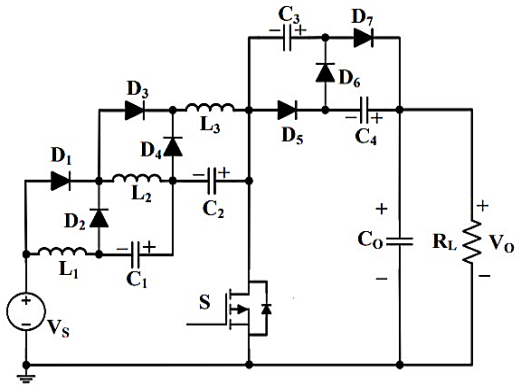

Figure 2. Modified single switch SISC DC-DC converter topology

3.2.1. Modes of operation

The modified topology has two modes of operation as follows:

- Mode-I: Switch (S) ON. The MOSFET switch S turned ON, allowing current to flow through energy-storing inductors L1, L2, and L3. The diodes D1, D3, and D6 are forward-biased. The load receives energy from the output capacitor C0, ensuring continuous power delivery.
- Mode-II: Switch (S) OFF. The inductors' stored energy is released upon opening the switch (S). Diodes (D3, D4, D5) transmit this energy to capacitors (C3, C4), which raise the voltage even more. The load (RL) receives the final boosted voltage from the output capacitor (C0).

3.2.2. Design of modified single-switch SISC topology

The design equations of the modified topology are given in (1)-(7). Output voltage in (1).

$$Vo=\frac{4}{(1-D)^2}\ V_s \tag{1}$$

Inductor shows in (2)-(4).

$$L_1> \frac{2DV_s}{\Delta \mathrm{IL1} \times f_s(1-D)} \tag{2}$$

$$L_2> \frac{DV_s}{\Delta \mathrm{IL2} \times f_s(1-D)} \tag{3}$$

$$L_3> \frac{DV_s}{\Delta \mathrm{IL2} \times f_s} \tag{4}$$

Capacitor shows in (5)-(7).

$$C_1=C_2\geq \frac{V_o\ (1-D)}{\Delta V_{c1} * f_s * R}\ I_o \tag{5}$$

$$C_3=C_4\geq \frac{P_o\ D}{\Delta V_{c3} * f_s * V_o}\ I_o \tag{6}$$

$$C_o\geq \frac{V_o\ D}{\Delta V_o * f_s * V_o}\ I_o \tag{7}$$

Where, f_s = switching frequency, D = duty cycle, I_o = output current, R = load resistor, ΔV_o = output voltage ripple, ΔI_{L2}= inductor current ripple, ΔV_{c1} = capacitor voltage ripple. The specified values of parameters employed in the simulation are listed in Table 1.

Table 1. Simulation parameters of single switch SISC topology

Parameter	Values
Switching frequency f_s	20 kHz
Input voltage V_i	24 V
Output voltage V_o	230 V
Duty cycle D	0.43
Gain	9.58
Rated power P_i	350 W
Capacitor C_1,C_2, C_3,C_4	10 µF
Capacitor C_0	20 µF
Inductor L_1,L_2, L_3	650 µH, 350 µH, 150 µH
Load R	100 Ω

3.2.3. Simulation results

The simulations are carried out in MATLAB/Simulink, and the results are depicted in Figures 3-6. Figure 3 shows the output voltage waveform of the DC-DC converter, which is about 230.9 V. Figure 4 shows the output current waveform of the DC-DC converter, which is about 1.85 A. From Figures 5 and 6, it is observed that the output voltage ripple is 3.5 V and the output current ripple is 0.005 A. The modified topology is compared with the existing conventional SISC topology, and the analysis is illustrated in Table 2.

Thus, the proposed modified single-switch SISC topology achieves high voltage gain, reduced output voltage and output current ripple, reduced switch voltage stress, and high efficiency compared to

conventional single-switch SISC as presented in Table 2. An additional inductor (L_3), a capacitor (C_4), and a diode pair (D_6 and D_7) is incorporated into a single-switch structure to constitute a modified SISC design. This leads to a reduction in voltage stress to about 1.2 against with approximately 3.5 in typical single-switch SISC converters. The proposed model delivers continuous current and attains an output voltage ripple of about 1.5 V. This is 70% lower than the cascaded configurations (around 6 V) and hybrid interleaved structures (around 3 V), as it requires only 15% additional passive components.

Dual ANN controllers are incorporated in the proposed converter, which is trained using the Levenberg–Marquardt algorithm [21] with a mean square error below 1.5. With this, the regulation of both switching frequency (41 kHz) and the duty cycle is carried out simultaneously under varying photovoltaic operating conditions. This is not followed in traditional converters, as it uses an ANN only to control the duty cycle. This dual ANN strategy enhances converter efficiency by 8.5% and attains an efficiency range of 82–88% compared with non-ANN SISC implementations. Also, settling time is reduced by half compared with PID-based control methods. This has been validated using a hardware prototype that generates an output of 94 V from a 10 V input.

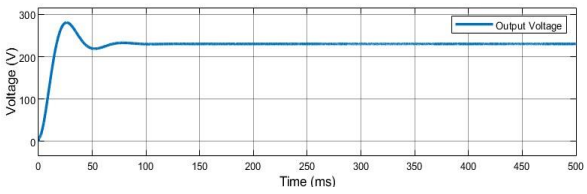

Figure 3. Output voltage of the modified single switch SISC topology

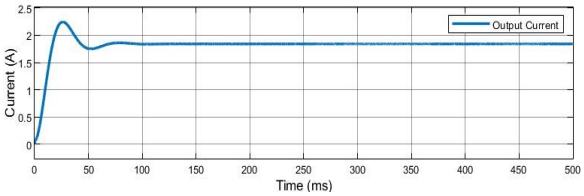

Figure 4. Output current of the modified single switch SISC topology

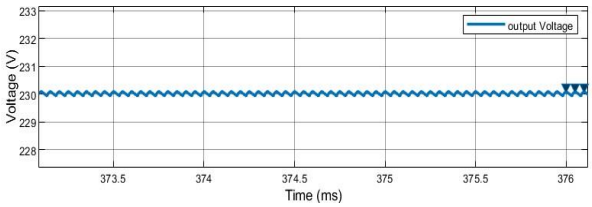

Figure 5. Output voltage ripple of the modified single switch SISC topology

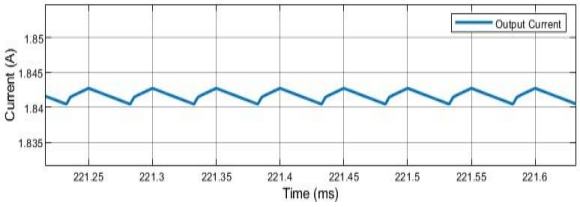

Figure 6. Output current ripple of the modified single switch SISC topology

Table 2. Comparison between single switch and modified single switch SISC topologies

Parameters	Modified single switch	Conventional single switch SISC
Duty cycle	0.43	0.58
Gain	$4/(1-D)^2$	$4/(1-D)$
Voltage ripple (V)	3.5	5
Current ripple (A)	0.005	0.153
Efficiency	82.3%	73.77%
Switching voltage stress	2.875	3.5

4. ANALYSIS OF SISC TOPOLOGIES

The performance of the suggested modified single switch SISC topology is analyzed with different SISC topologies, and the results are presented in Table 3. The parameters accounted for analysis are voltage gain (V_G), switch voltage stress (V_s), output voltage ripple (V_i), output current ripple (I_i), and efficiency (η). As shown in Table 3, the proposed modified single-switch SISC has superior performance compared to other topologies, such as high voltage gain, reduced switch voltage stress, low output voltage and current ripple, and enhanced efficiency. Hence, the proposed modified single-switch SISC is highly recommended for PV applications.

Table 3. Comparative analysis of SISC topologies

Topologies	V_G (%)	V_s (%)	V_i (%)	I_i (%)	ɳ (%)
Cascaded SISC [22]	8	6	5	10	80
Hybrid interleaved SISC [23]	10	2	3	5	90
Multilevel ladder SISC [24]	10	3	2	5	80
Conventional single-switch SISC [25]	5	1.5	2.1	8	73
Modified single-switch SISC	10	1.2	1.5	1	82

5. OPTIMIZATION USING ARTIFICIAL NEURAL NETWORKS

ANN is an artificial vision model that replicates the brain to identify patterns and resolve intricate issues. In this work, ANN is adopted for two purposes: i) To determine the switching frequency and duty cycle to minimize the losses, thereby improving the efficiency of the converter; and ii) To regulate the voltage during load power fluctuations, thereby improving the converter performance.

5.1. ANN for switching frequency and duty cycle

ANN is based on layers of interacting nodes (neurons) that compute through weighted connections. It offers real-time adaptability and guarantees system stability despite fluctuating load. By a disciplined MATLAB-driven methodology, data acquisition, model training, testing, validation, and optimization, ANNs can efficiently search for optimal parameters such as switching frequency (f_s) without tedious time-consuming tuning.

5.1.1. Dataset generation

Voltage ripple (V_s = 0.05) constraint is applied. Through the equations set forth beforehand, each voltage input's switching frequency (f_s) and duty cycle (D) are calculated. MATLAB code generates a dataset consisting of 281 training samples generated for an input voltage range of 10 V to 24 V, and a sample dataset is given in Table 4.

Table 4. Sample of the dataset generated

V_s	10	12	14	16	18	20	22	24
D	0.5830	0.5430	0.5066	0.4725	0.4405	0.4102	0.3814	0.3539
F_s	17216	20780	24157	28269	31050	34562	37985	41318

5.1.2. Training

The neural fitting tool (nftool) is used to train the ANN. In this work, two ANNs are used to train both switch frequency and duty cycle. Datasets are loaded into the model; by doing so, the input voltages are used as predictors, and corresponding duty cycle values and switching frequency are used as responses. For the training process, the Levenberg-Marquardt algorithm is used to achieve fast convergence with precise predictions. In this process, the ANN can develop relationships between input voltage and critical parameters with efficient optimization of circuit performance, and the result is depicted in Figure 7.

Algorithm

Data division: Random
Training algorithm: Levenberg-Marquardt
Performance: Mean squared error

Training Results

Training start time: 06-Mar-2025 10:42:26
Layer size: 10

	Observations	MSE	R
Training	197	0.7632	1.0000
Validation	42	1.1363	1.0000
Test	42	1.4727	1.0000

Figure 7. Neural network training results summary

Figure 7 presents ANN training results using the Levenberg Marquardt algorithm with mean squared error (MSE) as the performance metric. The low MSE values (0.7632 for training, 1.1363 for validation, and 1.4727 for testing) indicate minimal prediction errors. Additionally, the R-values of 1.0000 across all phases confirm the model's high accuracy and strong predictive capability. Both manual and ANN results for an input voltage of 24 V are compared, and the values from manual computation and the model

match precisely. By leveraging ANN, the values of duty cycle (0.43) and switching frequency (41.813 kHz) are efficiently determined. These results will be utilized for hardware implementation. The performance of the proposed converter is further validated with the existing topologies, and the analysis is listed in Table 5. The performance metrics are root mean square (RMSE), Integral square error (ISE), and integral time weighted absolute error (ITAE).

From Table 5, it is obvious that the proposed topology performs better than the conventional topologies. The low values of RMSE, ISE, and ITAE indicate that the errors are quickly detected and rectified. Thus, the proposed model with ANN suits well for PV applications. From Figure 8, it is observed that the proposed model works well under variable load conditions as the voltage regulations fall from 0.6-1.8%.

Table 5. Performance analysis of SISC topologies

Topology	RMSE (%)	ISE	ITAE
Cascaded SISC	3.1	0.65	1.9
Hybrid interleaved SISC	2.8	0.52	1.9
Multilevel ladder SISC	2.5	0.48	0.7
Conventional single-switch SISC	4.2	1.1	2.8
Modified single-switch SISC	2.1	0.45	1.2

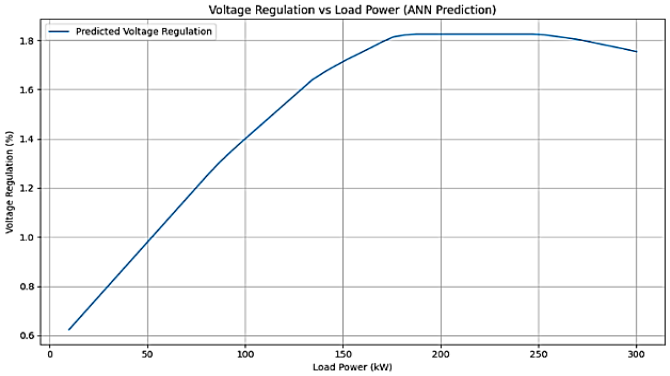

Figure 8. Voltage regulation

6. CIRCUIT – LEVEL IMPLEMENTATION

A prototype model of the proposed converter is built and validated. The hardware setup has a transformer, MOSFET driver, and passive devices. The Arduino UNO board is employed to generate a gate pulse to power the MOSFET. The observed pulse pattern is depicted in Figure 9. The hardware setup is tested with an input voltage of 10 V, and a load resistance of 100 Ω is used to confirm the converter's performance and practical feasibility. The driver circuit, the control circuit, and the power circuit of the proposed modified single-switched switched inductor switched capacitor DC-DC converter are illustrated in Figure 10. The comparison of hardware and simulated values is depicted in Table 3.

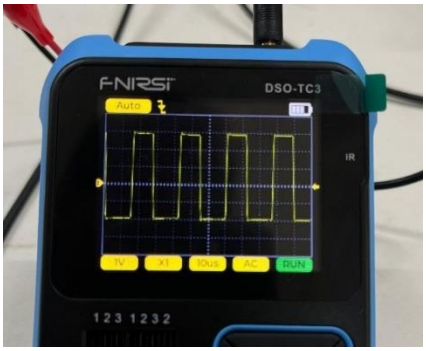

Figure 9. Gate pulse pattern in DSO

Figure 10. Hardware circuit

The observed results are: Output voltage: 94 V indicates steady-state operation in less than 5 ms, voltage ripple: 4.1 V peak-to-peak shows stable output regulation. Switch voltage stress: 2.6 indicates the effective low-stress converter design, efficiency: 82% at 350 W. Thus, the proposed model suits for photovoltaic front-end applications as it works well under varying irradiance and load conditions with the help of real-time ANN-based control. In Table 6, it is observed that the experimental implementation closely matches the simulation values. Overall, the simulation and hardware results are correlated and validate the feasibility and reliability of the proposed converter design for practical photovoltaic power conversion applications.

Table 6. Simulation vs hardware results

Parameters	Simulated results	Hardware results
Input voltage	10 V	10 V
Output voltage	95.6 V	94 V
Output voltage ripple	5.3 V	4.1 V
Stress across the switch	2.14	2.6
Efficiency	88%	82%

7. CONCLUSION

This study presents a modified single-switch SISC DC-DC converter integrated with dual ANN optimization trained using the Levenberg–Marquardt algorithm. The proposed approach simultaneously regulates both the switching frequency and duty cycle, enabling improved dynamic control of the converter. The design achieves a voltage gain of about ten times, maintains voltage stress near 1.2, limits output ripple to approximately 1.5 V, and delivers an efficiency between 82% and 88% when operating with photovoltaic inputs in the range of 10-24 V at a power level of 350 W. Compared with conventional SISC converters, which typically show efficiencies around 73.8% and output ripple close to 5 V, and interleaved configurations that experience voltage stress greater than 2, the proposed configuration provides improved performance. The inclusion of additional components (L_3, C_4, D_6, and D_7), combined with adaptive ANN-based control, reduces output ripple by nearly 70%, decreases voltage stress by about 66%, and increases efficiency by approximately 8.5% under varying load and irradiance conditions. The effectiveness of the design is confirmed through experimental validation using a hardware prototype that produces an output voltage of about 94 V with an observed ripple of roughly 4.1 V. The proposed converter structure provides a compact and scalable solution for photovoltaic front-end power conversion in grid-connected applications.

FUNDING INFORMATION

The authors declare that they have not received funding.

AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
Ramalingam Seyezhai	✓	✓		✓		✓	✓			✓	✓	✓		
A. S. Athish			✓	✓		✓			✓	✓				
K. Ashwathy		✓			✓	✓			✓					
R. Akash Karthick			✓	✓	✓				✓	✓				

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

The authors declare that they have no conflict of interest.

DATA AVAILABILITY

All data analyzed during this study are included in this published article.

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BIOGRAPHIES OF AUTHORS

Dr. Ramalingam Seyezhai is a professor in electrical and electronics engineering with 24 years of teaching and research experience, including 17 years of research experience in power electronics and renewable energy systems. She received her B.E. from Manonmaniam Sundaranar University in 1996, M.E. in power electronics and drives from Bharathidasan University in 1998, and Ph.D. from Anna University, Chennai. She has been actively involved in SSN-Institution's Innovation Council (SSN-IIC), SSN Innovation Centre, NBA, and ARIIA ranking in the institution, and curriculum framing for PG and PG NBA at the department level. She completed the innovation ambassador training conducted by MoE's Innovation Cell and AICTE during 2021. She can be contacted at email: seyezhair12@gmail.com.

A. S. Athish is pursuing a B.E. in electrical and electronics engineering at SSN College with interests in power systems, renewable energy, and embedded systems. He has done projects on high-gain DC-DC converters and resonant converters. He published research papers in IEEE. He is a NCC cadet, inter-college handball champion, and has held leadership roles such as Department Coordinator of Instincts '25. He can be contacted at email: athish22110045@ssn.edu.in.

K. Ashwathy completed B.E. in electrical and electronics engineering at Sri Sivasubramaniya Nadar College of Engineering, Chennai, with a CGPA of 9.00. Her research focuses on power electronics, renewable energy systems, and embedded systems, with projects including high-gain DC-DC converters and resonant converters. She published research papers in IEEE and Research Square and received the SSN Merit Scholarship along with gold medals for academic and has a keen interest in sports and extracurricular activities. She can be contacted at email: aswathy2110630@ssn.edu.in.

R. Akash Karthick completed B.E. Electrical and Electronics Engineering from Sri Sivasubramaniya Nadar College of Engineering with a GPA of 8.373. He is now pursuing a Master of Engineering Management at NC State University. He focuses on operations and supply chain management. He published research papers in IEEE as well as Springer. He can be contacted at email: akhash2110552@ssn.edu.in.