Design and analysis of a C^4S DC–DC converter for sustainable solar energy systems

G. Jegadeeswari[1], M. Vaigundamoorthi[1], R. Sundar[2], J. S. S. L. Bharani[3], C. Rajarajachozhan[4], M. Batumalay[5], S. P. Manikandan[6]
[1]Department of Electrical and Electronics Engineering, Saveetha Engineering College, Chennai, India
[2]Department of Marine Engineering, AMET Deemed to be University, Chennai, India
[3]Department of Electrical and Electronics Engineering, S. R. K. R. Engineering College, Andhra Pradesh, India
[4]Electronics and Communication Engineering, University College of Engineering, Kancheepuram, India
[5]Centre for Data Science and Sustainable Technologies and Faculty of Data Science and Information Technology, INTI International University, Nilai, Malaysia
[6]Department of Electronics and Communication Engineering, Saveetha Engineering College, Chennai, India

Article Info

Article history:

Received Mar 30, 2025
Revised Feb 14, 2026
Accepted Apr 23, 2026

Keywords:

C^4S converter
Coupled capacitor
DC–DC conversion
FLC PV systems sustainable solar energy
High-gain converter
Process innovation

ABSTRACT

Efficient DC-DC power conversion is essential for sustainable solar photovoltaic systems. Conventional converters often suffer from leakage currents, higher circuit complexity, and limited flexibility in interfacing with grid-connected inverters. This study introduced a novel hybrid DC-to-DC converter based on the C^4S (coupled capacitor combined Cuk-SEPIC) converter, proposed precisely for sustainable solar photovoltaic systems. The designed converter offers a dual output in the form of a bipolar direct current (DC) bus, allowing flexible combination with grid-connected inverters that receive either unipolar or bipolar DC inputs. This setup not only enables effective transfer of power to the grid but also efficiently removes the leakage currents without the necessity of lossy DC-link capacitors from the load-side current loop. Moreover, the magnetic cores are integrated by employing the input and output coupled capacitors, which considerably minimize ripple current and ensure the capability of power extraction from the PV unit. A fuzzy logic controller is employed to dynamically adjust the converter's action under varying load conditions and solar irradiance. The proposed topology minimizes driver circuits, reduces system complexity, eliminates leakage current without requiring lossy DC-link capacitors, and improves reliability. Simulation results demonstrate stable voltage regulation, reduced ripple, improved efficiency, and superior dynamic response compared to conventional control methods. The proposed converter demonstrates its potential as a high-performance, intelligent, and energy-efficient process innovation for modern sustainable solar energy systems.

Corresponding Author:

G. Jegadeeswari
Department of Electrical and Electronics Engineering, Saveetha Engineering College
Chennai, India
Email: jegadeeswari.dharan@gmail.com

1. INTRODUCTION

Utilization of renewable energy systems in today's world gives a rapid transition, and it has significantly improved the demand for intelligent power conversion and higher efficiency between the grid and the sources of distributed energy. Due to its flexibility, less pollution, and free resources, solar PV systems play a vital role in generating sustainable power [1], [2]. Though generating power from solar is only possible with the help of a proper converter setup, which gives an efficient DC-DC conversion [3].

Nowadays, many converter topologies are available, like boost, Cuk, zeta, and SEPIC, those provides high switching losses, more input current ripple, and limited voltage gain at wider input variations [4]-[6]. To avoid such limitations, many hybrid converters are introduced, like coupled inductors, combined capacitors, especially to improve voltage gain and minimize stress in the switch [7], [8]. However, to achieve these configurations, a complex control strategy, multiple driver circuits, and larger magnetic which affect the system's reliability and compactness [9].

In high-gain solar applications, hybrid converters in terms of coupled inductors have been popular recently and shown encouraging outcomes, particularly when it comes with a dual output model [10]. Additionally, these converters offer a bipolar direct current (DC) bus voltage and linkage of both unipolar and bipolar inverter topologies by effectively minimizing the problem associated with current leakage [11], [12]. Furthermore, the core losses, emissions, and current ripple are significantly reduced in terms of integrating the magnetic model that incorporates the input and output of the inductor into a single core of magnet [13].

In the present study, a unique converter called C^4S is proposed for a sustainable photovoltaic system. These converters have been developed to produce a dual output bipolar DC voltage, which enables the flexible combination of various types of inverters which minimize the necessity of lossy DC link capacitors in the loop of load current. By implementing a lesser driver circuit and integrating inductor which are magnetically coupled, ripple can be reduced, power can be minimized, and system complexity can be reduced.

A fuzzy logic control (FLC) is used to enhance the performance of the converter by providing reliable and dynamic operation even under varying load conditions. Although soft computing-based controllers provide better voltage stability, efficiency, and transient response than traditional proportional integral (PI) controllers [14], [15]. The performance of the designed converter and controlled schemes is validated with the simulation results, which reveal high performance, energy-efficient conversion, and are best suited for next-generation solar power systems.

In this contest, designing, developing, and analyzing novel hybrid C^4S converter topologies specially for a sustainable solar power energy system is the main goal of this proposed study. This study aims to accomplish dual output mode, higher efficiency, neglect system complexity, and reduced current leakage in the grid inverter tied system.

Despite extensive research on DC–DC converters for solar photovoltaic (PV) systems, several critical limitations remain unresolved:

- Existing Cuk–SEPIC and hybrid DC–DC converters cannot produce a balanced bipolar DC output in a single stage without additional converters or transformers.
- Most PV-based converters require bulky and lossy DC-link capacitors to suppress leakage currents, reducing efficiency and lifetime.
- Traditional hybrid converters struggle to achieve high voltage gain at moderate duty ratios, leading to high switch stress and degraded performance.
- Current converter designs exhibit high ripple currents, negatively affecting MPPT efficiency and PV energy harvesting.
- Few studies investigate coupled-inductor–based integration in both input and output stages to simultaneously minimize ripple and improve gain.
- Previous works do not provide dual-output (±DC) capability suitable for modern bipolar or unipolar inverters used in grid-interfaced PV systems.
- Most existing converters require multiple driver circuits, increasing complexity, cost, and control burden.
- Limited research exists on applying intelligent controllers (like FLC) optimized for fast dynamics under fluctuating PV conditions in hybrid converters.

The following are the novelty and contributions of this study:

- Introduction of a new C^4S hybrid topology that combines Cuk and SEPIC converters through a coupled capacitor, enabling dual energy-transfer paths.
- First implementation of bipolar ±DC output generation in a single-stage Cuk–SEPIC-based converter without additional circuitry.
- Usage of coupled inductors + coupled capacitors to simultaneously achieve: low ripple, higher gain, reduced magnetic volume, and improved PV current quality.
- Novel decoupling strategy that eliminates DC-link leakage currents without the need for bulky electrolytic capacitors.
- Significant reduction in driver circuits and control hardware, making the converter simpler and more reliable. Integration of an intelligent fuzzy logic controller directly tuned for non-linear PV conditions and dual-output regulation.
- Demonstration of a fully symmetrical bipolar DC bus, enabling compatibility with both unipolar and bipolar grid inverters.

2. METHODOLOGY

The schematic approach of a PV-based bipolar inverter-fed brushless direct current (BLDC) motor with a coupled capacitor, combined with a Cuk-SEPIC converter controlled by a fuzzy logic controller, is illustrated in Figure 1. Using the photovoltaic effect, the DC electrical energy is generated from direct sunlight by means of a solar panel. The generated DC voltage is sent into the combined Cuk-SEPIC converter to get a stable voltage, because it varies with solar irradiation and temperature. This combined converter gives a bipolar DC bus voltage with two outputs, which may be used to drive the DC motor with the help of a bipolar inverter. The purpose of the coupled capacitor in the proposed converter is to enhance the overall efficiency, diminish the input current ripple, and to reduce the switching losses.

The fuzzy logic controller is used to regulate the converter switch duty cycle specially to maintain a steady output voltage under fluctuating load conditions. The FLC enhances the voltage stability, conversion efficiency, and transient response over traditional controllers without the necessity of an accurate mathematical model. In order to ensure a stable DC supply, the coupling capacitor regulates the voltage and reduces the ripple, and acts as a buffer between the inverter and the converter.

The bipolar inverter receives a stable DC power from the coupling capacitors and transforms it into an AC power to operate the BLDC motor. By employing the bipolar switching mode, the inverter reduces the ripple and leakage current and ensures the efficient generation of torque. Subsequently, the BLDC motor transforms the electrical power into mechanical rotation, giving more reliable, higher efficiency, and smooth control of operation even under fluctuating load conditions. So, the integration of this proposed converter along with solar systems and motor drive gives intelligent control, improved power quality, enhanced utilization of energy, and makes it more suitable for photovoltaic applications.

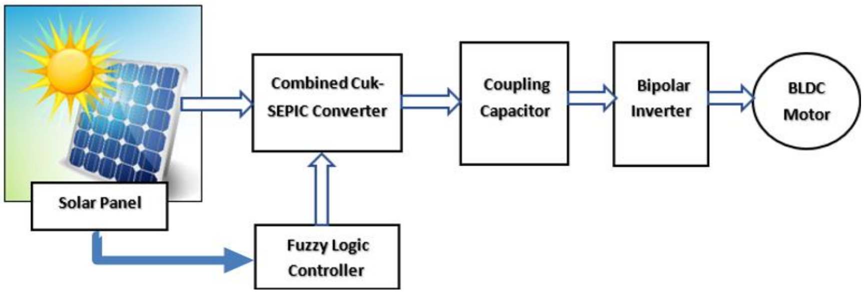


Figure 1. Schematic diagram of solar-powered BLDC motor drive using C^4S converter

2.1. Analysis of proposed converter

2.1.1. Combined Cuk-SEPIC converter

Recently, researchers have been focused on a hybrid C2S-based DC-DC converter, that are ideal for solar power applications and is illustrated in Figure 2(a). It offers both positive and negative outputs by using a single mode of switching through matched grounded reference, which is more common to both SEPIC and Cuk. All the inductors may get charged and discharged from capacitors when the switch is in the ON state, shown in Figure 2(b). During the switch is in the OFF state, as shown in Figure 2(c), the currents from the inductor get redirected from two diodes, and the inductors get discharged while the capacitors get charged. During CCM operation, the switch gets turned on before every complete discharge of the inductor.

This converter may be used for both step-up and step-down voltage conversion applications. The converter has an input/output voltage ratio of D/(1-D) for both positive and negative DC output terminals, resulting in better renovation of duty ratio which are greater than 1/2, and gives a step down from the duty ratio less than 1/2. When the output voltage has both positive and negative voltages, then the converter has an overall gain of 2D/(1-D). The variation of larger input voltage may be regulated with the same duty ratio, or in some cases, the same input voltage can handle the same duty ratio, which allows for a small rating of inductor to be used.

2.1.2. Coupling capacitor with C^2S converter

The advantages of capacitor coupling with C^2S converter are already discussed in the previous section. Though limited research has investigated the real impact of this coupling in both the input and output of the PV applications. As shown in Figure 3, this study inspects the outcome of capacitor coupling between L_S, L_{IN}, and L_C. To find the optimal coupling level, the topology presented in the study, termed as C^4S (coupled capacitor combined CUK-SEPIC converter), is subjected to multi-variable optimization. The outcomes reveal that the coupling capacitor has notable advantages, such as current ripple reduction, allowing for smaller weight, volume, and inductance.

The main function of decoupling the capacitor in the proposed converter is to stabilize the bipolar input and ensure the power transfer to the inverter in a smooth way. They retain the symmetry about the balanced voltage and common ground between both positive (V_{POS}) and negative (V_{NEG}) rails, which are necessary for the smooth operation of the inverter. Furthermore, the coupling capacitors act as a filter, reduce switching stress, and smooth the voltage ripple present on the inverter side. Unlike the steady state and transient period, these capacitors act as a storage element or release energy, especially to maintain a constant DC voltage, thereby improving the stability of the systems and their dynamic response.

Furthermore, the usage of decoupling capacitors in the proposed converter is to diminish the leakage current and common-mode issues, which are more common in PV systems connected through an inverter. In addition to it, it improves the safety, reduces the electromagnetic interference, and enhances the stability of the systems. On the other hand, this decoupling capacitor acts as an interface between the inverter and converter, stabilizing the output and guaranteeing its continuous power flow, and a ripple-free system. The usage of this proposed C^4S converter gives a significant rise in enhanced power quality, efficiency, and controlled stability, these advantages making it a vital element in modern solar power systems.

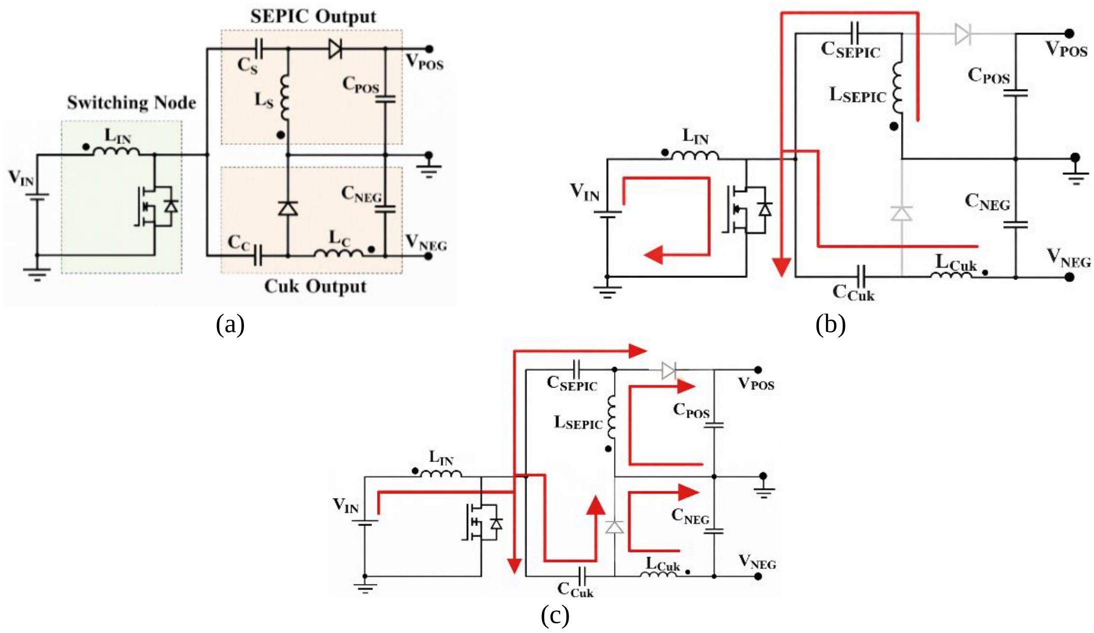


Figure 2. Proposed C^2S converter topology and its operating modes: (a) C^2S converter topology, (b) C^2S operation during ON condition, and (c) C^2S operation during OFF condition

2.1.3. Modelling fuzzy

In this study, the converter voltage is controlled by FLC to contest the reference setpoint. In contrast with other control, fuzzy theory permits each element to have a limited membership value that may be between 0 and 1, which allows human-like sensing, such as low, medium, and high. This controller offers better advantages over other controllers by removing the necessity of mathematical modelling of the system. In order to change the control signal, as per the error caused by the input and its rate of change, this controller may have four stages of operation, such as fuzzification, rule base, decision making, and defuzzification. Figure 4 illustrates the overall systematic diagram of FLC, showing how the four stages of operation are processed in the control systems.

- Fuzzification
  The methods of converting a crisp input into a fuzzy form, which is shown as a fuzzy set in each membership value is known as fuzzification. This process is depicted in Figures 5(a) and 5(b).
- Rule-based
  The rule base is formulated by IF-THEN statements, and the rule base used in this study is given in Table 1. This rule base is determined only after the process of fuzzification, and a set of fuzzy rules is formulated on the set of rules framed based on the conditions applied. The precision and accuracy of the model are purely based on the rule base, and it makes the decision based on the design of the rule base.

– Defuzzification
  The process of transforming the fuzzy value done through fuzzification is then again changed into a firm value, which is called defuzzification. This value will send it into the plant or systems for further processing, and this may be in the form of a weighted average. This method reduces each value of the membership function above that value of the fuzzy output. Average weights are used to collect the singleton values, which are used in the fuzzification process. These fuzzy sets can be used as the symmetric output of the membership functions.

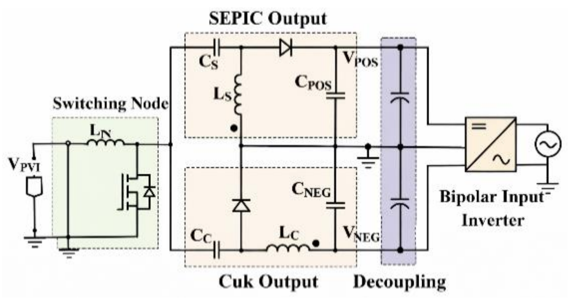


Figure 3. Coupling a capacitor with the C2S converter, fed to the bipolar input inverter

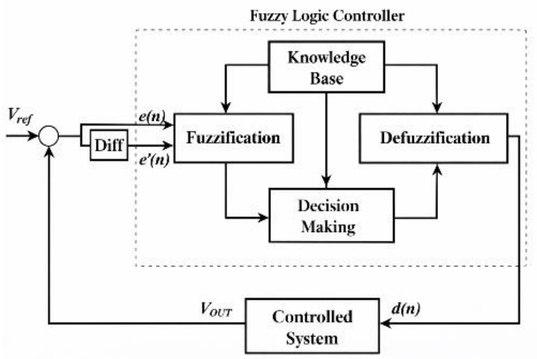
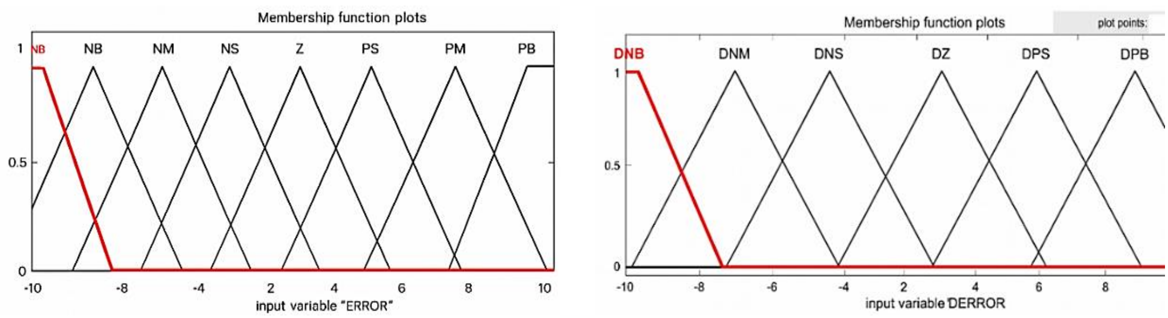


Figure 4. Basic structure of the fuzzy system



(a) (b)

Figure 5. Membership functions of input variables used in the fuzzy system: (a) input variable error and (b) input variable delta error

Table 1. Rule base

E / ΔE	NB	NM	NS	Z	PS	PM	PB
NB	NB	PS	NM	NM	NS	Z	Z
NM	NB	NM	NM	NS	Z	Z	PS
NS	Z	NM	NS	NB	Z	Z	PS
Z	NM	NS	NS	Z	Z	PS	PS
PS	NS	NM	Z	Z	PM	PS	PS
PM	Z	Z	Z	PS	PS	PM	PM
PB	Z	PS	PS	PB	PS	PM	PS

3. STEADY STATE PERFORMANCE ANALYSIS

The voltage conversion, current continuity, and distribution of device stress of the proposed converter are well explained by the steady state performance study. Let us consider, under CCM, that the converter is operated with constant inductor current and stable capacitor voltage over a period of switching. The steady state relations over input and output voltage, duty cycle, and coefficient of coupling can be derived by applying charge and the volt-second balance on capacitors as well as inductors.

3.1. Voltage balance equation

To maintain bipolar bus DC voltage symmetry:

$$V_{POS} + V_{NEG} = 0 \quad (1)$$

$$V_{dc} = V_{POS} - V_{NEG} = 2V_{POS} \quad (2)$$

This voltage balance of both positive and negative outputs, ensures same-magnitude, which is important for delivering symmetric loads or bipolar inverters. This type of symmetry ensures the power quality issues, and reduced common-mode noise in the overall system of operation [16].

3.2. Ripple voltage of decoupling capacitors

The ripple voltage on each capacitor, which are decoupled can be estimated as (3).

$$\Delta Vc = \frac{I_{dc}.D}{f_s.C_{dc}} \quad (3)$$

Where: I_{dc} is the current in the DC link; D is the converter switch duty ratio; f_s is the switching frequency; C_{dc} is the value of capacitance for the decoupling capacitor. Naturally, Δ_{VC} is always kept under the nominal voltage of 2–5% to confirm the stability of the systems and the low-order harmonic distortion [17], [18].

3.3. Energy stored in each decoupling capacitor

The (4) gives the energy stored in decoupling capacitors, which supports the stabilized input of the inverter and the transient variation of the load [19].

$$E_c = \frac{1}{2} C_{dc} V_c^{\,2} \quad (4)$$

3.4. Voltage gain analysis

The voltage gain of the proposed converter is expressed in (8). During the ON interval, the voltage on the primary is shown as (5).

$$V_{L,\ ON} = V_{in} - D\,V_O \quad (5)$$

During the OFF interval, as in (6).

$$V_{L,\ OFF} = V_{in} - n\,V_0 - V_O = V_{in} - (n+1)\,V_0 \quad (6)$$

Volt-second balance, as calculated in (7).

$$D\,(V_{in} - DV_0) + (1-D)(V_{in} - (n+1)V_0) = 0$$
$$V_0 = \frac{V_{in}(1+D+n)}{1-D} \quad (7)$$

So,

$$G = \frac{V_0}{V_{in}} = \frac{1+D+n}{1-D} \quad (8)$$

The gain G gives the converter attains a significantly greater conversion of voltage ratio when compared to normal SEPIC and boost topologies, due to the combined action of the duty ratio (D), coupled inductor turns ratio (n), and coupling capacitor [20], [21].

3.5. Switch stress

The full bus voltage of the switch must become (9),

$$V_{BUS} = V_{in} \frac{1+D+n}{1-D} \quad (9)$$

and regularized switch stress relative to V_0 is as (10).

$$\frac{V_{SW}}{V_0} = \frac{1}{1+D+n} \quad (10)$$

The (10) delivers that the proposed converter exhibits lower voltage of switch stress than normal boost-type converters, allowing the usage of low-level-voltage devices with the reduction of switching and conduction losses. The reduced voltage stress on the switch enhances the reliability and converter efficiency [22].

3.6. Comparison of converter performance

In this study, the designed converter is compared with another converter that employs coupling capacitors and has been proposed in previous studies. The comparison focuses on the parameters of both converters. The detailed parameter comparison is presented in Table 2.

Table 2. Parameter's comparison of converter

Converter	Voltage gain (Vo/Vin)	Switch stress (Vvs/Vo)	Input and output current steadiness
Boost, [23]	$\frac{1}{1-D}$	1	Continuous input
Buck/boost [24]	$\frac{1+D(n+1)}{1-D}$	$\frac{1}{1+D(n+1)}$	Continuous output
CCS [25]	$\frac{1+n}{1-D}$	$\frac{1}{1+n}$	Continuous input
Proposed converter C^4S	$\frac{1+D+n}{1-D}$	$\frac{1}{1+D+n}$	Continuous input and output

4. RESULTS AND DISCUSSION

In this section, the performance of the proposed C^4S (coupled capacitor combined Cuk-SEPIC) converter fed with BLDC motor was assessed through MATLAB/Simulink simulations under various load conditions and solar irradiance to authorize its efficacy, voltage regulation, and dynamic performance of the motor. The PV voltage response found from the simulation study is depicted in Figure 6. The voltage remains constant at around 87.3 V during the entire time period from 0 to 20 seconds. This response shows that it has a steady state voltage without having any fluctuations or ripple in the PV module output. The transient free response shows that the PV systems provide stable operation, implying during various temperature conditions and irradiance.

The output voltage waveform of the Cuk-SEPIC converter is depicted in Figure 7. The graph shows the dynamic response of the converter during initial starts and gives steady state operation. Initially, at t = 0 sec, the voltage starts from lower values and gradually increases as time increases. During 0 to 5 secs of time, the voltage increases sharply, indicating that the charging phase of the output capacitor and the build-up of energy in the converter itself. After 6 secs, the converter output voltage is settled around 220 V, which gives a steady state response with reduced ripple.

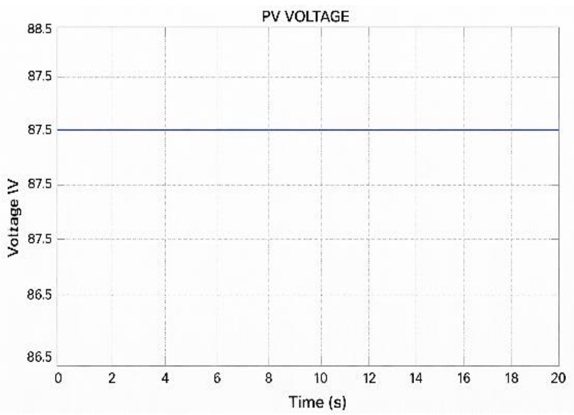


Figure 6. PV voltage response

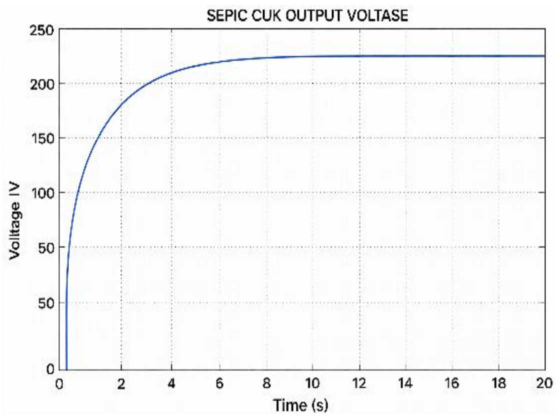


Figure 7. SEPIC-Cuk converter output voltage response

A high-frequency square wave pulse generation is shown in Figure 8. This gives the pulse to the switch given in the proposed converter. The response gives the steady state operation, and uniform spacing between the pulses represents the switching actions of the semiconductor devices in the converter. The duty ratio defined the turn-on time of each cycle, representing the transfer of energy from the converter. This pulse pattern gives a stable performance, and the conduction mode will be continuous.

The speed response of the BLDC motor over time is depicted in Figure 9. Initially, the motor accelerates at high current, which overcomes the inertia of the rotor, resulting in a steep rise in response. During the time 8 to 10 secs, the speed stabilized at around 1500 rpm, showing rated speed with good regulation in speed. The speed is well settled and stabilized without overshoot and oscillations. Finally, the speed settled in a quiet manner and gave an efficient performance with a steady state response.

Figure 10 illustrates the response of electromagnetic torque for the BLDC motor over time. From the graph, it is observed that the torque remains constant around the time period of 6.617 secs. The blue line indicates that the motor operates at steady state operation with 0.3 NM of torque, which is quite good. Due to this response, there is no oscillation, and a transient period occurs in the motor, resulting in good performance of the motor.

The two important electrical characteristics of a motor, such as stator current and EMF curve is shown in Figure 11. The upper graph shows that the stator current gives a small ripple and a maximum peak of about ±0.5 A. The lower graph gives the EMF of the motor, which is termed a trapezoidal waveform. During +100 to _100 V, the voltage varies, representing an EMF induced in the coil through magnetic poles.

The converter proposed in this study has the following merits: lesser switch stress, greater voltage gain, and output and input current in continuous mode is shown in Table 3. At D = 0.6, the proposed converter attains the maximum voltage gain of 6.2 compared to other converters. It also provides the lowest switch stress of 0.385, which diminishes the voltage stress of the switch, improving the robustness and efficiency of the proposed converter.

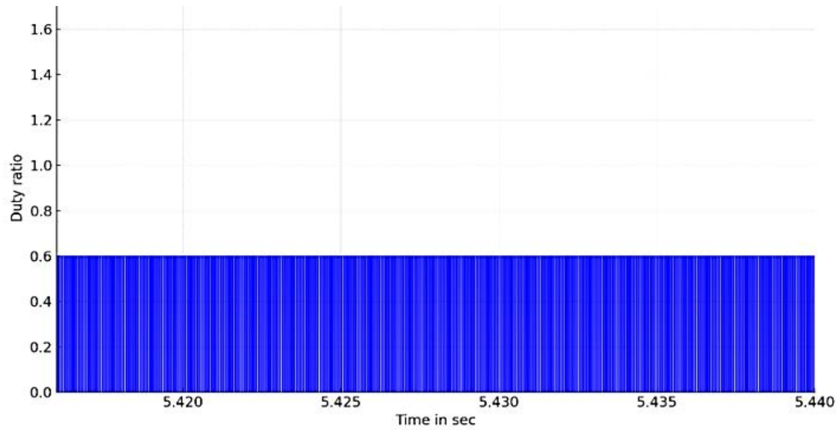


Figure 8. Duty cycle waveform of the converter

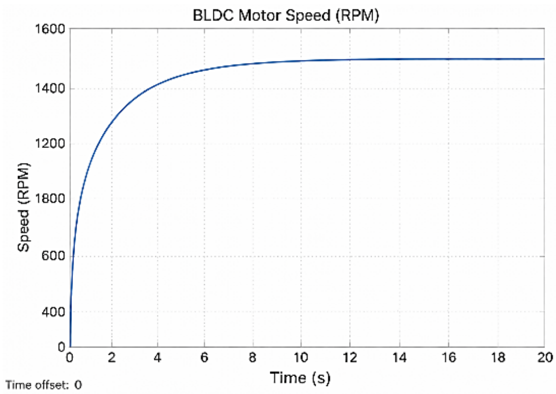


Figure 9. BLDC motor speed response

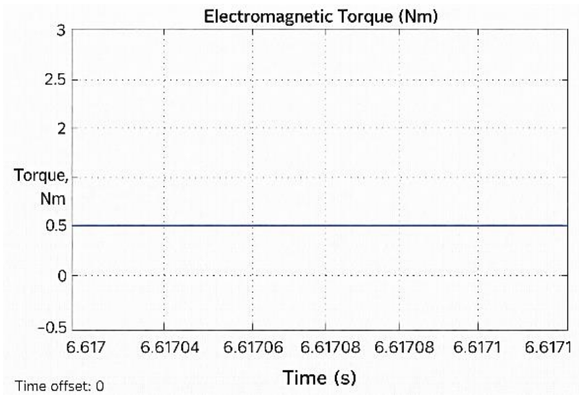


Figure 10. Torque response of BLDC

Table 3. Comparison of the proposed converter with existing

Converter	Duty cycles 0.3	0.5	0.6	Switch tube stress (Vvs/Vo)
	Voltage gain			
Boost, [23]	1.4	2	2.5	1.0
Buck/boost [24]	0.45	1	1.5	0.455
CCS [25]	1.9	3	4	0.5
Proposed converter C^4S	2.4	4	6.2	0.385

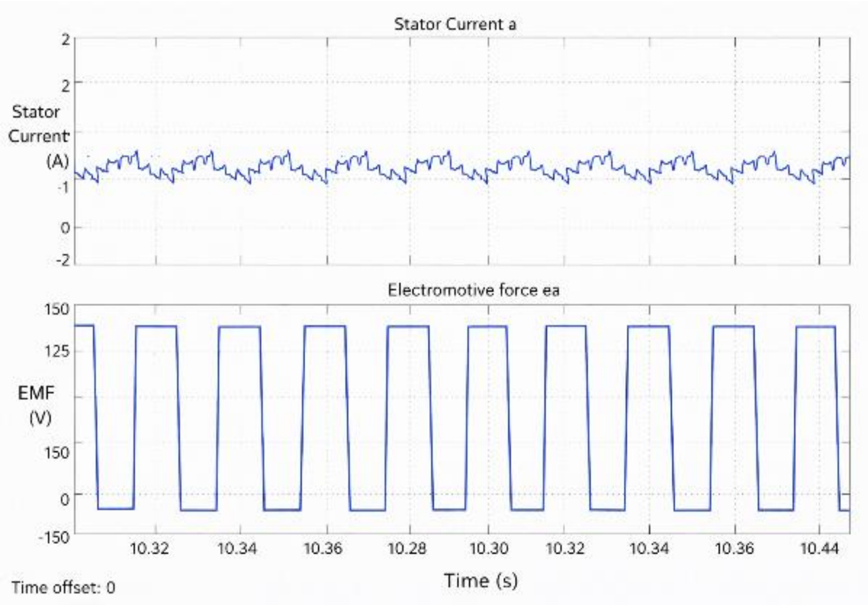


Figure 11. Stator current and electromotive force of BLDC motor

The voltage-gain comparison at different duty cycles (D = 0.3, 0.5, and 0.6) demonstrates a clear performance among the four converters. At D = 0.3, the boost converter attains a gain of 1.4, the buck/boost converter offers only 0.45, while the CCS reaches 1.9. The proposed CI-C^2S converter achieves the greatest gain of 2.4, showing excellent boost abilities even at low duty ratios. As the duty cycle reaches 0.5, boost reaches 2.0, buck/boost reaches 1.0, CCS reaches 3.0, and the proposed CI-C^2S achieves 4.0, showing a clear advantage over the other topologies. At the greatest duty cycle (D = 0.6), boost reaches 2.5, buck/boost reaches 1.5, CCS reaches 4.0, and the proposed CI-C^2S delivers a significantly larger gain of 6.2, which is 2.48 times higher than that of the boost converter and 55% higher than CCS.

In terms of voltage switch stress, the boost converter achieves a maximum of 1.0, while buck/boost and CCS reduce it to 0.455 and 0.5, respectively. The proposed CI-C^2S offers the lowest stress at 0.385, which suggests a substantially lower voltage stress on the switch. This reduced stress, coupled with its improved voltage gain, shows that the proposed C^4S converter gives higher efficiency and reliability over existing topologies. Figure 12 compares the voltage gain of the proposed C^4S converter against the existing topologies over a duty-cycle range of 0.3–0.6. Figure 13 compares the efficiency with the existing one.

The efficiency comparison across different power levels is shown in Table 4. This table demonstrates that the proposed CI-C^2S and CCS converters consistently outperform the conventional topologies. At 500 W, efficiency attains for boost (86.2%) and buck/boost (85%), while CCS (90.2%) and CI-C^2S reach (90.4%). As power increases to 1000 W, efficiencies improve slightly, with boost (87.6%), buck/boost (86.4%), CCS (91.6%), and CI-C^2S (91.6%). At 1500 W, the values increase to 87.7%, 86.5%, 91.7%, and 91.8%, respectively. Finally, at 2000 W, CI-C^2S offers the greatest efficiency of 92.4%, compared to CCS (92%), boost (88%), and buck/boost (86.8%), confirming the superiority of the proposed converter across all load levels.

Table 5 lists that the proposed FLC achieves a maximum output power of 248 W with a tracking time of 5.0 s, which is faster than P&O (8.2 s) and PID (5.9 s). The steady-state ripple is reduced to 0.9%, compared to 3.4% and 1.8% for P&O and PID, respectively. The overall tracking efficiency of the FLC is approximately 97.9%, demonstrating improved dynamic response and stability over conventional controllers.

Table 4. Efficiency comparison of proposed converter with existing

Power (W)	Efficiency %			
	Boost [23]	Buck/boost [24]	CCS [25]	C^4S
500	86.2	85.0	90.2	90.4
1000	87.6	86.4	91.6	91.6
1500	87.7	86.5	91.7	91.8
2000	88.0	86.8	92.0	92.4

Table 5. Performance analysis of FLC-based MPPT versus conventional methods

MPPT method	Maximum power (W)	Tracking time (s)	Steady-state ripple (%)	Tracking efficiency (%)
P&O	240	8.2	3.4	95.5
PID	245	5.9	1.8	97.1
Proposed FLC	248	5.0	0.9	97.9

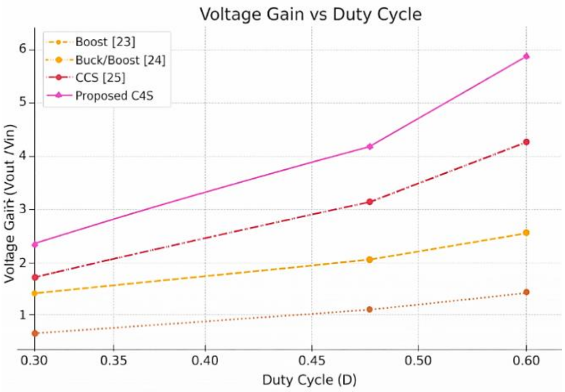


Figure 12. Comparison of voltage gain

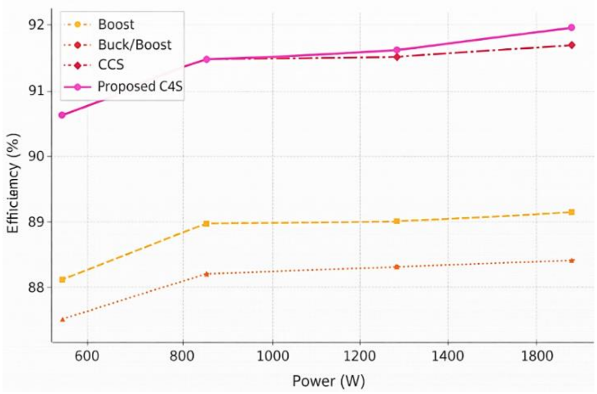


Figure 13. Comparison of efficiency

5. CONCLUSION

The performance evaluation of the proposed C^4S (coupled capacitor combined Cuk-SEPIC) converter integrated with a solar-fed BLDC motor drive confirms its superiority over conventional DC–DC converter topologies in terms of voltage gain, switch stress reduction, and efficiency. The PV subsystem demonstrates excellent stability, maintaining a constant terminal voltage of 87.3 V, with no observable ripple or transient disturbance, indicating strong robustness against irradiance variations. The proposed converter output voltage also exhibits a fast-dynamic response, rising sharply during the initial 0–5 s interval before settling smoothly at approximately 220 V after 6 s, confirming effective energy buildup and minimal steady-state ripple.

The switching pulse waveform generated for the converter shows uniform spacing with a duty ratio of D = 0.6, validating continuous conduction mode and stable switching behavior. Correspondingly, the BLDC motor exhibits smooth acceleration and reaches its rated speed of 1500 rpm without overshoot or oscillation, demonstrating excellent speed regulation. The electromagnetic torque maintains a steady value of 0.3 Nm at around 6.617 s, confirming the absence of torque ripples and ensuring stable motor operation.

The proposed topology achieves the highest voltage gain among all converters at every duty cycle. At D = 0.6, C4S attains a gain of 6.2, outperforming the CCS (4.0), boost (2.5), and buck/boost (1.5). Even at lower duty cycles (D = 0.3 and 0.5), the C4S converter maintains superior gains of 2.4 and 4.0, respectively. Additionally, the proposed converter displays the lowest switch stress of 0.385, compared to boost (1), buck/boost (0.455), and CCS (0.5). This significant reduction in semiconductor voltage stress improves reliability, reduces switching loss, and enhances overall thermal performance.

Efficiency analysis across a wide power range (500–2000 W) further validates the converter's advantage. At 500 W, C4S achieves 90.4% efficiency, surpassing boost (86.2%) and buck/boost (85.0%). At higher power levels, C4S consistently maintains superior performance, recording 91.6% at 1000 W, 91.8% at 1500 W, and the highest efficiency of 92.4% at 2000 W. These results confirm that the proposed converter provides improved power conversion efficiency across all load conditions. Finally, the C4S converter offers substantial advantages, including higher voltage gain, lower switch stress, improved efficiency, and enhanced power quality, making it a robust for PV-powered BLDC motor drives. Its continuous input/output current, reduced ripple, and reliable dynamic performance make it well-suited for renewable energy and inverter-based applications.

ACKNOWLEDGMENTS

The authors would like to express their sincere gratitude to the faculty members for their continuous guidance and encouragement throughout this research work.

FUNDING INFORMATION

This research received no specific grant from any funding agency in the public, commercial, or not-for-profit sectors.

AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
G. Jegadeeswari	✓	✓	✓	✓	✓	✓		✓	✓	✓			✓	
M. Vaigundamoorthi		✓				✓		✓	✓		✓	✓		
R. Sundar	✓		✓	✓		✓	✓			✓	✓		✓	
J. S. S. L. Bharani	✓		✓		✓	✓		✓		✓			✓	
C. Rajarajachozhan	✓		✓	✓	✓		✓			✓	✓		✓	
M. Batumalay	✓	✓		✓	✓			✓	✓				✓	
S. P. Manikandan	✓		✓	✓	✓			✓		✓			✓	

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

The authors declare that they have no conflict of interest.

DATA AVAILABILITY

No new data were generated or analyzed in this study.

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BIOGRAPHIES OF AUTHORS

Dr. G. Jegadeeswari is an assistant professor in the Electrical and Electronics Engineering Department, Saveetha Engineering College (Autonomous), Chennai since 2024; She received the B.Tech. degree in Electrical and Electronics Engineering and the M.Tech. degree in power electronics and drives, both from Pondicherry University, in 2007 and 2012, respectively; and Ph.D. degree in Faculty of Electrical and Electronics Engineering from AMET University, Chennai, in 2024. With over 13 years of teaching experience and 6 years of research expertise, she has published more than 100 research articles, with 30 indexed in Scopus. She is a member of professional organizations such as IEEE and ISOR and holds 3 national and international patents. Additionally, she has authored 3 textbooks, 1 Editor Book, and contributed 8 book chapters to renowned publishers such as IGI Global, CRC Press, Bentham Science, and Wiley. She has organized over 70 workshops, faculty development programs (FDP), seminars, and conferences at both department and university levels. She has submitted research proposals to prestigious bodies like TNSCST, AICTE, DST, NCW, and SERB and secured an ATAL FDP grant of ₹2,70,000. Her contributions to academia have earned her several accolades, including best teacher and best paper awards from various institutions. She is also a reviewer and editorial board member for several international journals. Her research interests encompass power electronics and drives, special machines, and renewable energy. She can be contacted at email: jegadeeswari.dharan@gmail.com.

Dr. M. Vaigundamoorthi working as faculty in the Department of Electrical and Electronics Engineering, Saveetha Engineering college Chennai 602105- India. He received his B.E. Electrical and Electronics Engineering degree from Madurai Kamaraj University during the year 2002. He received his Master of Engineering degree (power electronics and drives) and Ph.D. degree in the area of power electronics DC-DC converter for solar PV from College of Engineering Guindy (CEG) Anna University, Chennai, India in 2007 and 2013, respectively. He has 22 years of Teaching experience and has published 15 research articles in reputed international journals and 6 patents. His area of interest includes power electronics for renewable energy systems, controller design, and nonlinear dynamics analysis in solar PV systems. He can be contacted at email: vaigundamoorthim@saveetha.ac.in.

Dr. R. Sundar is currently working as an associate professor in Marine Engineering at AMET Deemed to be University. He received his Doctor of Philosophy (Ph.D.) in Engineering and Technology, specializing in Renewable Energy, from AMET University. He received a Master's degree in Power Electronics and Drives from SPIHER Electronics from the Madras Institute of Technology (MIT) Campus, Anna University. He received his Bachelor of Engineering degree in electrical and electronics engineering from the University of Madras. He has 22 years of teaching experience, with areas of specialization including marine automation and control systems, marine electrical technology, electrical machines, renewable energy systems, IoT, and power electronics. He has published more than 25 papers in reputed journals, including Scopus, SCI-indexed journals, and Elsevier publications. He has presented 35 papers at various international conferences. He is also the author of the textbook on the design of electrical machines, control systems, and electric and hybrid vehicles. He has been a lifetime member of the Institute of Research Engineers and Doctors (IRED) and the International Association of Engineers (IAENG). He has been a member of the Academic Council, IQAC Core team, NDLI Club President, Marine Technology Society (MTS) Student Chapter Coordinator, and served on several committees, including the Library Committee. He can be contacted at email: mrsundarkrishna@gmail.com.

J. S. S. L. Bharani received the B.E. (electrical and electronics engineering) in 2008. Later, she did her M.Tech. (power systems and automation) in 2021. Presently, she is working as an assistant professor in the Department of Electrical and Electronics Engineering at S. R. K. R. Engineering College, Bhimavaram, Andhra Pradesh, India. Her research area is photovoltaic systems using machine learning and deep learning techniques. She can be contacted at email: jsslbharani@srkrec.ac.in.

Dr. C. Rajarajachozhan received the B.E. degree in electronics and communication engineering, M.E. degree in Communication Systems and Ph.D. degree from the Anna University, Chennai in the year of 2007, 2010, and 2020, respectively. Presently, he is working as an assistant professor in the Electronics and Communication Engineering Department at the University College of Engineering, Kancheepuram. His research interests include semiconductor device modelling and technology. He can be contacted at email: chozhanacademic@gmail.com.

Dr. M. Batumalay earned her master's degree in engineering from the University of Malaya, Malaysia, and subsequently pursued her Ph.D. in Photonics Engineering at the same institution. Her research focuses on lasers, fiber optics, and fiber sensors. Previously, she invented fiber optics into sensors capable of detecting changes in relative humidity and chemical solutions. She collaborates with both local and international researchers to delve deeper into the behavior and characteristics of fiber optics sensors and plasmonic sensors, resulting in numerous high-quality publications in relevant journals. Additionally, she actively serves as a reviewer for several journals and holds a committee position in the Optical Society of Malaysia (OSM), where she contributes to activities involving young researchers. Furthermore, she is also registered as a professional engineer with the Board of Engineers Malaysia (BEM) and as a Chartered Engineer with The Institution of Engineering and Technology (IET). Presently associated with a prestigious private university in Malaysia, renowned for its expertise in communication, networking, and cloud computing, she holds pivotal leadership positions. As the Director of the Center for Data Science and Sustainable Technologies, the Chair of the University Research Committee, and the Chief Internal Auditor for Malaysia Research Assessment, he epitomizes academic excellence. She is actively contributing as a Managing Editor for the Journal of Innovation and Technology (JOIT). Her fervent aspiration is to engage with emerging talents and prospective research candidates, thereby enhancing the academic landscape. She can be contacted at email: malathy.batumalay@newinti.edu.my.

Dr. S. P. Manikandan holds a B.E. degree in Electronics and Communication Engineering from PSN College of Engineering and Technology, affiliated with Anna University. Following his undergraduate studies, he completed his M.E. in embedded systems and technologies from Sri Ram Engineering College, affiliated with Anna University. He has completed a Ph.D. at Dr. M.G.R. Educational and Research Institute. Now, he is working at Saveetha Engineering College, Thandalam, Chennai. He specializes in key subjects such as digital electronics, circuits and devices, and linear integrated circuits. With over 15 years of teaching experience, he has actively enhanced his academic knowledge through participation in various NPTEL and SWAYAM courses. He has made significant contributions to research and innovation, having published patents and books. He has also presented papers at numerous national and international conferences and published his research in reputed Scopus-indexed journals. He can be contacted at email: drmanikandansp@gmail.com.