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Design and analysis of modified single switch AC-DC bridgeless Cuk converter

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ABSTRACT

The Cuk converter is widely used in power electronics due to its ability to provide both step-up and step-down voltage conversion with low ripple characteristics. However, conventional designs suffer from increased component count, higher losses, and significant voltage stress on switching devices. In this paper, an improved single-switch bridgeless AC-DC Ćuk converter is proposed for power factor correction (PFC) and loss reduction. The proposed topology employs a two-stage integrated structure with two low-value coupling capacitors (1 μF each). These capacitors effectively reduce voltage stress across the main switch and enhance switching performance. The operating principles of the proposed converter are analyzed under different switching conditions, highlighting its improved dynamic behavior and reduced component stress. Simulations using MATLAB/Simulink show that the proposed design achieves high efficiency, very low output voltage ripple (less than 1%), and a near-unity power factor of 0.9988. This performance, particularly the fast dynamic response, was achieved using a specially designed proportional-integral (PI) controller for output voltage regulation. The converter demonstrates fast dynamic response with a settling time of less than 0.23 s and a maximum overshoot of 7.5% under sudden load and input variations. Compared to conventional two-switch topologies, the proposed design significantly reduces switch voltage stress while maintaining a simpler structure, leading to lower cost and compact size. These results confirm that the proposed converter is a promising solution for high power quality applications.

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1. INTRODUCTION

Electric companies produce many devices that use different DC voltage levels in the same circuit. To solve this problem, engineers strive to design circuits to fulfil these requirements [1]-[3]. DC-to-DC converters provide a wide range of voltage and current. These circuits are considered essential for many electronic devices such as switch-mode power supplies (SMPS), laptop computers, medical devices, electric vehicles, DC transmission lines, and microgrids [4]-[6]. These converters provide a wide range of voltage and current. The Cuk converter is a unique solution in this field, due to its ability to achieve step-up and step-down output voltages using PWM, while minimizing ripples in the input and output currents [7], [8]. However, conventional models of this converter often suffer from design complexity, a high number of components, increased losses, and challenges in improving power factor (PFC).

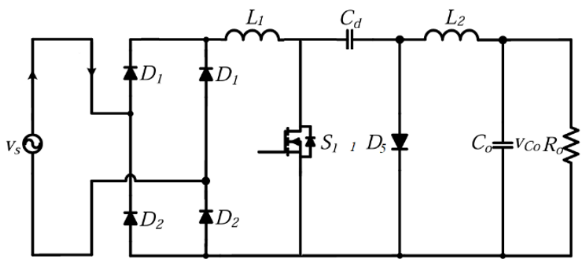
In response to these challenges, this research proposes an improved design for a single-switch Ćuk Bridgeless Converter, which combines the rectifier stage and the switching stage in a single structure, reducing the number of active and passive components and improving the system's dynamic response. The proposed design relies on the use of carefully selected inductors and capacitors to reduce voltage and current stress on the power elements and minimize total harmonic distortion (THD) in the input current. The performance of this design was verified through comprehensive modelling and simulation using MATLAB/Simulink, where the efficiency, power factor, and output voltage quality were evaluated under various operating conditions. Furthermore, to enhance the dynamic performance and improve voltage regulation, a proportional-integral (PI) controller is integrated with the simulation model in this work. This controller is designed to effectively regulate the duty cycle, directly contributing to the fast settling time and limited overshoot as demonstrated in the simulation results. The remaining parts of this paper include: comparison between previous Cuk inverters and the proposed design, circuit structure and operation analysis, simulation results, and finally, the conclusion.

2. PREVIOUS CUK CONVERTERS VERSUS PROPOSED DESIGN

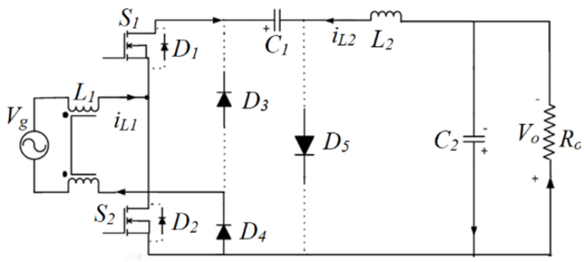
Figure 1 illustrates some types of Cuk converter circuits. In Figure 1(a), the Cuk converter is constructed by combining two stages. The first stage is a full-wave rectifier that converts the alternating voltages to direct voltages. The second stage represents the chopper circuit (such as buck, boost, or buck-boost) to obtain a variable level of output voltages. This Cuk converter can provide both step-up and step-down output voltage using the PWM technique [9]-[12].

In Figure 1(b), the designers combined both stages into one circuit to overcome the high level of harmonics resulting from the traditional circuit. Two diodes were replaced by two switches, which make the modified model with a strong dynamic response, easy to isolate, and built-in inrush current restriction under transients and overload conditions [13]-[20].

Figure 2 depicts the suggested bridgeless PFC Cuk converter circuit. In this instance, the structure has less complexity by controlling a single MOSFET switch instead of two MOSFETs as in Figure 1(b) above. In addition, it has a small-sized inductor with lower loss as compared with the other schemes given in the previous studies [21], [22]. Due to its two switches, the bridgeless PFC structure is more complex in implementation and control; the structure is suggested to lessen the complexity by controlling a single MOSFET switch instead of two MOSFETs as in Figure 1(b) [23]-[26].



(a)



(b)

Figure 1. Two configurations of Cuk converter: (a) traditional two-stage type and (b) modified single-stage type with two switches

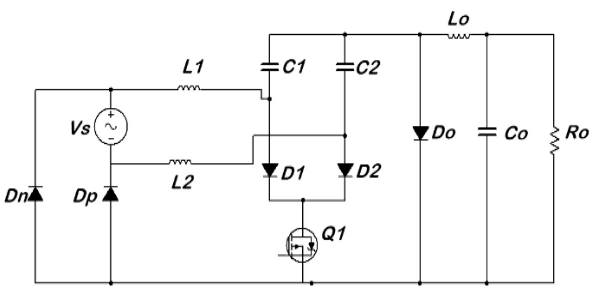


Figure 2. Modified single-switch bridgeless AC-DC Cuk converter

3. CIRCUIT OPERATION AND ANALYSIS

The circuit-proposed bridgeless Cuk converter analysis is carried out assuming all converter components are perfect. Furthermore, the power converter is expected to have a steady-state operation with a constant input voltage (Vs) and output voltage (Vo). The converter is studied only during the positive half-line cycle since the action is regular for two halves of the input voltage waveform. Thus, as seen in Figures 3 and 4, the circuit displays two modes during the switching time (TS) [27], [28].

3.1. Mode 1

When the positive cycle is applied as demonstrated in Figure 3, switch Q1 is turned ON, while the diodes (D2, Do and Dn) are in reverse bias. The operation of this mode has four paths. Path (1) is represented by the inductor current (iL1) flowing through D1, Q1, and returning through Dp to the source. The current (iL1) starts to increase linearly with a slope of (Vs/L1), then the inductor (L1) is magnetized to supply the voltage (VS). Path (2) is represented by capacitors (C1 and C2), Vs, L1, and L2. Path (3) is represented by coupling C1, D1, Q1, Co, and Lo. During this path, the energy stored in C1 is transferred to Co and Lo. In path (4), the output capacitor (Co) transfers energy to the load (Ro).

$$V_S = L_1 \frac{di_{L1}}{dt} \tag{1}$$

$$-i_{Lo} = C_o \frac{dv_{Co}}{dt} + \frac{V_o}{R_o} \tag{2}$$

$$dv_{Co} = \frac{i_{Co}}{C_o} dt \tag{3}$$

$$V_o = V_{Co} \tag{4}$$

$$V_o = V_{C1} - V_{Lo} \tag{5}$$

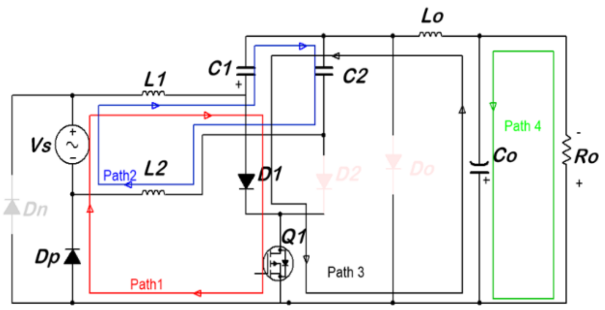


Figure 3. The configurations during the positive half-line cycle when Q1 is ON and Do is OFF

3.2. Mode 2

When the positive cycle is applied as shown in Figure 4, switch Q1 is turned OFF. In this operation mode, four paths are available, the D1, D2, and Dn are in reverse bias. In path (1), inductor (L_1) is magnetized to supply voltage (V_s- V_{c1}), the current (i_{L1}) of input inductor (L_1) increases linearly by slope of (V_s-V_{C1}/L_1). This path, represented by the current (i_{L1}) flows through L_1, C_1, Do and returns through Dp to the source. Simultaneously, the circulating current flowing through V_s, L_1, C_1, C_2, and L_2, with the same direction is denoted path (2), at the same time, energy in output inductor (L_O) is transported to capacitor (C_O) as denoted by path (3), on the other hand the C_o transferred energy to load (R_o) through path (4).

$$V_{C1} = V_S - L_1 \frac{di_L}{dt} \tag{6}$$

$$V_{Co} = V_{Lo} = L_o \frac{di_{Lo}}{dt} \tag{7}$$

$$C_o \frac{dv_{Co}}{dt} = i_{Lo} - \frac{V_o}{R_o} \tag{8}$$

$$V_o = R_o * I_o \tag{9}$$

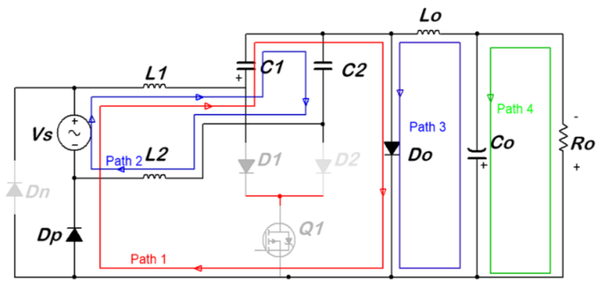


Figure 4. The outlines through the positive cycle when Q1 is OFF and Do is ON

4. CIRCUIT STRUCTURE

The designs of the AC-DC converters that are now on the market do not entirely meet the standards. Every industry desires an AC-DC converter with a promising performance that includes tight tolerances and ripple-free output current. For this reason, the authors are inspired to design and develop a new topology for the AC-DC converter to enable concurrent boost and buck operation. In addition to reliable operation and effective switching that leads to minimize ripple and verify superior power quality [29].

Modified Cuk converter has advantages such as minimizing the peak current of the power electronic device switch and lowering ripple on source current, power factor is improved by lowering ripple AC side harmonics and source current's THD. However, the converter's inductor coupling results in a slight weight and size reduction, the shared current lowers the rated current's magnitude. This enhances dynamic performance and lowers switch current stress. Because ripple reduction lowers losses, efficiency is also increased.

4.1. Voltage conversion (M)

According to the power balance principle, the steady-state average power across the lossless converter is zero [30].

$$P_{ac}(t) = \frac{2}{T}\int_0^{\frac{T}{2}} V_{ac}(t)\cdot I_{ac}(t)dt \tag{10}$$

The average AC supply current is as in (11).

$$I_{AC} = \frac{V_{AC}}{R_{ein}} \tag{11}$$

The effective input resistance is given by (12).

$$R_e = \frac{2*L_e}{T_S*D} \tag{12}$$

The ratio of voltage conversion M is produced by dividing the output DC voltage by the average AC input voltage:

$$M = \frac{V_{dc}}{V_{in}} = \frac{V_{dc}}{\sqrt{2}\cdot V_s} \tag{13}$$

A Cuk converter's voltage conversion ratio can be raised in one of two ways: The switch that regulates the inductor's charging and discharging should have its duty cycle increased. As a result, the inductor will retain more energy and the output capacitor and load resistor will receive more energy. Either raise the load resistance or decrease the output capacitance. This will shorten the inductor's energy release into the output circuit and raise the inductor's terminal voltage [30].

4.2. Inductor design

To a certain extent, the quality of the AC source current is improved by the inductors on either side of Cuk converters, which lessen the ripples in the source and load currents [27].

$$L_1 = L_2 = \frac{(V_S - V_C)*D}{I_L * f_{sw}} \tag{14}$$

A converter's total size and weight expand with the number of inductors it includes. One of the main problems with converters used in servers is their size and compatibility [31].

4.3. Choice of coupling capacitor and output capacitor

Due to their significant impact on the input inductor, output inductor, switching frequency, and the input line current quality, the coupling capacitors C_1 and C_2 are crucial components of the modified Cuk strategy. Capacitors C_1 and C_2 must be chosen so that the output voltage has the least amount of switching voltage ripple and that their steady-state voltages closely resemble the rectified input AC line voltage waveform [32].

$$C_1 = \frac{1}{(2\pi\, f_{sw})^2 * (L_1 + L_o)} \tag{15}$$

$$C_o = \frac{(\Delta I_o)}{4\pi(\Delta V_o) * (f_{sw})} \tag{16}$$

The capacitors C_1 and C_2 are assembled in such a way as to conduct energy from the input to the output stage with constant voltage; in steady state, the average inductor voltages V_{L1a}, V_{L1b}, V_{L2a}, and V_{L2b} are zero. These inductor voltages are useful in calculating the output voltage equation via volt-second balance. However, the output capacitors must be big enough to store the energy needed to balance the difference between the constant load power and the time-varying input power [33].

$$f_l < f_r < f_s \tag{17}$$

The resonant frequency (f_r) must be lower than the frequency (f_s) and must be higher than the frequency (f_l).

4.4. Power MOSFET selection

The gate-drain charge (Q_{GD}), the maximum drain-to-source voltage ($V_{DS(max)}$), the on-resistance ($R_{DS(ON)}$), and the minimum threshold voltage ($V_{th(min)}$) are the factors that influence the MOSFET selection. Depending on the gate drive voltage, the MOSFETs are working with a switch voltage equal to V_{in}+V_{out}. Nonetheless, the duty ratio for the boost operation is significantly higher than 0.5. Therefore, the design is inadequate for boost operation due to the stress on the switching device Q1 caused by the maximum current and duty ratio exceeding 0.5. The reduction in switch current simplifies the cooling arrangements and reduces the size of the switching devices [34].

4.5. Output diode selection

Both the peak current and the reverse voltage must be handled by the output diode selection in this converter. The peak current passes through a chosen diode.

$$I_{Do} = I_{L1} + I_{LO} \tag{18}$$

The power loss of the diode is equal to the current pass multiplied by the voltage across it; therefore, Schottky diodes must be used to reduce power dissipation [34].

$$V_{D\,reverse} = V_{CO} + V_{LO} \tag{19}$$

Table 1 compares the previous types to the Cuk Converter and the converter proposed in this work.

Table 1. Comparison of different Cuk configurations

Parameter	Classical Cuk converter [9]	Bridgeless Cuk converter [15]	Modified Cuk converter
Switch	1	2	1
Diode	5	4	5
Inductor	2	3	3
Capacitor	3	3	3
Total no. of components	11	12	12
Voltage gain	$M = \frac{D}{1-D}$	$M = \frac{D}{1-D}$	$M = \frac{D}{1-D}$
Switch	$(1+M)V_i$	$(V_o + V_i)$	$\frac{V_o}{D}$
Voltage stress	$M^2 \frac{V_i}{R}$	$(1+M)\frac{V_i + V_o}{R}$	$(2+M)\frac{V_i}{R}$

5. SIMULATION RESULT AND DISCUSSION

In this section, the MATLAB/Simulink simulation of the modified bridgeless Cuk converter in Simscape Electrical is shown in Figure 5. This model was simulated using MATLAB 2020a for an input AC voltage of 220 V. The simulation parameters of this model are listed in Table 2. The model is assessed under steady-state operating conditions with a constant load by applying the PWM technique to the switch (Q1), turning it ON and OFF once per cycle for energy transmission. Figure 6 gives the PWM applied to Q1. The input voltage and current flowing through the input inductor (L1) are shown in Figures 7 and 8, respectively. Figure 9 illustrates the relation between input voltage and input current (IL1). The observed results in Figure 9 confirm the success of the proposed model in achieving PFC, where the input current closely follows the sinusoidal shape of the input voltage, exhibiting high accuracy with no noticeable phase shift. Figure 10 shows the DC output voltage of the Cuk converter. The converter successfully regulates the DC output voltage, quickly stabilizing at the target value of approximately -400 V (reversed polarity is a characteristic of the Cuk converter).

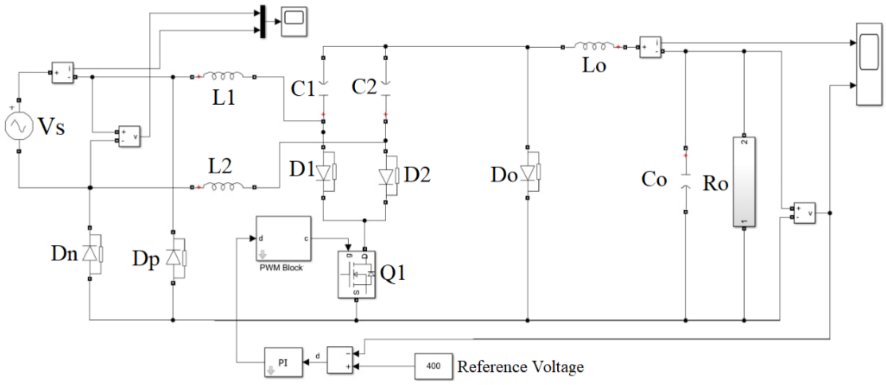


Figure 5. MATLAB model

Table 2. Modified single-switch bridgeless AC-DC Cuk converter parameters

Description	Variable	Value	Unit	Description	Variable	Value	Unit
Input voltage	Vs	220	volt	Output voltage	Vo	80-420	V
Frequency	F_{in}	50	Hz	Coupling cap.	C1	1.0	µF
Inductor 1	L1	2.9	mH	Coupling cap.	C2	1.0	µF
Inductor2	L2	2.9	mH	O/P capacitor	Co	1200	µF
O/P inductor	Lo	25.5	mH	Switching Freq.	Fsw	10000	Hz
Power	P	500	watt	Duty	D	40%	

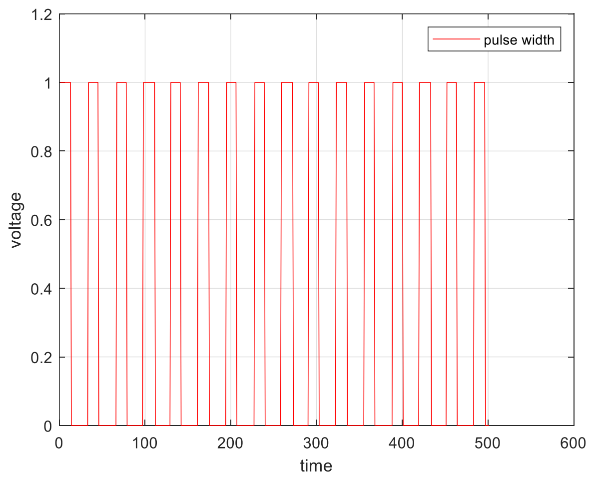


Figure 6. Pulse width modulation applied on Q1

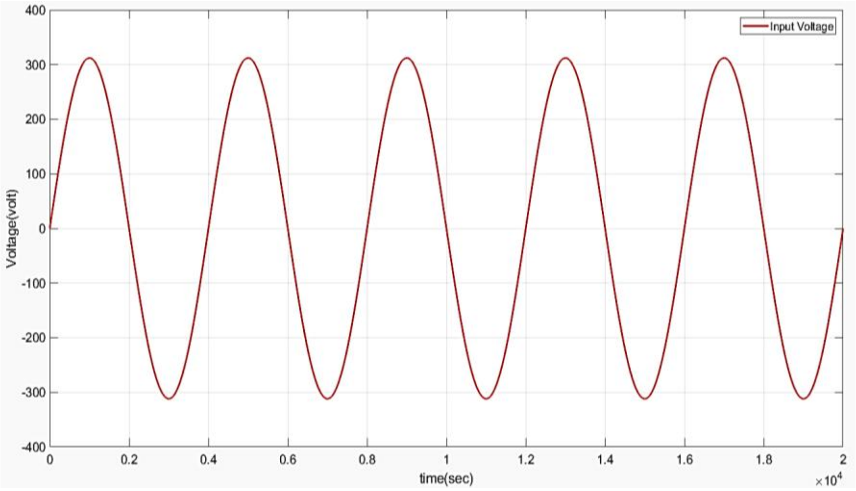


Figure 7. AC input voltage

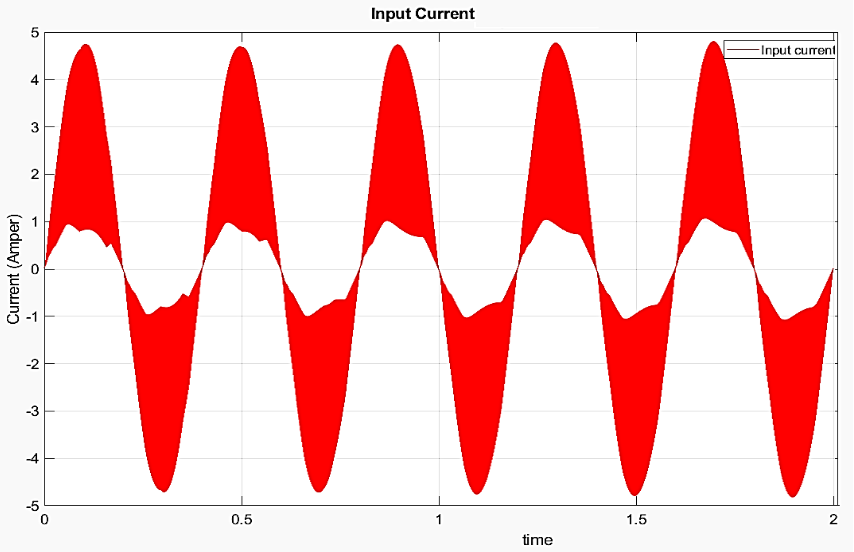


Figure 8. AC input current

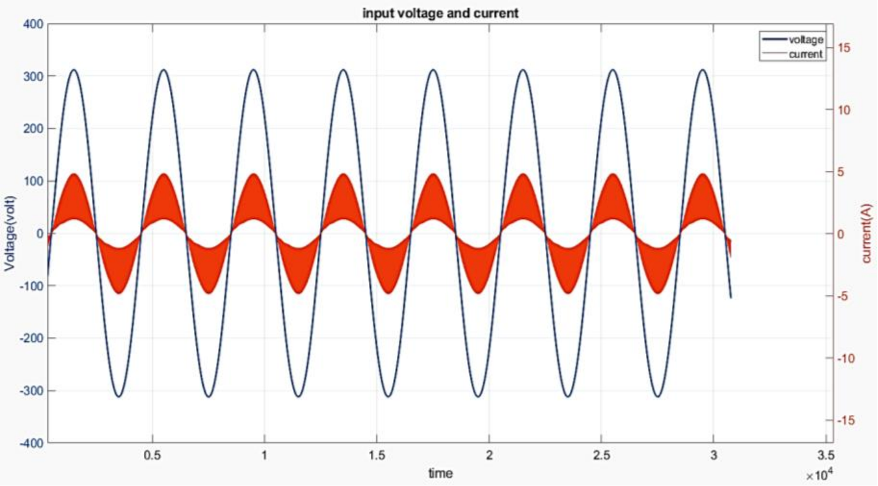


Figure 9. Relation between input voltage and current

Figure 11 shows that the output voltage ripple is very low when reaching steady-state operation. This demonstrates the effectiveness of the output filters and provides pure, stable DC power to the load. Figure 12 confirms that the power factor stabilizes at a value very close to unity (PF ≈ 1.0) (reaching 0.9988 at the measurement points). This demonstrates the converter's excellent performance in drawing efficient power from the source.

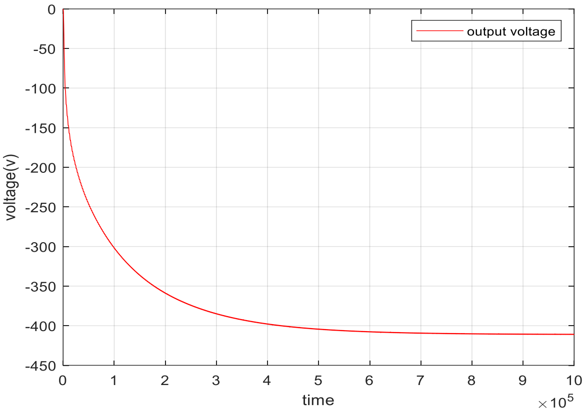


Figure 10. Output voltage of modified system

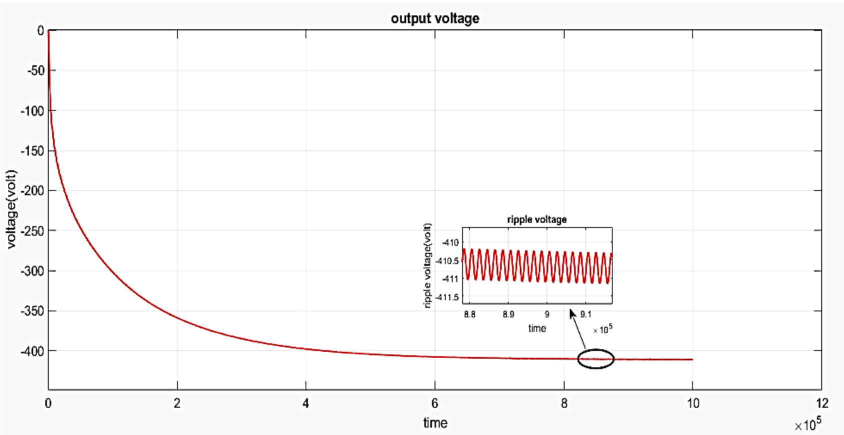


Figure 11. Output voltage ripple

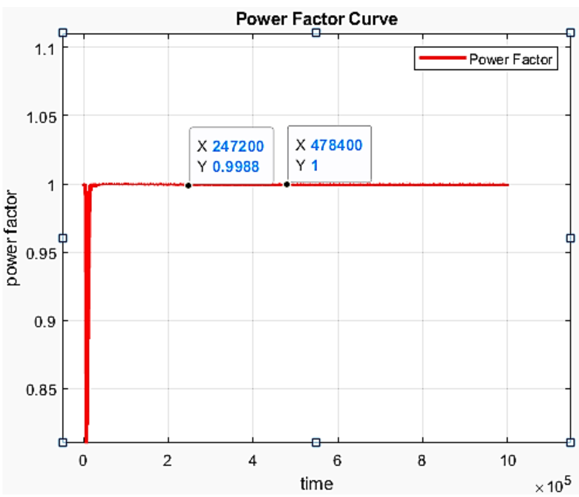


Figure 12. Power factor curve

The converter's performance was evaluated under dynamic load changes, as shown in Figure 13. The load was changed from 500 W to 250 W at 0.4 seconds and then back to 500 W at 0.8 seconds. The system demonstrated a rapid and stable response, with a settling time of approximately 0.23 seconds and an overshoot of 6.25% after the first load change (500 W → 250 W). When the load was increased back to 500 W at 0.8 seconds, the converter exhibited a settling time of approximately 0.1 seconds and an undershoot of 7.5%, confirming the robustness of the converter design and its ability to efficiently handle varying operating conditions over a total time frame of 1.2 seconds.

Figure 14 illustrates the converter's performance under a sudden change in input voltage (blue line). The input voltage dropped from 312 Vp to 150 Vp in 0.4 seconds and then rose again to 312 Vp in 0.8 seconds. The system demonstrated a stable response, with a settling time of less than 0.1 seconds after the initial change and a 7.5% undershoot (from 400 to 370 V). Upon an input surge of 0.8 seconds, the converter also recorded a 7.5% overshoot (from 400 to 430 V) with a settling time of approximately 0.1 seconds, confirming the robustness of the converter design and its ability to handle sharp supply voltage fluctuations while maintaining a symmetrical response. The dynamic results in Figures 13 and 14 were obtained using a PI controller tuned via the Ziegler-Nichols method, with final gains of Kp = 0.05 and Ki = 2.5.

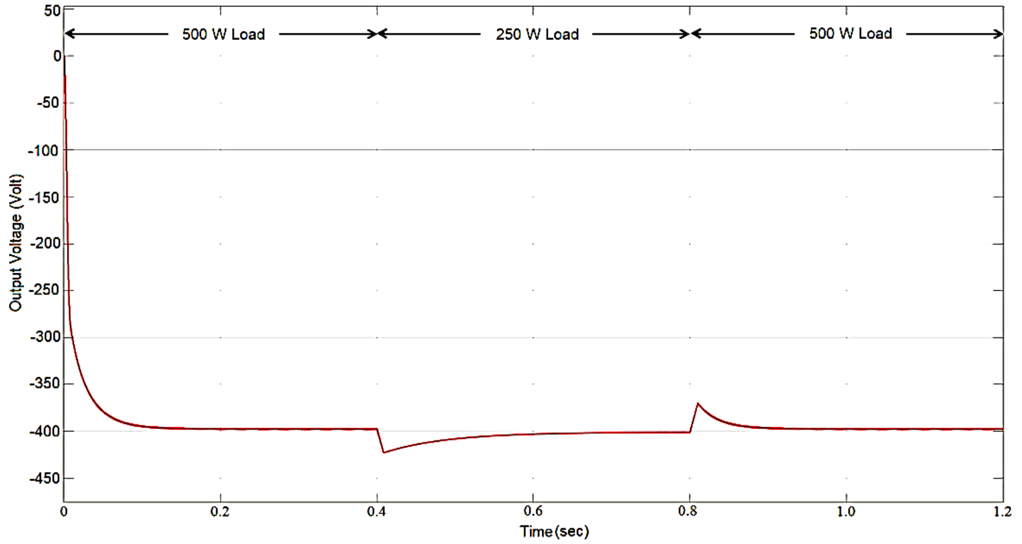


Figure 13. Output voltage dynamic load changes

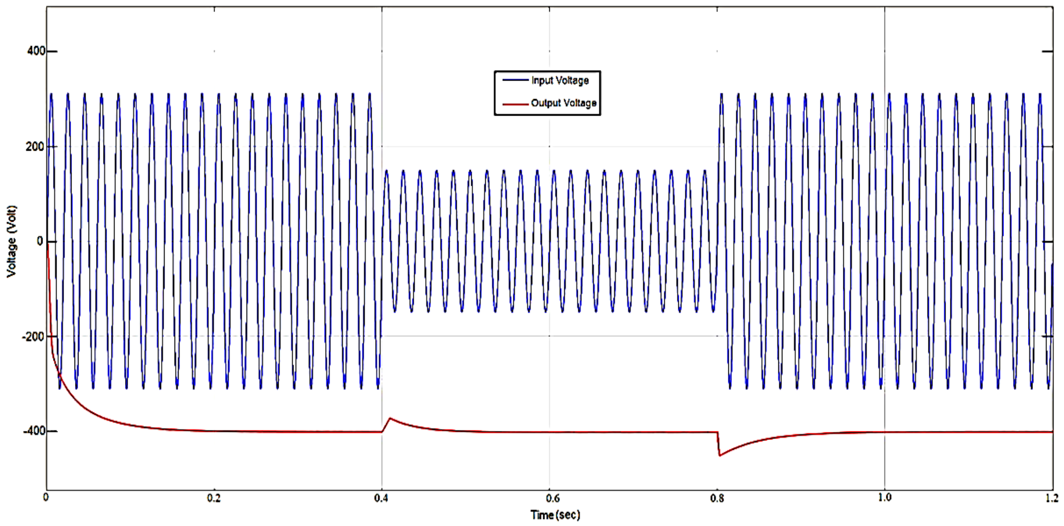


Figure 14. Output and input voltages under a sudden change in input voltage

6. CONCLUSION

The proposed modified single-switch bridgeless Ćuk converter demonstrates effective performance in power factor correction applications, achieving a near-unity power factor of 0.9988, low output voltage ripple (less than 1%), and fast dynamic response under load and input variations. The integration of rectification and buck–boost stages into a single-switch structure significantly reduces circuit complexity, component count, and conduction losses, making the design suitable for compact and cost-effective power supply applications. In addition, the use of low-value coupling capacitors effectively reduces voltage stress across the main switch, enhancing reliability and overall system efficiency compared to conventional topologies. However, this study is limited to simulation-based validation under ideal operating conditions. Practical factors such as parasitic elements, switching losses, thermal effects, and electromagnetic interference have not been considered, which may affect real-world performance. Furthermore, THD analysis and detailed quantitative comparison with other converter topologies were not fully addressed. Future work will focus on experimental implementation and hardware validation of the proposed converter, including detailed efficiency, THD, and thermal analysis. In addition, advanced control strategies such as fuzzy logic and model predictive control will be investigated to further enhance dynamic performance. A comprehensive comparative study with other PFC converter topologies under identical operating conditions will also be conducted to validate the effectiveness of the proposed design.

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The authors declare that no funding was received for this research.

AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

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Hassan Wahhab Salih		✓				✓	✓	✓		✓	✓	✓		
Nasir Hussein Selman	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

The authors declare that they have no conflict of interest.

DATA AVAILABILITY

The data supporting the findings of this study are presented within the manuscript.

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