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Optocoupler-based closed-loop hysteresis control for buck converter: experimental results

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ABSTRACT

This work experimentally evaluates a simplified closed-loop on–off (hysteresis) controller for a single-phase buck converter using an LM324 comparator and an optocoupler-based gate drive to the IRF830 MOSFET. The controller compares the output voltage against a reference and drives the switch in a binary manner, yielding variable-frequency regulation with low component count. Performance is assessed for DC–DC regulation and dynamic reference tracking under sinusoidal, triangular, and rectangular waveforms at 1 Hz and 60 Hz, as well as under input-voltage droop, load perturbations, and real-time changes in reference waveform. Results show envelope-accurate tracking with fast transients and bounded ripple across all tested conditions, including representative grid-frequency operation. The controller maintains stability and preserves waveform fidelity despite supply and load disturbances; edge transients observed for rectangular references at 60 Hz are consistent with expected output-capacitor dynamics and remain bounded. The findings support the suitability of analogue on–off hysteresis with optocoupler isolation as a low-complexity approach for applications requiring efficient DC–DC conversion and dynamic signal tracking, especially where cost, simplicity, and rapid response are prioritized.

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1. INTRODUCTION

Buck converters are a fundamental technology for reducing DC system output voltage using non-dissipative components such as inductors, capacitors, and controlled switches [1]. While the basic principle relies on commutation, finding optimal control strategies remains a highly active research field. Recent literature highlights various applications, including buck controls for electric vehicle (EV) charging stations [2]-[6] and strategies oriented toward extending battery life [5], [6]. Furthermore, research has focused on the efficiency analysis of different control strategies [7], [8] and the proposal of entirely new control paradigms for buck converters [9]-[11].

This article presents an experimental evaluation of a simplified closed-loop on-off (hysteresis-type) control strategy for a single-phase buck converter. The system uses an LM324 operational amplifier and optocoupling to compare the output voltage with a reference, generating a binary signal to regulate performance. Within the broader context of power electronics, this approach is recognized as one of the standard control modalities alongside voltage-mode control (VMC), current-mode control (CMC), and sliding-mode control (SMC) [12].

Hysteresis control (HC) is a legitimate and widely studied alternative to digital or model-based schemes, prioritized for its fast switching, robust boundary-based regulation, and hardware simplicity [12], [13]. While literature often contrasts HC with more advanced strategies such as sliding-mode variants or adaptive schemes that offer superior disturbance rejection [14], [15]. HC remains favored for its rapid transient response and ease of implementation [14]-[17]. Furthermore, although digital controllers such as PID or model-predictive schemes can provide higher precision and steady-state accuracy [18], [19], carefully designed low-complexity analogue controllers can still achieve effective dynamic tracking for various reference trajectories, such as step or ramp variations [19], [20].

The practical appeal of this analogue approach lies in its low computational burden and cost-effectiveness [12], [19]. The hardware realization, involving opto-isolation and op-amp-based error processing, reflects established architectures used in applications such as voltage regulator modules (VRMs) [21], [22]. Research indicates that such analogue paths can provide robust regulation and high fidelity in dynamic tracking, even under nonlinear-load conditions [23], effectively emulating AC-like profiles from DC sources [14], [15], [20].

The experiments reported here test this controller's ability to track dynamic references, including sinusoidal, triangular, and rectangular waveforms, and its robustness against supply drops and load changes [13]-[15]. The results align with the performance envelopes of more complex robust-control strategies [14], [15], confirming that a simplified analogue HC approach is a viable design path for applications where hardware simplicity and speed are paramount [12], [19]. While more sophisticated approaches may be advantageous for extremely tight regulation [14]-[16], the proposed system demonstrates high fidelity across a broad range of operating scenarios [18], [19].

The remainder of this article is organized as follows: i) Section 2 details the design and implementation of the buck converter and its controller; ii) Section 3 presents experimental and simulation results demonstrating the system's rapid response and tracking efficiency; and iii) Final findings underscore the suitability of this low-complexity architecture for efficient voltage regulation and dynamic signal tracking.

2. METHOD

This section details the design and implementation of the buck converter and the analogue closed-loop on-off controller, including component sizing, hardware architecture, and the experimental-simulation workflow adopted for validation.

2.1. Buck converter design

Component selection followed standard design criteria [24], [25] to ensure continuous conduction and bounded output ripple under the operating envelope explored experimentally. The relationship between parameters was found by comparing the performance of the system when the switch was closed and open, looking for parameters that would guarantee continuous conduction during the experiment.

The inductor lower bound and capacitor upper bound were determined using the relations in equations (1)-(2), which were developed by [24], as the boundary parameters to guarantee continuous conduction. $f = 40$ kHz chosen as a conservative switching-frequency reference given the variable commutation inherent to analogue hysteresis control, and $\Delta V \leq 3\%$ of V_{out} as the ripple constraint. Load resistance for each operating point was measured experimentally and used directly in sizing calculations, acknowledging its voltage dependence in the employed load module.

$$L_{min} = \frac{V_{in} * R}{8 * V_{out} * f} \tag{1}$$

$$C_{max} = \frac{V_{in} * R}{32 * L * \Delta V * f^2} \tag{2}$$

A design table was compiled to evaluate L_{min} and C_{max} across representative pairs (V_{in}, V_{out}) and measured R, which guided a hardware selection of $C = 100\ \mu$F and $L = 0.457$ mH to satisfy constraints throughout the tested range. The final converter topology is the canonical step-down stage with input source, high-side controlled switch, catch diode, output inductor, and shunt capacitor feeding the resistive load, as depicted in Figure 1 with the adopted parameter values annotated, which follow the limits shown in Table 1. On the left side of the figure, the buck converter with real parameters is shown, while on the right side, the buck converter implemented in the laboratory is presented.

2.2. Analog control design

The control system for the buck converter consists of an LM324 operational amplifier that compares the V_{out} at any given time with a reference signal V_{ref}, and works as an on-off signal that enters an optocoupler

HCPL-3120, which is supplied by a 15 V source, which is the signal provided to the gate of the IRF830 MOSFET. The control setup is shown in Figure 2, which shows the case of a buck controller with a V_{ref} of 10 V.

Table 1. Design criteria for the inductance and capacitance of the buck converter

Input voltage	Output voltage	Resistance (Ω)	Minimum inductance (H)	Maximum capacitance (F)
10	5.0	11.2	7.0E-5	1.9E-5
	10.0	16.0	5.0E-5	1.3E-5
20	5.0	15.3	1.4E-4	1.9E-5
	10.0	16.0	1.0E-4	1.3E-5

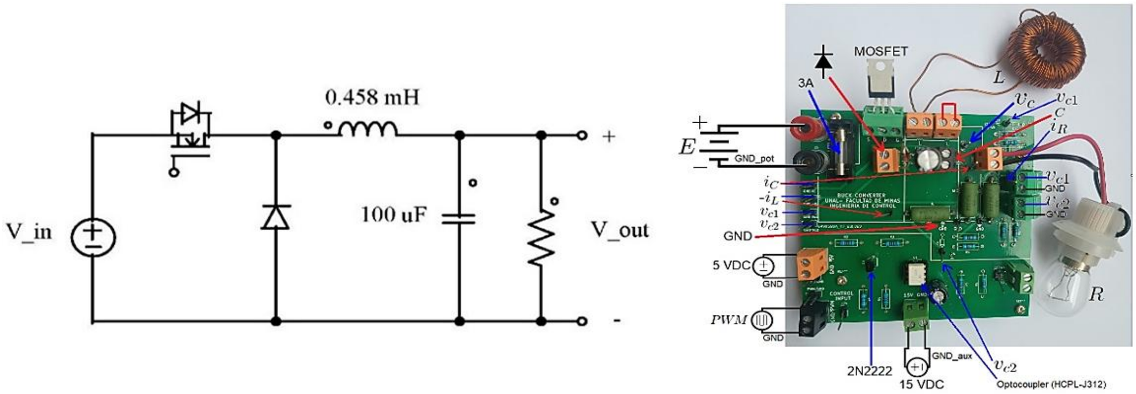

Figure 1. Buck converter with real parameters and laboratory implementation

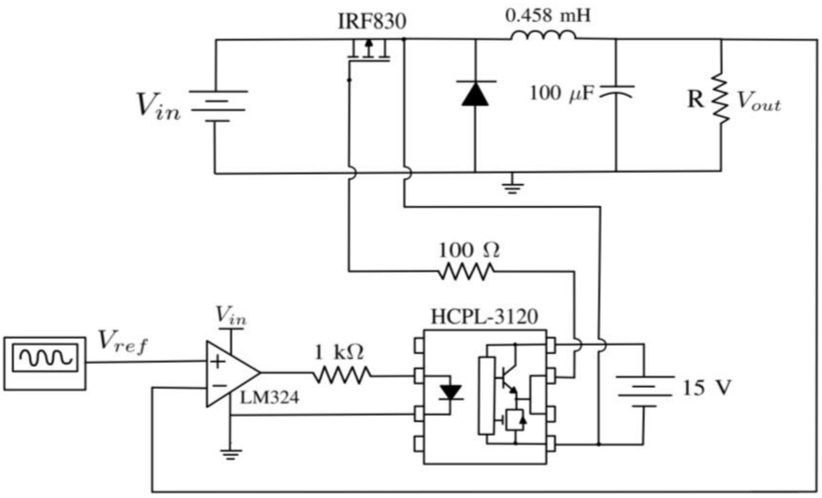

Figure 2. Buck converter with its closed-loop control

2.3. Experimental procedure and simulation

The evaluation stage comprised: i) DC–DC regulation over $V_{ref} \in [0, V_{in}]$, ii) dynamic tracking for sinusoidal, triangular, and rectangular V_{ref} at 1 Hz and 60 Hz, and iii) disturbance response under input voltage droop, load addition/removal, and in situ changes of V_{ref} waveform class. Time-domain measurements were collected on the laboratory prototype and benchmarked against PSIM simulations configured with the same component values and reference trajectories to assess correlation and to visualize high-frequency ripple not fully resolved in the experimental captures.

3. RESULTS AND DISCUSSION

This section reports time-domain performance for tracking experiments and disturbance tests, alongside comparisons with simulation to contextualize ripples, dynamics, and waveform fidelity.

3.1. Tracking of sinusoidal references

For a 5 V peak sinusoid with 2.5 V offset, the prototype exhibits close waveform conformity at 1 Hz and 60 Hz, with minimal phase lag and small ripple consistent with boundary-switching regulation, as shown in Figures 3-6 (experimental vs. PSIM). The 60 Hz case, representative of grid-frequency dynamics, is tracked with negligible distortion relative to the reference envelope, supporting suitability for applications requiring DC-sourced emulation of AC-like profiles at fundamental frequency.

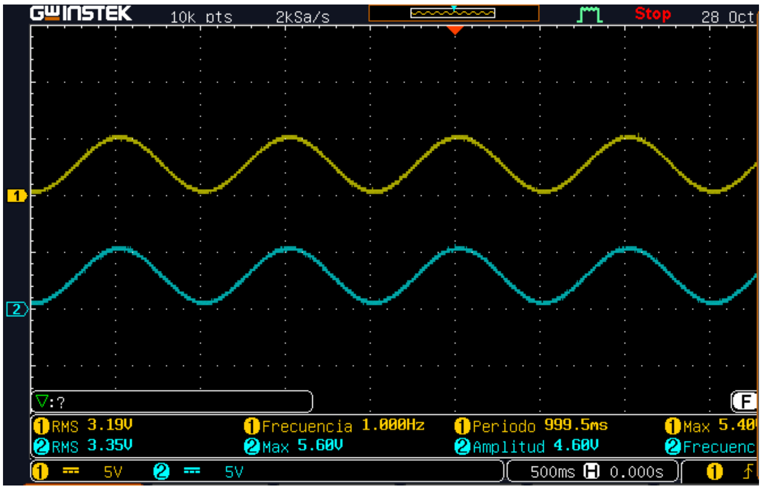

Figure 3. Time response for sinusoidal V_{ref} behavior at 5 V amplitude and 1 Hz frequency

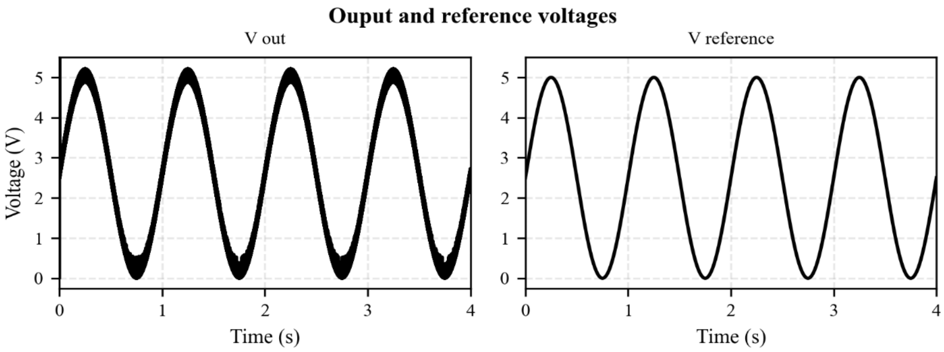

Figure 4. Time response for sinusoidal V_{ref} behavior at 5 V amplitude and 1 Hz frequency

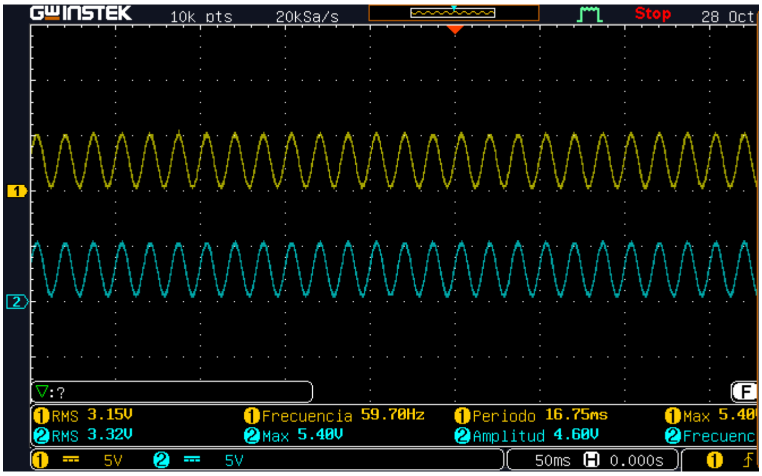

Figure 5. Time response for sinusoidal V_{ref} behavior at 5 V amplitude and 60 Hz frequency

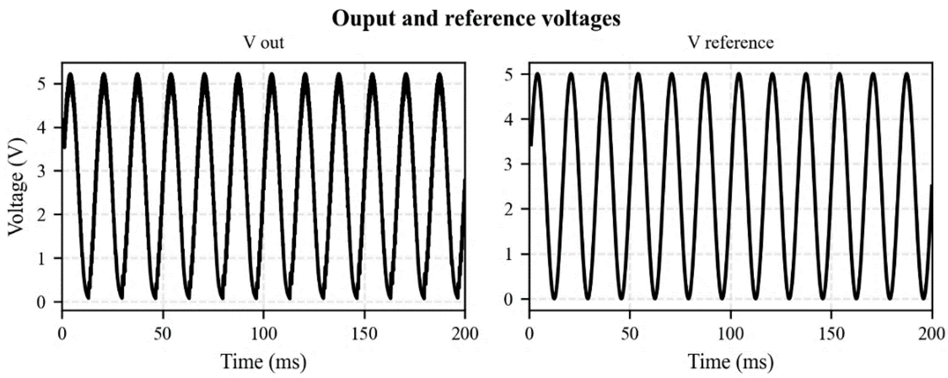

Figure 6. Time response for sinusoidal V_{ref} behavior at 5 V amplitude and 60 Hz frequency

3.2. Tracking of triangular references

Triangular references at 1 Hz and 60 Hz are tracked with low steady-state error and small ripple superimposed on the ramp segments, as illustrated in Figures 7-10. The simulation traces resolve the switching ripple more clearly, while the experimental captures emphasize the envelope fidelity; the agreement between both indicates that the variable-frequency hysteresis behavior remains bounded and does not compromise macroscopic tracking across the tested slopes.

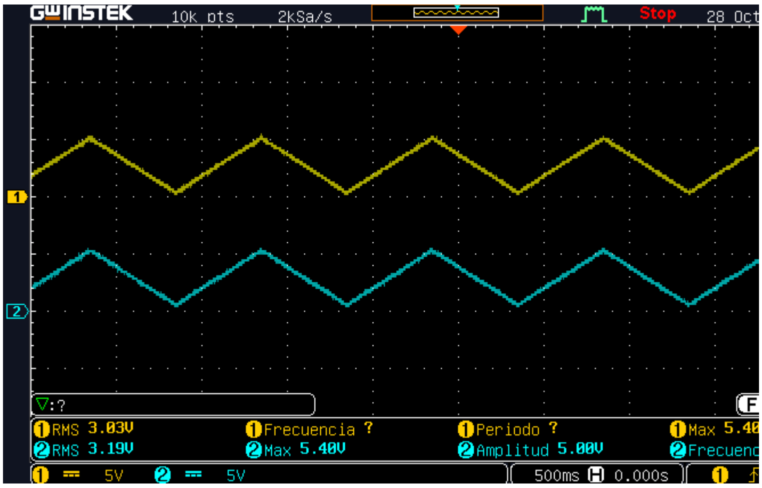

Figure 7. Time response for triangular V_{ref} behavior at 5 V amplitude and 1 Hz frequency

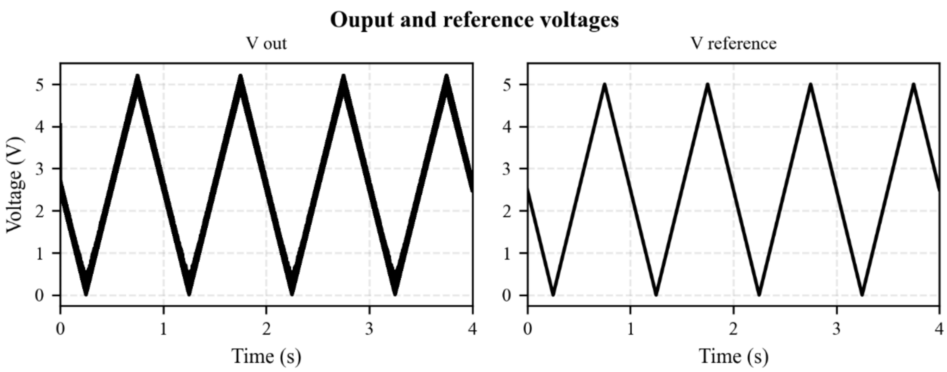

Figure 8. Time response for triangular V_{ref} behavior at 5 V amplitude and 1 Hz frequency

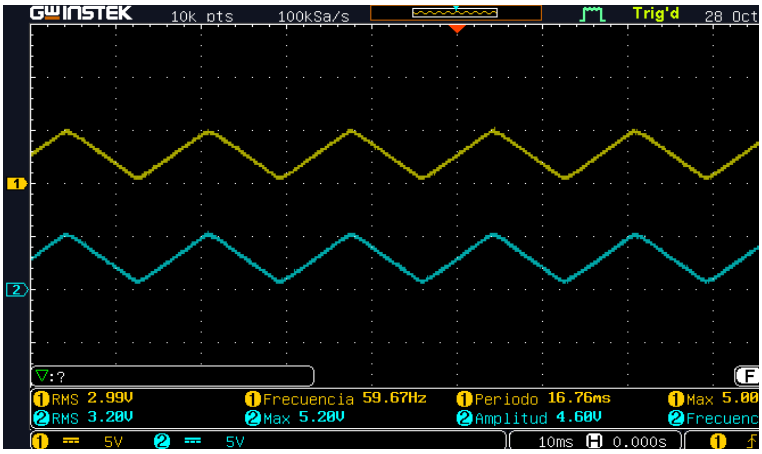

Figure 9. Time response for triangular V_{ref} behavior at 5 V amplitude and 60 Hz frequency

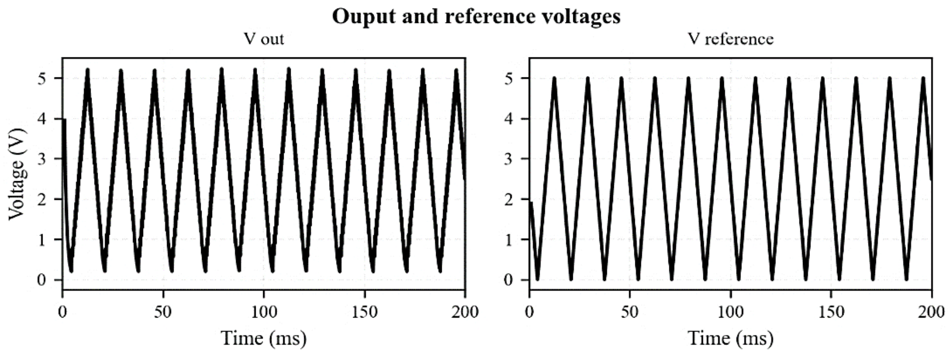

Figure 10. Time response for triangular V_{ref} behavior at 5 V amplitude and 60 Hz frequency

3.3. Tracking rectangular references

For 50% duty rectangular references at 1 Hz and 60 Hz (5 V peak), the 60 Hz case reveals observable transients at edges due to the capacitor's discharge/charge dynamics when subjected to abrupt steps, whereas the 1 Hz case masks this effect because the discharge completes rapidly relative to the period, as shown in Figures 11-14. Transient overshoots seen in simulation up to 2 p.u. at rising edges are attributed to numerical artifacts given the absence of a corresponding experimental signature and the independence from excitation frequency; the measured behavior indicates physically plausible bounded transitions.

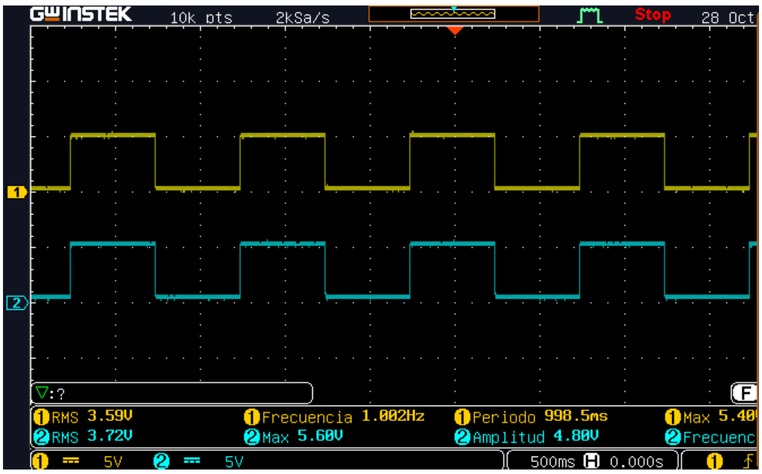

Figure 11. Time response for rectangular 50% V_{ref} behavior at 5 V amplitude and 1 Hz frequency

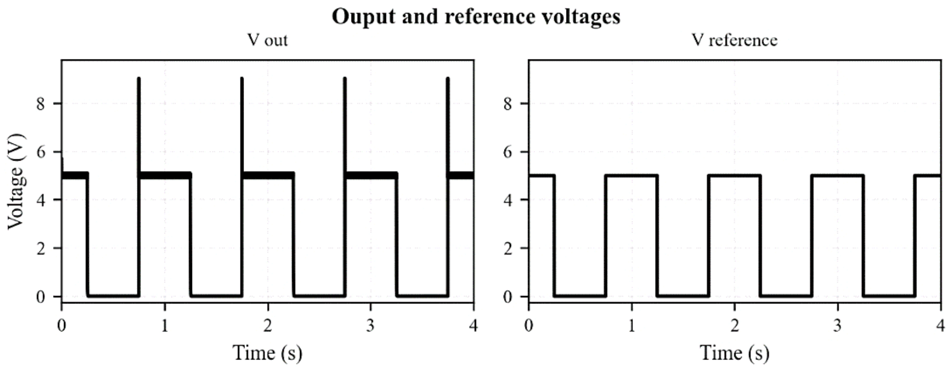

Figure 12. Time response for rectangular 50% V_{ref} behavior at 5 V amplitude and 1 Hz frequency

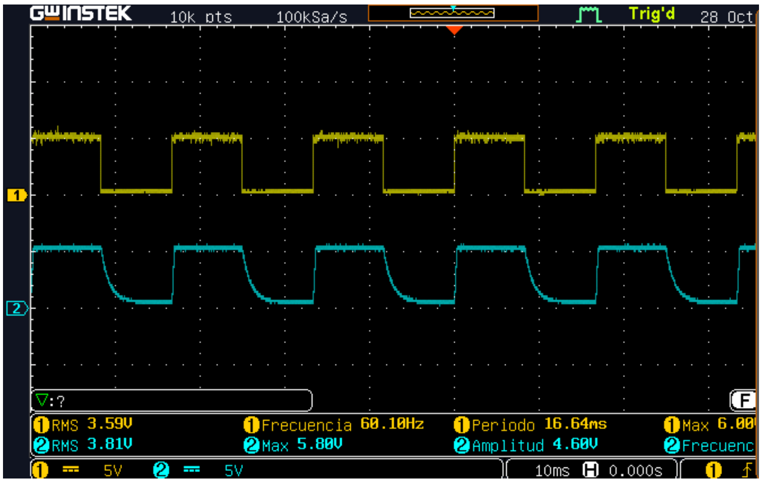

Figure 13. Time response for rectangular 50% V_{ref} behavior at 5 V amplitude and 60 Hz frequency

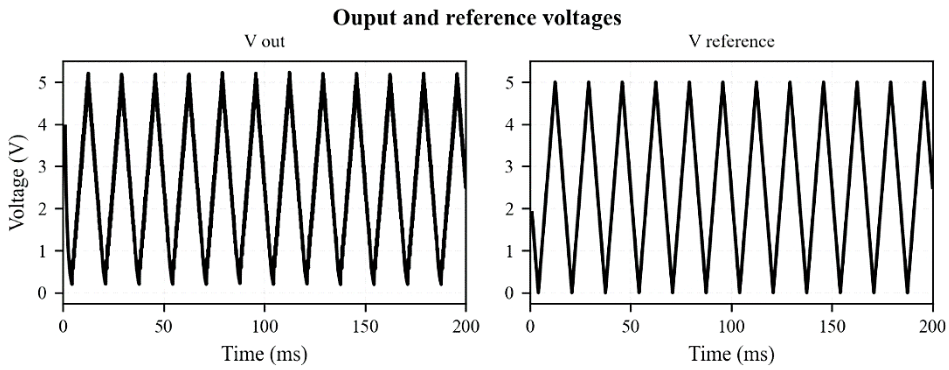

Figure 14. Time response for rectangular 50% V_{ref} behavior at 5 V amplitude and 60 Hz frequency

3.4. System's behavior against perturbations

Under a programmed reduction from 20 V, the output follows the sinusoidal 1 Hz 5 V reference until the input headroom approaches the reference peak; beyond this point, the natural dropout prevents reaching the crest, yet the waveform shape is preserved, as shown in Figure 15. With a sinusoidal V_{ref}, adding and removing a parallel load produces expected variations in load voltage magnitude and ripple due to the load's voltage-dependent resistance; regulation remains stable and promptly settles after each perturbation, as shown in Figure 16. Real-time changes of V_{ref} among rectangular, triangular, and sinusoidal classes at 1 Hz are accommodated with fast adaptation and without loss of stability, demonstrating the controller's robustness to abrupt command changes, as shown in Figure 17.

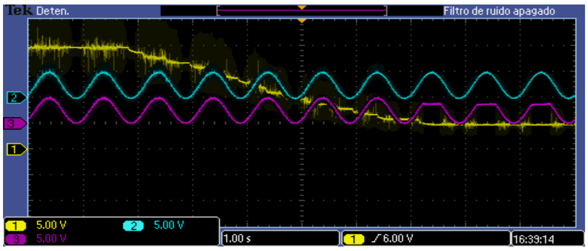

Figure 15. Time response of the system when a voltage drop occurs

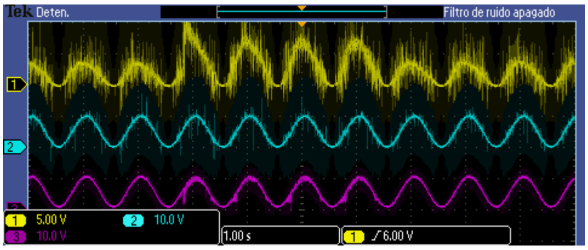

Figure 16. Time response of the system when a load perturbation occurs

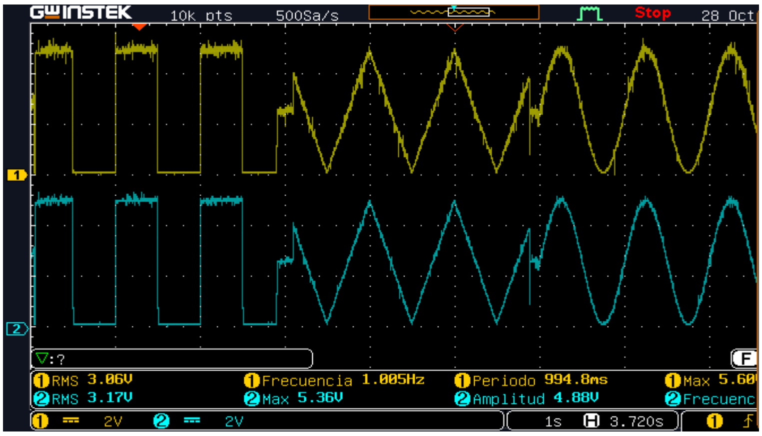

Figure 17. Time response of the system when reference waveform changes

3.5. Interpretation and implications of results

Across all waveforms, the analogue on–off loop delivers envelope tracking with small ripple and rapid transients, reaffirming the efficacy of a low-complexity, isolated comparator–opto architecture for dynamic voltage shaping from a DC source. Edge-sensitive cases (rectangular at 60 Hz) highlight the expected capacitor-induced transients, suggesting that if tighter edge fidelity is required, minor design refinements such as hysteresis band tuning, output RC shaping, or modest digital assistance could further reduce step-induced deviations without sacrificing simplicity.

4. CONCLUSION

The experimental results demonstrate that a low-complexity, opto-isolated on-off controller achieves high-fidelity dynamic tracking and robust DC regulation, supporting the claim that sophisticated digital control is not always necessary for high-performance voltage shaping. The study validated the prototype's ability to track sinusoidal, triangular, and rectangular references at grid frequencies (60 Hz) with fast transient response and minimal ripple, even under disturbances such as input voltage drops and load perturbations. These outcomes align with the theoretical expectations of boundary-based control and support standard power electronics theories regarding output-capacitor dynamics, confirming that observed step transients remain physically bounded and predictable. By successfully emulating AC-like behaviors with minimal hardware, this research moves the body of scientific knowledge forward by providing an empirical benchmark for high-speed, low-cost analogue regulation that rivals the dynamic tracking performance of more complex robust-control strategies. Consequently, this architecture offers a viable design path for cost-sensitive applications requiring both efficiency and precise dynamic signal tracking.

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AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

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David Estrada Grisales	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓			
José Ángel Buitrago Gutiérrez	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓			
Fredy E. Hoyos	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

The authors declare no conflict of interest.

INFORMED CONSENT

We have obtained informed consent from all individuals included in this study.

DATA AVAILABILITY

The datasets that support the findings of this study are available from the corresponding author upon request.

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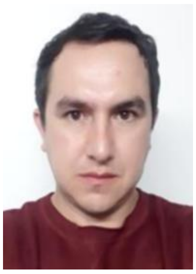

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