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Enhancing SAPF performance with VOC and SVM for electrical networks depollution

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ABSTRACT

This paper presents a significant enhancement in the filtering performance of shunt active power filters (SAPF) by leveraging the voltage oriented control (VOC) in combination with a three-level NPC inverter using space vector modulation (SVM). The VOC technique enables precise control of the SAPF by utilizing the orientation of the voltages, thereby optimizing harmonic compensation and reference tracking. Incorporating a three-level inverter allows for more refined voltage modulation, resulting in a substantial reduction in injected harmonic content. Simulation results from MATLAB/Simulink demonstrate the effectiveness of this approach. Before compensation, the measured total harmonic distortion (THD) reaches 27.98%, exceeding the IEEE 519-1992 standard threshold of 5%. However, after applying the SAPF, the THD drops to 0.85%, aligning with international standards for power quality. The figures included in the study illustrate the stability of the phase-locked loop (PLL) voltages and the noticeable improvement in the source current waveforms, which exhibit a near-sinusoidal profile after filtering. These findings validate the superiority of the VOC strategy coupled with an NPC inverter and SVM in effectively mitigating harmonic distortions and enhancing power quality in modern electrical networks.

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1. INTRODUCTION

Power electronics has rapidly evolved in recent decades, driven by major progress in semiconductor technology and control design. These advances have enabled its integration into a wide range of systems such as motor drives, electric traction, and harmonic mitigation. Consequently, power converters are now fundamental across all voltage and power levels. The growing use of nonlinear devices, particularly diode or thyristor rectifiers, has however introduced significant power quality concerns. Harmonic distortion, reactive power flow, and neutral current imbalance often occur in three-phase systems [1].

A variety of active filter configurations have been studied in the literature to address power quality issues in electrical grids. Among these, SAPFs are particularly effective in mitigating current harmonics in medium-to-low-power applications. Active filtering provides rapid dynamic response, making it ideal for loads with fluctuating demands [2]. Moreover, active filters can compensate for reactive power and stabilize load conditions, delivering a comprehensive solution for power quality management [3].

Conventional voltage-oriented control (VOC) strategies for shunt active power filters (SAPF) have limitations that can be overcome by incorporating three-level SVM. Unlike conventional two-level space vector modulation (SVM), the three-level SVM enhances the voltage waveform synthesis, leading to lower output voltage distortion and improved switching performance [4]. In VOC-SVM, the inverter voltage states are calculated based on a space vector approach to ensure reduced harmonic distortion and a constant switching frequency [5].

The present work proposes improvements to the conventional VOC-SAPF by: i) Developing a robust SVM for the three-level NPC inverter, ii) Embedding a robust PLL based on a BPMVF, iii) Integrating an anti-windup PI controller to stabilize the DC-bus voltage. Simulation results validate the efficiency of the proposed control. The SAPF successfully decreases the THD of the source current from 27.98% to 0.85%, demonstrating total compliance with IEEE 519-1992 standards. Furthermore, the filter achieves a near-unit power factor and a fast dynamic response during load disturbances [6], [7].

2. ROBUST PLL WITH BPMVF AND DC-BUS VOLTAGE REGULATION

2.1. Conventional PLL

A PLL is essential for extracting the grid phase angle and angular frequency. It comprises a phase detector, loop filter (usually PI), and voltage-controlled oscillator [8], [9]. The source voltages are defined as (1).

$$\begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} = \sqrt{2} v_{s_{rms}} \begin{bmatrix} \cos\theta \\ \cos(\theta - 2\pi/3) \\ \cos(\theta + 2\pi/3) \end{bmatrix} \tag{1}$$

After Clarke–Park transformations (2).

$$\begin{bmatrix} v_{sd} \\ v_{sq} \end{bmatrix} = \begin{bmatrix} \cos\hat{\theta} & \sin\hat{\theta} \\ -\sin\hat{\theta} & \cos\hat{\theta} \end{bmatrix} \begin{bmatrix} v_{s\alpha} \\ v_{s\beta} \end{bmatrix} \tag{2}$$

When synchronization is achieved, v_{sq}=0, and the estimated frequency is (3).

$$\hat{\omega}_s = (K_{pp} + \frac{K_{ip}}{s})(\hat{\theta} - \theta) \tag{3}$$

This leads to a second-order dynamic model (4)

$$F(s) = \frac{\omega_n^2 + 2\zeta\omega_n s}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{4}$$

Where K_{pp}=$\frac{2\zeta\omega_n}{\sqrt{3}v_{s_{rms}}}$ and τ_{ip}=$\frac{2\zeta}{\omega_n}$.

2.2. PLL enhancement by BPMVF

To strengthen robustness under voltage imbalance and disturbances, a BPMVF is incorporated into the PLL [10]. Its dynamics are expressed as (5).

$$\begin{cases} \hat{v}_{s_\alpha} = \dfrac{K_c}{s}(v_{s_\alpha} - \hat{v}_{s_\alpha}) - \dfrac{\omega_c}{s}\hat{v}_{s_\beta} \\ \hat{v}_{s_\beta} = \dfrac{K_c}{s}(v_{s_\beta} - \hat{v}_{s_\beta}) + \dfrac{\omega_c}{s}\hat{v}_{s_\alpha} \end{cases} \tag{5}$$

Where K_c and ω_c represent the filter gains. This approach improves phase tracking accuracy and significantly enhances system immunity to harmonics and DC offsets [11].

2.3. DC-bus voltage control with anti-windup

The DC-link voltage must remain stable to ensure correct power exchange between the grid and converter [12], [13]. The capacitor behavior is (6).

$$i_{dc} = C_{dc}\frac{dv_{dc}}{dt} \tag{6}$$

The instantaneous power balance between DC and AC sides is (7).

$$v_{dc}^{*} i_{dc} = \frac{3}{2}(v_{sd} i_{sd} + v_{sq} i_{sq}) \tag{7}$$

Combining both expressions yields (8).

$$\frac{v_{dc}(s)}{i_{sd}(s)} = \frac{3 v_{s_{rms}}}{\sqrt{2} v_{dc}^{*} C_{dc} s} \tag{8}$$

The regulator transfer function is (9).

$$G_{v_{dc}} = \frac{K_{pv} s + K_{iv}}{K s^2 + K_{pv} s + K_{iv}} \tag{9}$$

Anti-windup compensation is introduced by feeding back the saturation error through a gain f_a=$\frac{1}{T_a}$ (T_a=0.001s), preventing integrator accumulation and ensuring fast, stable recovery [14], [15].

3. PRINCIPLE OF VOC

VOC transforms three-phase currents into the rotating dq frame for decoupled regulation [16]. The dynamic model of the line-side converter is (10).

$$u_{ld} = R_s i_{ld} + L\frac{di_{ld}}{dt} + u_{sd} - \omega L i_{lq}, \quad u_{lq} = R_s i_{lq} + L\frac{di_{lq}}{dt} + u_{sq} + \omega L i_{ld} \tag{10}$$

Assuming $R_s \approx 0$, the simplified decoupled control laws are:

$$u_{ld} = \omega L i_{lq} + u_{sd} + \Delta u_{sd}, \quad u_{lq} = -\omega L i_{ld} + \Delta u_{sq} \tag{11}$$

where:

$$\Delta u_{sd} = K_{pi}(i_{sd}^{*} - i_{sd}) + K_{ii}\int (i_{sd}^{*} - i_{sd})dt, \quad \Delta u_{sq} = K_{pi}(i_{sq}^{*} - i_{sq}) + K_{ii}\int (i_{sq}^{*} - i_{sq})dt \tag{12}$$

The outputs are transformed back to the inverse dq frame and processed by the SVM to generate switching signals, ensuring stable harmonic mitigation and reactive power compensation [17].

4. THREE-LEVEL SVM ALGORITHM

4.1. Structure of the three-level NPC converter

A three-level NPC converter includes twelve switches and six clamping diodes. Two series-connected capacitors form the DC-link, each charged to half of V_{dc} [18]. Each phase leg includes four switches (S_{a1}-S_{a4}) and two clamping diodes (D_{a1}-D_{a2}). The diodes maintain the midpoint potential and ensure voltage sharing between capacitors [19]. Depending on the switching combination, the phase terminal can be connected to $\frac{V_{dc}}{2}$, 0, or -$\frac{V_{dc}}{2}$, as illustrated in Figure 1.

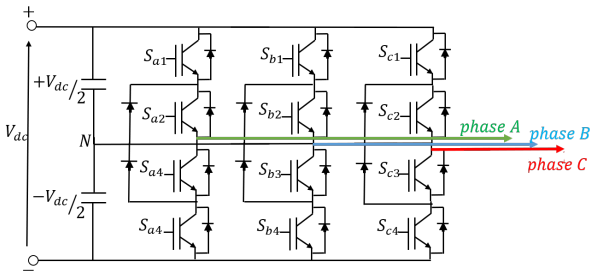


Figure 1. Topology of a three-level NPC converter

The output voltages can be expressed in either phase-to-neutral or line-to-line form, e.g., V_{ab}=V_a-V_b. Maintaining charge balance between the two DC-link capacitors is critical for stable operation, and SVM plays a central role in this balancing process. The neutral point N established by the capacitors divides V_{dc} into two equal parts. In practice, small voltage deviations may occur due to unequal switching sequences; proper selection of redundant vectors helps restore balance [20].

4.2. Principle of SVM

SVM offers better DC-link utilization, lower current ripple, and reduced harmonic distortion compared with sinusoidal PWM [21]. It is widely adopted in multilevel topologies despite the increased number of switching states [22], [23]. The general switching states for one phase are summarized in Table 1. The SVM scheme is illustrated in Figure 2, where each hexagonal region corresponds to possible switching combinations.

Table 1. Switching states in a three-level NPC converter

Output level	Gate signals		State
	S_{a1}	S_{a2}	Symbol
$+\frac{V_{dc}}{2}$	1	1	$(+)$
0	0	1	(0)
$-\frac{V_{dc}}{2}$	1	0	$(-)$

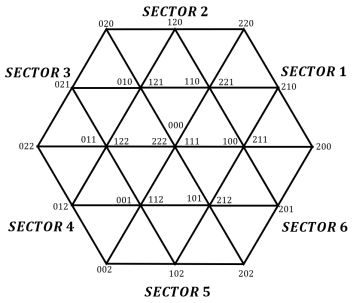


Figure 2. Space vector diagram for a three-level NPC inverter

In a balanced three-phase system, the sum of phase voltages equals zero:

$$V_a + V_b + V_c = 0 \tag{13}$$

and the phase voltages are:

$$V_a = V_m \sin(\omega t), \quad V_b = V_m \sin(\omega t - \frac{2\pi}{3}), \quad V_c = V_m \sin(\omega t + \frac{2\pi}{3}) \tag{14}$$

These sinusoidal quantities form a rotating voltage vector whose magnitude and position determine the inverter output. The complex representation of this vector in the stationary reference frame is:

$$V_{\text{ref}} = \frac{2}{3}(V_a + aV_b + a^2V_c), \quad a = e^{j\frac{2\pi}{3}} \tag{15}$$

Its modulus and angular position are:

$$|V_{\text{ref}}| = \sqrt{V_\alpha^2 + V_\beta^2}, \quad \theta_s = \tan^{-1}\left(\frac{V_\beta}{V_\alpha}\right) \tag{16}$$

where the Clarke transformation yields:

$$V_\alpha = \frac{2}{3}\left(V_a - \frac{1}{2}V_b - \frac{1}{2}V_c\right), \quad V_\beta = \frac{2}{3}\left(\frac{\sqrt{3}}{2}V_b - \frac{\sqrt{3}}{2}V_c\right) \tag{17}$$

The inverter synthesizes the desired voltage vector within each switching period by adjusting the dwell times of selected vectors [24]. This ensures nearly sinusoidal line voltages, minimized switching stress, and effective neutral-point balancing-key requirements for high-performance power converters [25].

5. RESULTS AND DISCUSSION

A complete simulation model has been developed using the parameters detailed in Table 2. The objective is to evaluate the performance of the proposed VOC combined with SVM when applied to the SAPF. Figure 3 shows the complete MATLAB/Simulink model of the proposed solution.

Table 2. System parameters: nonlinear load, source, and SAPF components

Component	Parameter	Value
Nonlinear load	Load inductor	1 mH
	Load resistor	30 Ω
	Rectifier inductor	0.566 mH
	Rectifier resistor	0.01 Ω
Source	Frequency	50 Hz
	Internal resistor	0.1 Ω
	RMS voltage	220 V
	Internal inductor	0.1 mH
SAPF	Reference voltage	600 V
	Filter inductor	1 mH
	Bus capacitor	1100 μF
Simulation environment	Resolution method	Euler (ode1)
	Step type	Fixed step
	Sampling time	1 μs

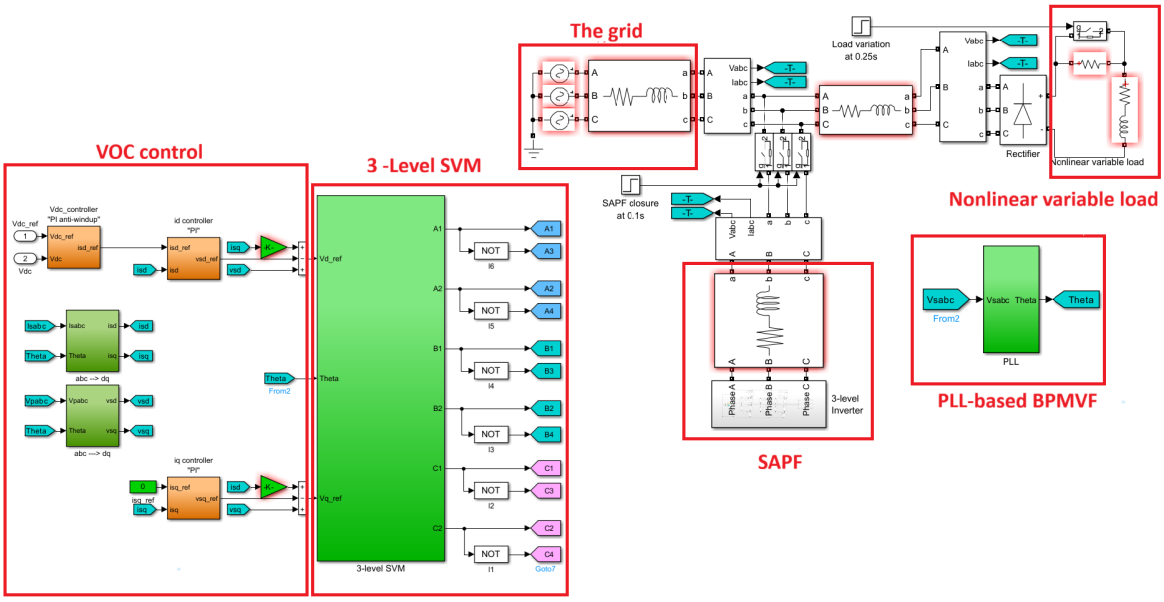


Figure 3. Overall MATLAB/Simulink schematic of the proposed VOC–SVM-based SAPF using a three-level NPC inverter and a BPMVF-based PLL under a nonlinear variable load

The grid currents and voltages are measured and processed by the BPMVF-based PLL to extract the grid angle θ required for the abc-dq transformations in the VOC strategy. The VOC controller generates the reference compensation currents and voltage references, which are synthesized by the three-level SVM to produce the gate signals of the NPC inverter. The SAPF then injects compensating currents at the PCC to mitigate harmonics drawn by the nonlinear variable load and to achieve near-unity power factor.

Initially, the effectiveness of the filter is assessed through Fourier analysis of the current waveforms, along with a comparison of their THD values. Subsequently, the control's robustness and stability are evaluated during the connection of the SAPF. At t=0.1s, the filter is activated, and a variation in the load resistance from 30 Ω to 15 Ω is introduced. The DC-link capacitor is initially charged to 500 V.

Source voltage: Figure 4(a) presents the measured source voltages both before and after the activation of the SAPF. As observed, the voltage waveforms retain a balanced and sinusoidal nature, with minimal distortion or phase asymmetry. This consistency confirms the inherent stability of the supply network and validates the efficiency of the SAPF in maintaining power quality. Furthermore, the undisturbed waveforms ensure reliable synchronization conditions, which are critical for the proper operation of grid-connected systems.

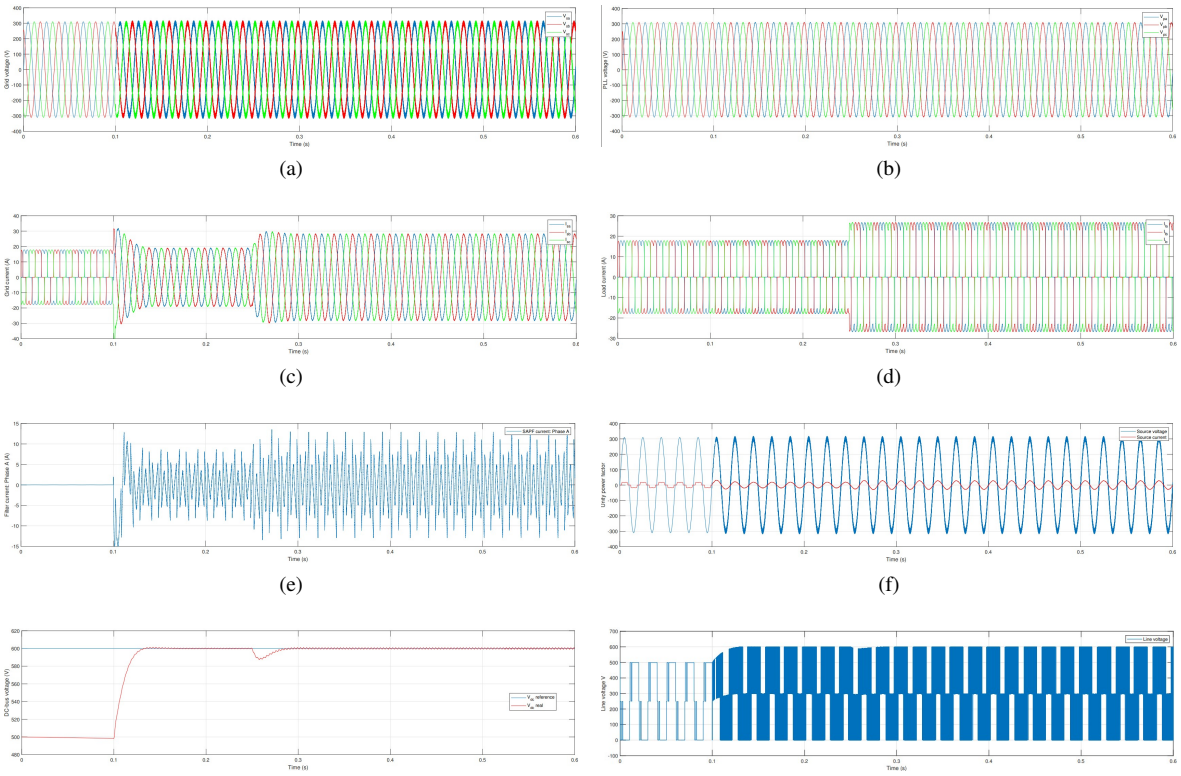


Figure 4. Dynamic performance of the proposed VOC–SVM-based three-level NPC inverter under nonlinear load: (a) source voltage, (b) PLL input voltage, (c) source current, (d) load current, (e) SAPF current, (f) source voltage and current alignment (unity power factor), (g) DC-link voltage response, and (h) line voltage

PLL-based BPMVF: Figure 4(b) displays the input voltages of the PLL under both pre- and post-activation conditions of the active filter. As evidenced by the waveform, the PLL input remains stable and unaffected after the filter is engaged, demonstrating the robustness of the proposed PLL architecture. The structure, which incorporates a BPMVF, effectively preserves synchronization with the grid even in the presence of harmonic distortions and other grid disturbances. This resilience confirms the PLL's ability to reject noise and maintain accurate phase tracking, ensuring reliable operation in distorted grid environments.

Source current: Figure 4(c) depicts the source current under nonlinear load operation. Before compensation ($t<0.1$ s), the waveform is strongly distorted and departs from the ideal sinusoid due to harmonic-rich load currents. After the SAPF is switched on at t=0.1 s, the source current is rapidly reshaped into an almost sinusoidal waveform. This confirms that the proposed SAPF control effectively compensates the load-generated harmonics and maintains power quality during demanding operating conditions.

Load current: Figure 4(d) illustrates the load current waveform, which exhibits pronounced nonlinearity and oscillatory dynamics–a hallmark of rectifier-based loads such as diode or thyristor bridges. These loads introduce harmonic distortion and irregular current fluctuations due to their discontinuous conduction patterns. The observed distortion–particularly low-order harmonics and high-frequency noise–can lead to: i) voltage waveform degradation in the grid, ii) increased losses in distribution systems, iii) interference with sensitive equipment. This behavior strongly justifies the implementation of active power filtering, which dynamically injects compensating currents to cancel harmonics and reactive power, ensuring compliance with power quality standards.

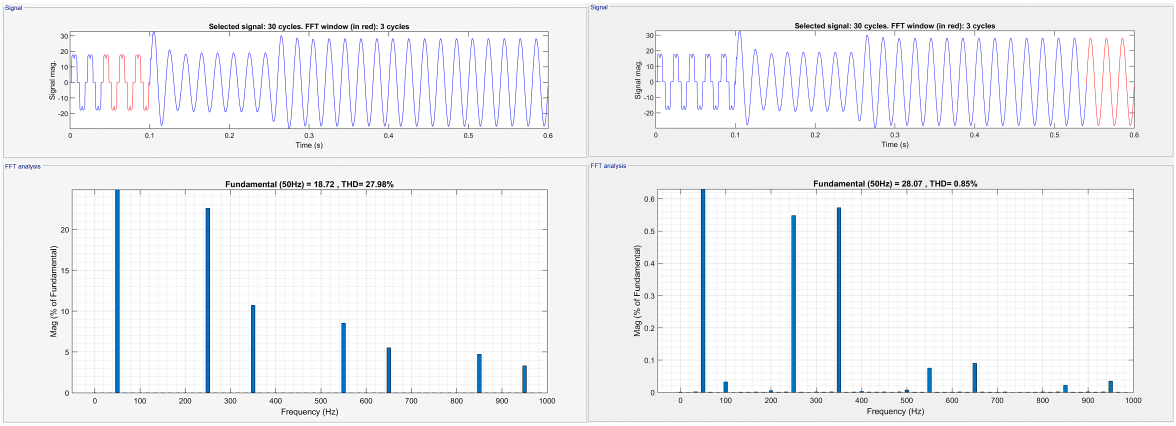
Filter current: As illustrated in Figure 4(e), the SAPF rapidly injects compensating currents immediately upon activation. The waveform clearly demonstrates that the SAPF dynamically generates inverse harmonic components, effectively canceling out the distortion produced by the nonlinear load. This compensation ensures improved power quality by mitigating harmonic pollution.

Unitary power factor: As demonstrated in Figure 4(f), the source voltage and current waveforms exhibit precise alignment after compensation. Once the SAPF is applied, both signals become perfectly synchronized in phase, confirming that the system attains a near-unity power factor.

DC-bus voltage: Figure 4(g) shows the transient response of the DC-bus voltage control. Starting from its initial value, it quickly reaches the reference of 600 V. The response exhibits a short settling time with negligible overshoot, indicating a well-damped behavior. This confirms the effectiveness of the anti-windup PI regulator in preventing integrator windup and ensuring stable converter operation under load variations.

The SVM technique optimizes switching states, enhancing voltage balance across DC-link capacitors while maintaining high efficiency. This results in a smoother line voltage with lower THD, making it ideal for grid-connected power quality applications, as shown in Figure 4(h).

THD Amelioration: Figure 5 compares the spectra of the source current after and before filtering, i) Before filtering THD=27.98%, indicating a high harmonic distortion level. ii) After filtering THD=0.85%, demonstrating a drastic reduction in harmonic distortion, achieving full compliance with the IEEE 519-1992 standard.



(a) (b)

Figure 5. Three-phase source current waveform of the proposed system and THD comparison of the source current (a) before SAPF activation and (b) after SAPF activation (THD reduced from 27.98% to 0.85%)

6. CONCLUSION

This paper has proposed a comprehensive approach to enhancing the performance of a SAPF through the integration of VOC and a three-level SVM scheme. The primary objective was to improve harmonic compensation, ensure dynamic stability, and optimize the power quality in electrical networks subjected to nonlinear loads. A key contribution of this work lies in the adoption of a three-level inverter topology, which offers finer voltage resolution compared to conventional two-level structures. This enhancement enables more accurate synthesis of the reference voltage vectors, reducing output ripple and switching losses. In conjunction with the VOC strategy, the system achieves precise current tracking and effective decoupling of active and reactive components. Another critical element introduced is a robust PLL based on a BPMVF, capable of maintaining synchronization even under significant waveform distortion. Additionally, a PI controller augmented with an anti-windup mechanism was implemented to regulate the DC-bus voltage and improve the overall stability of the control loop. Simulation results validate the efficiency of the proposed VOC-SVM. The SAPF successfully reduces the THD of the source current from 27.98% to 0.85%, demonstrating full compliance with IEEE 519-1992 standards. Furthermore, the filter achieves a near-unit power factor and a fast dynamic response during load disturbances.

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AUTHOR CONTRIBUTIONS STATEMENT

This manuscript adopts the Contributor Roles Taxonomy (CRediT) to clearly identify the roles of each author, promote transparency, and prevent disputes regarding authorship.

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Yassine Zahraoui	✓		✓	✓		✓			✓		✓		✓	

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal Analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject Administration
Fu : **Fu**nding Acquisition

CONFLICT OF INTEREST STATEMENT

All authors affirm that there are no conflicts of interest related to the content or publication of this work.

DATA AVAILABILITY

No new datasets were created or analyzed in the course of this research; as such, data availability does not apply.

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