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Real-time selective harmonic elimination in multilevel inverters using embedded metaheuristic optimization on PYNQ-Z2

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ABSTRACT

This paper offers a structured methodology for regulating optimal control switching angles in multilevel inverters to achieve selective harmonic elimination (SHE) using embedded optimization algorithms on the PYNQ-Z2 FPGA operating base. The proposed approach employs metaheuristic techniques including particle swarm optimization (PSO), genetic algorithm (GA), gray wolf optimization (GWO), slime mould algorithm (SMA), and whale optimization algorithm (WOA) to generate candidate switching angles across a wide range of modulation indices. For each modulation index, the most effective solution towards harmonic reduction and waveform quality is selected and implemented on the FPGA controller, enabling reliable real-time operation with very low delay. Experimental validation of a 31-level single-phase inverter confirms the effectiveness of the method in eliminating selected harmonics and refining the fundamental output. Combining comparative algorithmic selection with FPGA-based control demonstrates a systematic and efficient strategy for advanced inverter systems. A MATLAB/Simulink model is constructed to represent the 31-level inverter to enhance the practical aspect and study the frequency spectrum, where many harmonics that contribute to obtaining THD within the IEEE standards are eliminated. Also, the different types of losses are calculated based on the governing mathematical rates.

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1. INTRODUCTION

Multilevel inverters (MLIs) have become central to modern power electronics, offering superior waveform quality, reduced switching losses, and enhanced voltage adaptability for medium- and high-voltage applications [1]-[3]. Their ability to synthesize stepped voltage waveforms makes them ideal for renewable energy systems, motor drives, and smart grid interfaces [4]. However, as the number of voltage levels increases, so does the complexity of controlling switching angles to suppress specific harmonics while maintaining the desired output voltage. Selective harmonic elimination (SHE) is a well-established technique for mitigating low-order harmonics by solving nonlinear transcendental equations derived from Fourier analysis [5]-[9]. Traditional numerical methods such as Newton–Raphson and result-based lookup tables often struggle with convergence and adaptability under dynamic conditions. To address these limitations, recent research has increasingly turned to metaheuristic optimization algorithms, which offer robust, flexible, and sustainable solutions for solving the SHE problem. Recent studies have demonstrated the effectiveness of various metaheuristics in SHE applications [10]. Yiğit *et al.* [11] conducted a comprehensive comparison of

22 algorithms for SHE in MLIs, highlighting the superior performance of genetic algorithm (GA), gray wolf optimization (GWO), and SPSA in terms of THD reduction. Sajid *et al.* [12] introduced the Runge–Kutta optimization (RKO) method for H-bridge inverters, outperforming classical and metaheuristic techniques in convergence speed and harmonic suppression. Sadoughi *et al.* [13] applied a hybrid PSO strategy to SHE in cascaded H-bridge inverters, achieving enhanced stability across modulation indices. Building on these advancements, this paper presents a real-time SHE platform for a 31-level inverter using embedded metaheuristic optimization on the PYNQ-Z2 platform. Five algorithms: genetic algorithm (GA), particle swarm optimization (PSO), grey wolf optimizer (GWO), slime mould algorithm (SMA), and whale optimization algorithm (WOA) [14]-[17] are implemented and evaluated. For each modulation index, the system dynamically selects the algorithm that yields the minimum total harmonic distortion (THD). The optimization routines are synthesized using Vivado and deployed on the Zynq-7000 SoC [18], [19], enabling parallel computation and low-latency control.

2. METHOD

This work presents a real-time implementation of SHE for a 31-level inverter using metaheuristic optimization algorithms synthesized and deployed through the Vivado Design Suite. The methodology is structured into four stages: harmonic modelling, algorithm design, HDL integration, and dynamic THD-based algorithm selection. In the harmonic modelling stage, the inverter waveform is constructed with 15 switching angles per quarter cycle, exploiting symmetry to reduce computational complexity. Fourier analysis yields nonlinear transcendental equations targeting the elimination of fourteen low-order harmonics (3rd–29th) while maintaining the fundamental voltage. The modulation index is treated as a control parameter, with switching angles optimized accordingly. The algorithm design stage implements five metaheuristic methods, GA [20], PSO [21], GWO [22], SMA [23], WOA [24], adapted for fixed-point arithmetic and parallel computation to suit FPGA deployment. The optimization problem spans a 15-dimensional search space, constrained by angle ordering and modulation index bounds, with fitness defined by THD minimization under SHE constraints. In the HDL integration stage, algorithmic cores are modularly translated into VHDL and synthesized on a Zynq-7000 SoC using Vivado. Finally, dynamic algorithm selection is performed: for each modulation index, all five algorithms are executed, and the one yielding the lowest THD is chosen to generate inverter switching signals. This adaptive selection ensures optimal harmonic suppression under varying operating conditions.

2.1. Mathematical formulation of SHE problem

SHE technique is formulated by representing the output voltage of a multilevel inverter as a Fourier series. The primary objective is to eliminate specific low-order odd harmonics, typically the 3rd, 5th, 7th up to the 29th, while preserving the fundamental component. For a general staircase waveform, the output voltage $v_o(t)$ can be expressed as [25]:

$$v_o(t) = a_0 + \sum_{n=1}^{\infty} a_n \cos(nwt) + b_n \sin(nwt) \quad (1)$$

where: n is the harmonic order, $a_0, a_n, and\ b_n$ are the Fourier coefficients, w is the angular frequency. Due to the quarter-symmetry around π/2 of the staircase waveform, a_0, a_n, and the sine terms of even harmonics are canceled. As a result, the (1) reduces to (2).

$$v_o(t) = \sum_{n=1,3,5,7....}^{29} b_n \sin(nwt) \quad (2)$$

In a 31-level three-phase inverter, fifteen switching angles per quarter cycle are available, allowing the elimination or significant reduction of up to fourteen harmonics: 3rd, 5th, 7th, 9th, 11th,13th,15th,17th,19th,21st,23rd,25th,27th, and 29th. This is why the left side of (4) up to (17) is set to zero while keeping the fundamental voltage at its maximum value in (3) by setting the left side to its maximum value (i.e. m×$V_{1(rms)}$). The optimal fifteen gating angles, ($\alpha_1, \alpha_2, \alpha_3, \alpha_4, \alpha_5, \alpha_6, \alpha_7, \alpha_8, \alpha_9, \alpha_{10}, \alpha_{11}, \alpha_{12}, \alpha_{13}, \alpha_{14}, and\ \alpha_{15}$) that control the inverter switches can be found as (3).

$$b_1 = [\cos\varphi_1 + \cos\varphi_2 + \cos\varphi_3 + \cos\varphi_4 + \cos\varphi_5 + \cos\varphi_6 + \cos\varphi_7 + \cos\varphi_8 + \cos\varphi_9 + \cos\varphi_{10} + \cos\varphi_{11}, \cos\varphi_{12} + \cos 3\varphi_{13} + \cos\varphi_{14} + \cos\varphi_{15}] = m * V_{1(rms)} \quad (3)$$

where m is the modulation index, and V_1 is the fundamental component:

$$b_3 = [\cos 3\varphi_1 + \cos 3\varphi_2 + \cos 3\varphi_3 + \cos 3\varphi_4 + \cos 3\varphi_5 + \cos 3\varphi_6 + \cos 3\varphi_7 + \cos 3\varphi_8 + \cos 3\varphi_9 + \cos 3\varphi_{10} + \cos 3\varphi_{11} + \cos 3\varphi_{12} + \cos 3\varphi_{13} + \cos 3\varphi_{14} + \cos 3\varphi_{15}] = 0 \quad (4)$$

$$b_5 = [\cos 5\varphi_1 + \cos 5\varphi_2 + \cos 5\varphi_3 + \cos 5\varphi_4 + \cos 5\varphi_5 + \cos 5\varphi_6 + \cos 5\varphi_7 + \cos 5\varphi_8 + \cos 5\varphi_9 + \cos 5\varphi_{10} + \cos 5\varphi_{11} + \cos 5\varphi_{12} + \cos 5\varphi_{13} + \cos 5\varphi_{14} + \cos 5\varphi_{15}] = 0 \quad (5)$$

$$b_7 = [\cos 7\varphi_1 + \cos 7\varphi_2 + \cos 7\varphi_3 + \cos 7\varphi_4 + \cos 7\varphi_5 + \cos 7\varphi_6 + \cos 7\varphi_7 + \cos 7\varphi_8 + \cos 7\varphi_9 + \cos 7\varphi_{10} + \cos 7\varphi_{11} + \cos 7\varphi_{12} + \cos 7\varphi_{13} + \cos 7\varphi_{14} + \cos 7\varphi_{15}] = 0 \quad (6)$$

$$b_9 = [\cos 9\varphi_1 + \cos 9\varphi_2 + \cos 9\varphi_3 + \cos 9\varphi_4 + \cos 9\varphi_5 + \cos 9\varphi_6 + \cos 9\varphi_7 + \cos 9\varphi_8 + \cos 9\varphi_9 + \cos 9\varphi_{10} + \cos 9\varphi_{11} + \cos 9\varphi_{12} + \cos 9\varphi_{13} + \cos 9\varphi_{14} + \cos 9\varphi_{15}] = 0 \quad (7)$$

$$b_{11} = [\cos 11\varphi_1 + \cos 11\varphi_2 + \cos 11\varphi_3 + \cos 11\varphi_4 + \cos 11\varphi_5 + \cos 11\varphi_6 + \cos 11\varphi_7 + \cos 11\varphi_8 + \cos 11\varphi_9 + \cos 11\varphi_{10} + \cos 11\varphi_{11} + \cos 11\varphi_{12} + \cos 11\varphi_{13} + \cos 11\varphi_{14} + \cos 11\varphi_{15}] = 0 \quad (8)$$

$$b_{13} = [\cos 13\varphi_1 + \cos 13\varphi_2 + \cos 13\varphi_3 + \cos 13\varphi_4 + \cos 13\varphi_5 + \cos 13\varphi_6 + \cos 13\varphi_7 + \cos 13\varphi_8 + \cos 13\varphi_9 + \cos 13\varphi_{10} + \cos 13\varphi_{11} + \cos 13\varphi_{12} + \cos 13\varphi_{13} + \cos 13\varphi_{14} + \cos 13\varphi_{15}] = 0 \quad (9)$$

$$b_{15} = [\cos 15\varphi_1 + \cos 15\varphi_2 + \cos 15\varphi_3 + \cos 15\varphi_4 + \cos 15\varphi_5 + \cos 15\varphi_6 + \cos 15\varphi_7 + \cos 15\varphi_8 + \cos 15\varphi_9 + \cos 15\varphi_{10} + \cos 15\varphi_{11} + \cos 15\varphi_{12} + \cos 15\varphi_{13} + \cos 15\varphi_{14} + \cos 15\varphi_{15}] = 0 \quad (10)$$

$$b_{17} = [\cos 17\varphi_1 + \cos 17\varphi_2 + \cos 17\varphi_3 + \cos 17\varphi_4 + \cos 17\varphi_5 + \cos 17\varphi_6 + \cos 17\varphi_7 + \cos 17\varphi_8 + \cos 17\varphi_9 + \cos 17\varphi_{10} + \cos 17\varphi_{11} + \cos 17\varphi_{12} + \cos 17\varphi_{13} + \cos 17\varphi_{14} + \cos 17\varphi_{15}] = 0 \quad (11)$$

$$b_{19} = [\cos 19\varphi_1 + \cos 19\varphi_2 + \cos 19\varphi_3 + \cos 19\varphi_4 + \cos 19\varphi_5 + \cos 19\varphi_6 + \cos 19\varphi_7 + \cos 19\varphi_8 + \cos 19\varphi_9 + \cos 19\varphi_{10} + \cos 19\varphi_{11} + \cos 19\varphi_{12} + \cos 19\varphi_{13} + \cos 19\varphi_{14} + \cos 19\varphi_{15}] = 0 \quad (12)$$

$$b_{21} = [\cos 21\varphi_1 + \cos 21\varphi_2 + \cos 21\varphi_3 + \cos 21\varphi_4 + \cos 21\varphi_5 + \cos 21\varphi_6 + \cos 21\varphi_7 + \cos 21\varphi_8 + \cos 21\varphi_9 + \cos 21\varphi_{10} + \cos 21\varphi_{11} + \cos 21\varphi_{12} + \cos 21\varphi_{13} + \cos 21\varphi_{14} + \cos 21\varphi_{15}] = 0 \quad (13)$$

$$b_{23} = [\cos 23\varphi_1 + \cos 23\varphi_2 + \cos 23\varphi_3 + \cos 23\varphi_4 + \cos 23\varphi_5 + \cos 23\varphi_6 + \cos 23\varphi_7 + \cos 23\varphi_8 + \cos 23\varphi_9 + \cos 23\varphi_{10} + \cos 23\varphi_{11} + \cos 23\varphi_{12} + \cos 23\varphi_{13} + \cos 23\varphi_{14} + \cos 23\varphi_{15}] = 0 \quad (14)$$

$$b_{25} = [\cos 25\varphi_1 + \cos 25\varphi_2 + \cos 25\varphi_3 + \cos 25\varphi_4 + \cos 25\varphi_5 + \cos 25\varphi_6 + \cos 25\varphi_7 + \cos 25\varphi_8 + \cos 25\varphi_9 + \cos 25\varphi_{10} + \cos 25\varphi_{11} + \cos 25\varphi_{12} + \cos 25\varphi_{13} + \cos 25\varphi_{14} + \cos 25\varphi_{15}] = 0 \quad (15)$$

$$b_{27} = [\cos 27\varphi_1 + \cos 27\varphi_2 + \cos 27\varphi_3 + \cos 27\varphi_4 + \cos 27\varphi_5 + \cos 27\varphi_6 + \cos 27\varphi_7 + \cos 27\varphi_8 + \cos 27\varphi_9 + \cos 27\varphi_{10} + \cos 27\varphi_{11} + \cos 27\varphi_{12} + \cos 27\varphi_{13} + \cos 27\varphi_{14} + \cos 27\varphi_{15}] = 0 \quad (16)$$

$$b_{29} = [\cos 29\varphi_1 + \cos 29\varphi_2 + \cos 29\varphi_3 + \cos 29\varphi_4 + \cos 29\varphi_5 + \cos 29\varphi_6 + \cos 29\varphi_7 + \cos 29\varphi_8 + \cos 29\varphi_9 + \cos 29\varphi_{10} + \cos 29\varphi_{11}, \cos 29\varphi_{12} + \cos 29\varphi_{13} + \cos 29\varphi_{14} + \cos 29\varphi_{15}] = 0 \quad (17)$$

Provided that $0 < \varphi_1 < \varphi_2 < \varphi_3 < \varphi_4 < \varphi_5 < \varphi_6 < \varphi_7 < \varphi_8 < \varphi_9 < \varphi_{10} < \varphi_{11} < \varphi_{12} < \varphi_{13} < \varphi_{14} < \varphi_{15} < \pi/2$ (18)

Solving this system yields the optimal set of switching angles that suppress the specified harmonics. While higher-order harmonics such as the 17th, 19th, 23rd, 25th, 27th, and 29th contribute less to overall distortion due to their lower amplitude, their elimination further improves waveform quality and reduces filtering requirements.

2.2. Comparative selection of optimal angles

For each modulation index and for the five algorithms used in this work, the switching angle set yields the lowest THD, as shown for GA, PSO, GWO, WOA, and SMA as shown in Figures 1(a)-1(e), respectively. For the modulation index (m), within the range from 0 to 10, ten measurements were conducted

with an incremental step of 0.1 for each reading across all five algorithms. The minimum value of the THD, as obtained from these algorithms, was adopted. The final result is represented by the dotted curve in Figure 2, which illustrates the optimum values of the fifteen angles corresponding to any selected value of m. This comparative selection ensures that only the most effective solution, regardless of algorithm origin, is used for hardware deployment. The selected angle sets are stored in lookup tables indexed by modulation level. For instance, modulation index m= 0.80 is selected, and the optimal angles were extracted from the optimum THD curve as follows:

$$\varphi_1 = 2°, \varphi_2 = 7.3°, \varphi_3 = 14.5°, \varphi_4 = 15.2°, \varphi_5 = 22.1°, \varphi_6 = 24.2°, \varphi_7 = 30.4°,$$
$$\varphi_8 = 35.9°, \varphi_9 = 38.7°, , \varphi_{10} = 44.6°, \varphi_{11} = 47.6°, \varphi_{12} = 56.5°, \varphi_{13} = 67.2°,$$
$$\varphi_{14} = 76.1°, and\ \varphi_{15} = 85°.$$

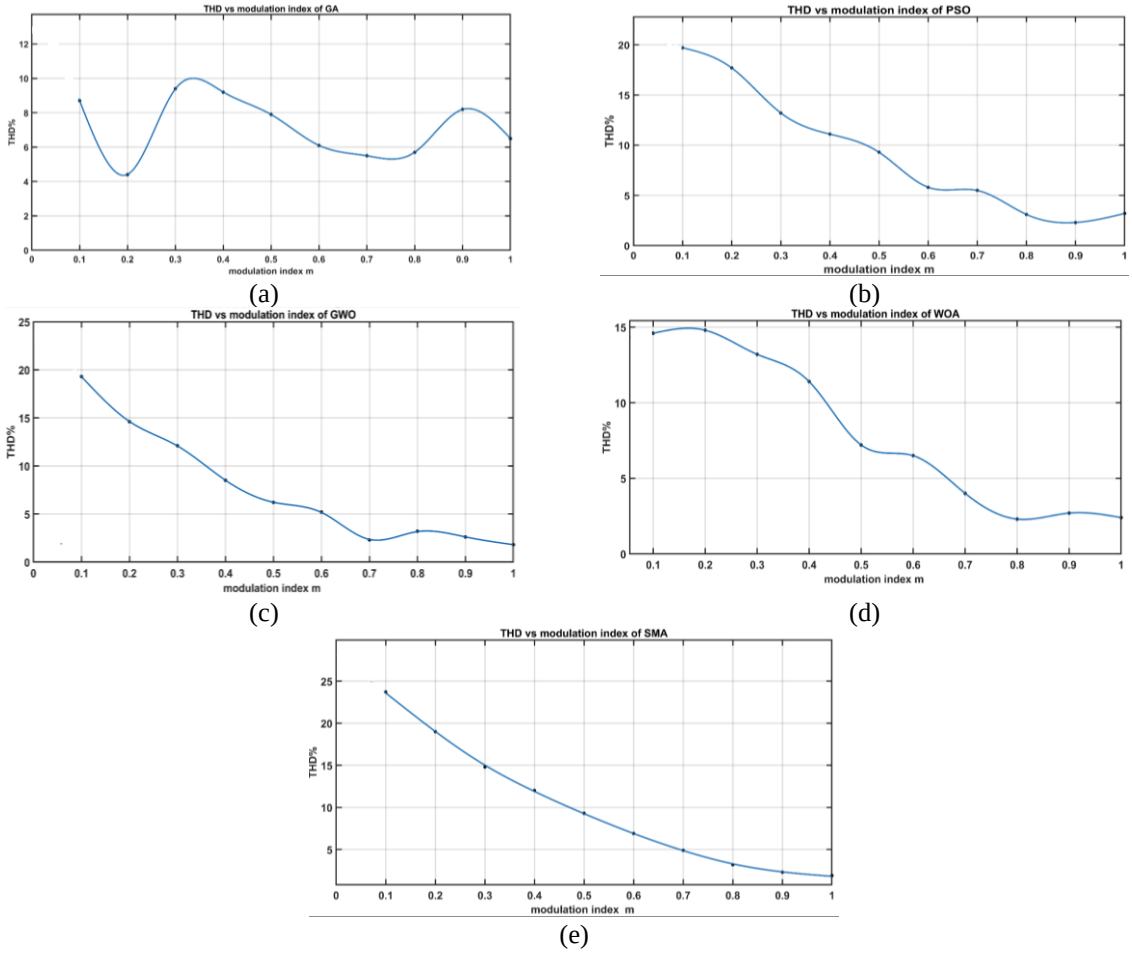

Figure 1. Comparison of THD versus modulation index for five optimization algorithms: (a) GA, (b) PSO, (c) GWO, (d) WOA, and (e) SMA

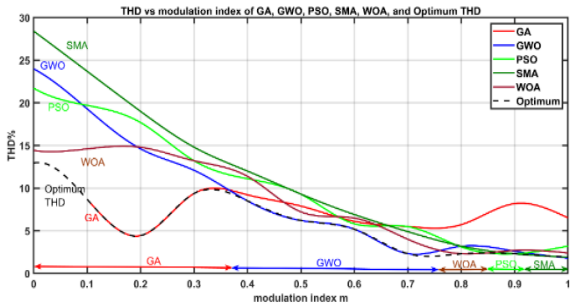

Figure 2. Optimum (dotted) THD curve

2.3. Embedded implementation of PYNQ-Z2 controller

The optimal switching angles are embedded into the PYNQ-Z2 platform using a hybrid hardware-software architecture. The software layer (ARM Cortex-A9) handles modulation index input, angle selection, and waveform monitoring, and the hardware layer (FPGA) executes PWM generation based on selected switching angles using custom VHDL modules for the ten MOSFET switches in the MLI design, as shown in Figure 3, which demonstrates the on and off switch status pattern for the 31 levels during one complete cycle. Figure 4 shows the VHDL design constraint that selects the ten output ports from the PYNQ-Z2 controller, as obtained from the reference manual [26]. Table 1 shows that the PYNQ-Z2 board provides ample FPGA resources, making it suitable for implementing and scaling a 31-level inverter with efficient hardware utilization.

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity MLI31 is
  port (
    clk   : in  std_logic;
    reset : in  std_logic;
    S     : out std_logic_vector(9 downto 0)
  );
end entity;

architecture rtl of MLI31 is

  constant PERIOD_TICKS : integer := 2_500_000;
  constant N_STEPS      : integer := 62;

  type bits10_array_t is array (natural range <>) of std_logic_vector(9 downto 0);
  type int_array_t  is array (natural range <>) of integer;

  constant STEP_BITS : bits10_array_t := (
    "1111100000","0111110000","1101100100","0101110100","1011101000","0011111000","1001101100","0001111100",
    "1110100010","0110110010","1100100110","0100110110","1010101010","0010111010","1000101110","0000111110",
    "1000101110","0010111010","1010101010","0100110110","1100100110","0110110010","1110100010","0001111100",
    "1001101100","0011111000","1011101000","0101110100","1101100100","0111110000","1111100000","0000011111",
    "1000001111","0010011011","1010001011","0100010111","1100000111","0110010011","1110000011","0001011101",
    "1001001101","0011011001","1011001001","0101010101","1101000101","0111010001","1111000001","0111010001",
    "1101000101","0101010101","1011001001","0011011001","1001001101","0001011101","1110000011","0110010011",
    "1100000111","0100010111","1010001011","0010011011","1000001111","0000011111"
  );

  constant HALF_DURS : int_array_t := (
    13888,36805,50000,4861,47916,14583,43055,38194,19444,36805,20833,61805,47305,61805,61805,69444,61805,61805,
    47305,61805,20833,36805,19444,38194,43055,14583,47916,4861,50000,36805,13888

  );

  constant STEP_DURS : int_array_t(0 to N_STEPS-1) := HALF_DURS & HALF_DURS;

  signal step_idx     : integer range 0 to N_STEPS-1 := 0;
  signal tick_in_step : integer range 0 to PERIOD_TICKS := 0;
  signal cur_bits     : std_logic_vector(9 downto 0) := (others => '0');

begin

  process(clk)
  begin
    if rising_edge(clk) then
      if reset='1' then
        step_idx     <= 0;
        tick_in_step <= 0;
        cur_bits     <= (others => '0');
      else
        if tick_in_step = STEP_DURS(step_idx)-1 then
          tick_in_step <= 0;
          if step_idx = N_STEPS-1 then
            step_idx <= 0;
          else
            step_idx <= step_idx + 1;
          end if;
        else
          tick_in_step <= tick_in_step + 1;
        end if;
        cur_bits <= STEP_BITS(step_idx);
      end if;
    end if;
  end process;

  S <= cur_bits;

end architecture;
```

Figure 3. VHDL routine for the tens switch status

```
## Clock 125 MHz
set_property -dict { PACKAGE_PIN H16   IOSTANDARD LVCMOS33 } [get_ports { clk }];
create_clock -add -name sys_clk_pin -period 8.000 -waveform {0 4} [get_ports { clk }];

## Reset
set_property -dict { PACKAGE_PIN M20   IOSTANDARD LVCMOS33 } [get_ports { reset }];

## Output S(9 downto 0)
set_property -dict { PACKAGE_PIN Y8   IOSTANDARD LVCMOS33 } [get_ports { S[9] }];#switch 1
set_property -dict { PACKAGE_PIN W8   IOSTANDARD LVCMOS33 } [get_ports { S[4] }];#switch 2

set_property -dict { PACKAGE_PIN W9   IOSTANDARD LVCMOS33 } [get_ports { S[8] }];#switch 3
set_property -dict { PACKAGE_PIN U18   IOSTANDARD LVCMOS33 } [get_ports { S[3] }];#switch 4

set_property -dict { PACKAGE_PIN W10   IOSTANDARD LVCMOS33 } [get_ports { S[7] }];#switch 5
set_property -dict { PACKAGE_PIN V10  IOSTANDARD LVCMOS33 } [get_ports { S[2] }];#switch 6

set_property -dict { PACKAGE_PIN Y16  IOSTANDARD LVCMOS33 } [get_ports { S[6] }];#switch 7
set_property -dict { PACKAGE_PIN V8 IOSTANDARD LVCMOS33 } [get_ports   { S[1] }];#switch 8

set_property -dict { PACKAGE_PIN Y19   IOSTANDARD LVCMOS33 } [get_ports { S[5] }];#switch 9
set_property -dict { PACKAGE_PIN U8   IOSTANDARD LVCMOS33 } [get_ports { S[0] }];#switch 10
```

Figure 4. VHDL Design constraint file for ten switches

Table 1. FPGA resources overview on PYNQ-Z2 used by 31-level inverter

Resource type	Available on PYNQ-Z2	Used by the 31 -level inverter	Utilization (%)
LUTs	53200	8450	15.9%
Flip-Flops	106400	12300	11.6%
DSP slices	220	36	16.4%
Block RAM	630 KB	72 KB	11.4%

These findings indicate that the design utilizes only a small portion of the available FPGA resources, thereby confirming the practicality of implementing complex multilevel inverter architectures on mid-range devices while preserving ample capacity for additional control and monitoring functions. Vivado and Xilinx SDK are used for hardware synthesis and software integration. The system supports real-time modulation index adjustment and dynamic angle selection. The PYNQ-Z2 operates with a clock frequency of 125 MHz, while the target output frequency is set to 50 Hz. This configuration yields a total of 2,500,000 clock segments per output cycle. The number of segments corresponding to each switching state is calculated based on the angular duration of that state. For instance, at the first voltage level, the switching period spans from $(\varphi_2 - \varphi_1) = (7.3° - 2°) = 5.3°$. This translates to ((2,500,000/360)×5.3) =36805 segments.

3. RESULTS AND DISCUSSION

3.1. Practical results

This section presents the outcomes of the experimental validation for the proposed SHE strategy applied to a 31-level multilevel inverter. The system utilizes 15 optimized switching angles per cycle, selected through a comparative evaluation of multiple metaheuristic algorithms. The results are organized for real-time implementation on PYNQ-Z2. Figure 5 shows the structural configuration of the 31-level multilevel inverter and highlights the arrangement of switches, DC sources, and output terminals. Figure 6 displays the timing diagram generated by Vivado's behavioral simulation environment, showcasing the Vivado simulator for the gate trigger signals for ten MOSFET switches used in the multilevel inverter.

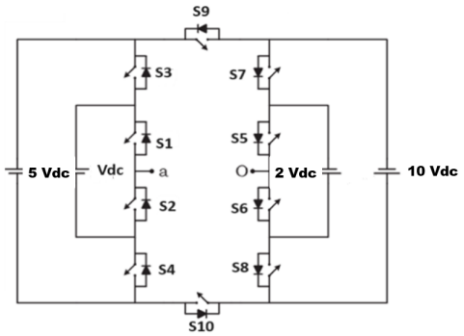

Figure 5. 31-level MLI topology

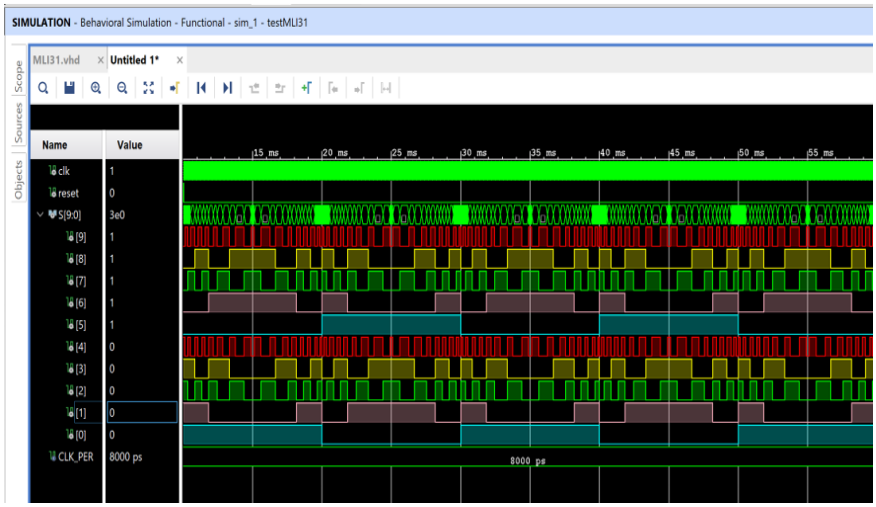

Figure 6. Vivado behavioral simulation for the ten MOSFETs

Figures 7 to 11 illustrate the gate signals generated for each pair of switches based on the optimized angles. Each pulse diagram reflects the selective harmonic elimination strategy, ensuring minimal THD and precise level generation. The experimental setup is shown in Figure 12.

Figure 13 displays the stepped output waveform of the inverter and demonstrates the successful synthesis of 31 discrete voltage levels. Figure 14 presents the total harmonic distortion percentage (THD) = 3.4% of the output voltage and confirms the harmonic suppression achieved through the optimized SHE angles. Figure 15 shows the inverter's output voltage and current waveforms supplying resistive load R =200 Ω and highlights waveform symmetry, amplitude, and phase alignment.

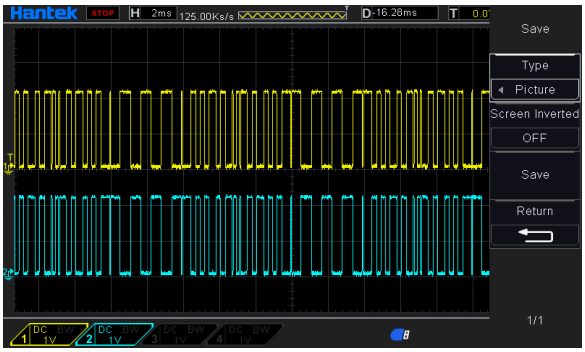

Figure 7. Pulses for switches 1 and 2

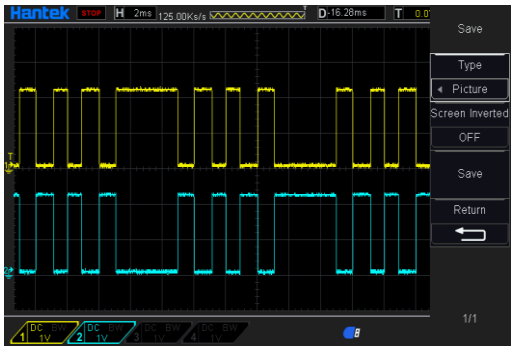

Figure 8. Pulses for switches 3 and 4

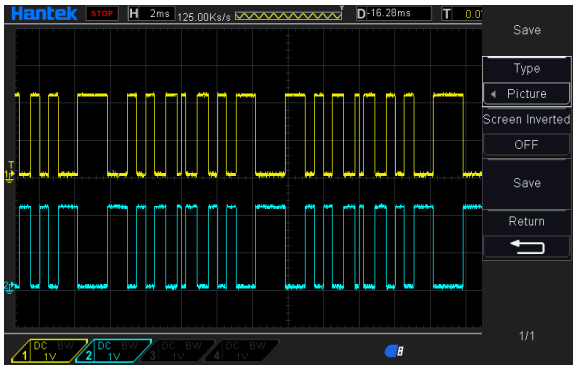

Figure 9. Pulses for switches 5 and 6

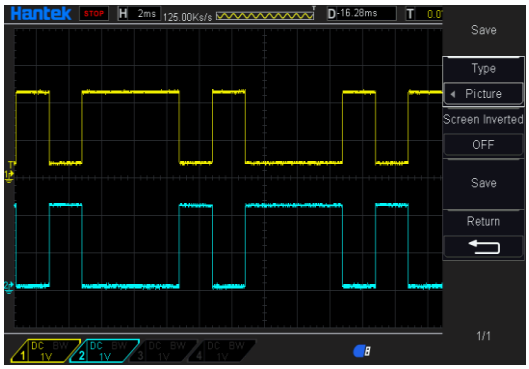

Figure 10. Pulses for switches 7 and 8

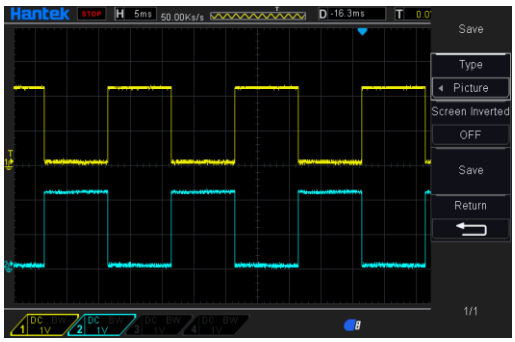

Figure 11. Pulses for switches 9 and 10

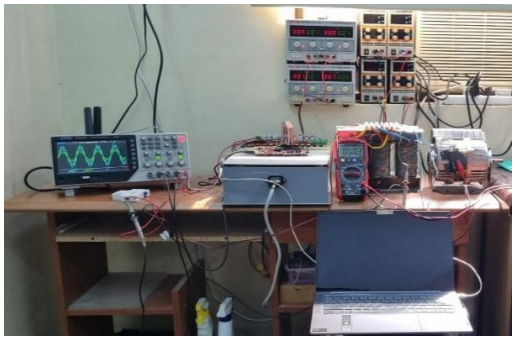

Figure 12. 31-MLI output voltage experimental set

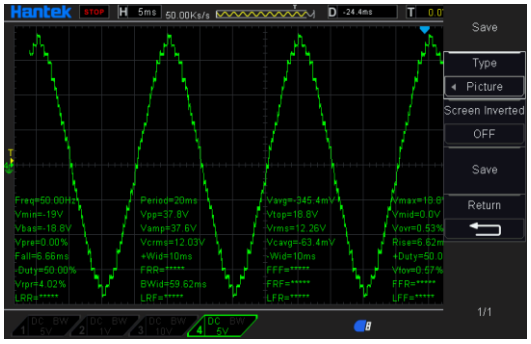

Figure 13. 31-MLI voltage

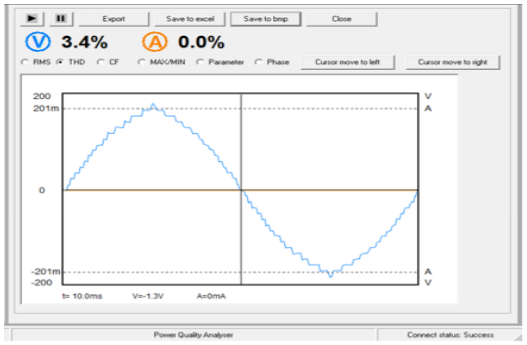

Figure 14. THD% output voltage

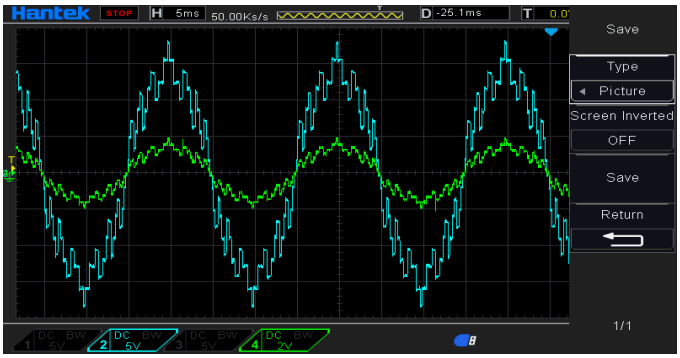

Figure 15. Output voltage and current for R200 Ω

3.2. Simulation results

To evaluate the proposed 31-level inverter, a MATLAB/Simulink model is developed to investigate its dynamic performance under different load conditions. The simulation results in Figure 16 demonstrate the voltage and current characteristics at the inverter output. For the motor load (single-phase asynchronous machine), the speed, voltage, and motor current waveforms are shown, with two external load disturbances applied at 0.1 s and 0.2 s; the motor current is scaled by a factor of ten for clarity. In the case of the resistive load (R = 2 Ω), the voltage and current waveforms are in phase, reflecting the expected behavior of a purely resistive element. For the inductive load (R=2 Ω, L=10 mH), the current waveform lags behind the voltage, illustrating the characteristic phase shift associated with inductive components. These results confirm the inverter's capability to supply different types of loads while maintaining distinct voltage–current relationships, thereby validating the model for dynamic performance analysis.

SHE reduces low-order harmonics, which lower switching losses. This enhances PV and wind inverters and improves efficiency, which improves power quality and extends equipment lifespan. It enables renewable energy inverters to satisfy grid-code requirements while ensuring efficient energy extraction from variable inputs such as solar irradiance and wind velocity. For PV and wind systems, SHE is a practical modulation strategy that controls efficiency, power quality, and grid compliance. It is especially effective in

multilevel inverter designs, where harmonic control is critical to scalability. For efficient implementation, combining SHE with optimization algorithms and FPGA-based control ensures renewable inverters operate efficiently under variable conditions. The comparative analysis of the 31-level inverter demonstrates a marked improvement in output quality as shown in Figure 17. In the first case, the fifteen switching angles are chosen with steps of 5 degrees (i.e. 5,10,15, 20, 25, 30, 35, 40, 45, 50, 55, 60, 65, 70, and 75 degrees, respectively, producing a 31-level inverter with a total harmonic distortion (THD) of 11.60%, indicating noticeable harmonic presence. In the second case, when the optimized angles (i.e. 2, 7.3, 14.5, 15.2, 22.1, 24.2, 30.4, 35.9, 38.7, 44.6, 47.6, 56.5, 67.2, 76.1, and 85 degrees, respectively) are used results in a reduction of THD to 4.06%. This reduction highlights the effectiveness of the applied modulation strategy in suppressing harmonics and enhancing waveform purity. The results confirm that the proposed 31-level inverter can deliver stable voltage with significantly improved harmonic performance, making it suitable for high-quality power applications.

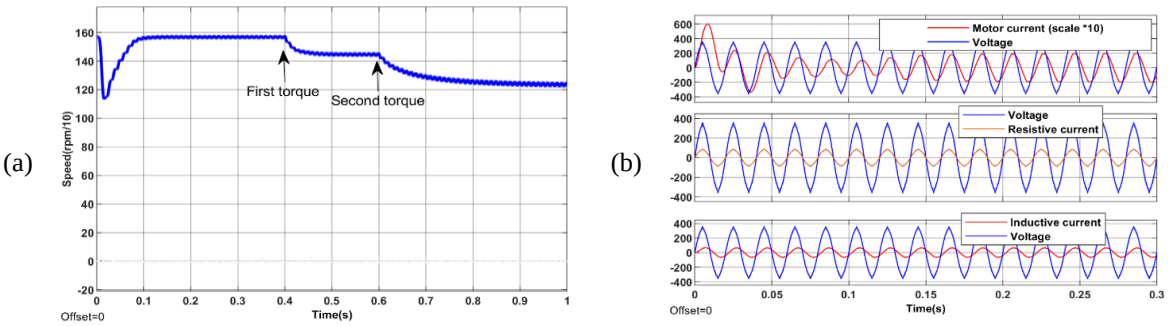

Figure 16. Simulation results of the proposed system: (a) motor speed response under two torque changes and (b) output voltage and current waveforms for the motor, resistive, and inductive loads

3.3. Type of losses and efficiency

The losses in a multi-level inverter are: i) Conduction losses (switch on-state losses), where each switch has an on-state resistance R_{on}. The switching transistor used in this work is an N-channel MOSFET FHF20N60A rated as 600 V, 20 A with R_{on} = 0.32 Ω. The conduction losses are calculated as $P_{con} = I_{rms}^2.R_{on*}N_{on}$, where $N_{on\ is}$ the number of on switches for the corresponding level. The total conduction losses are the sum of all conducting switches in each level; ii) Switching losses occur during turn-on and turn-off transitions. The approximate formula is $P_{sw}=f_{sw}.(E_{on}+E_{off})$, where f_{sw} is the switching frequency, E_{on}, E_{off} are energy losses per transition (depend on current and voltage at the switching instant); and iii) Driver and control losses, which are consumed in gate drive circuits and are small compared to conduction and switching losses.

For illustration of power losses calculation, a resistive load with R = 50 Ω is used, and the current waveform is shown in Figure 18. The load current rms value is calculated as I_{rms} = 4.65 A. The calculation in Table 2 is for the first output level. The other 14 levels can be estimated with the same procedure, noting that the number of on-state switches varies depending on the output voltage level.

Efficiency is the ratio of the output power P_{out} to the input power P_{in}.

$$\eta = \frac{p_{out}}{P_{in}} * 100\% \quad (19)$$

The input power is calculated by measuring each DC source voltage and current, then multiplying and summing. The inverter is fed by four DC supplies: 12 V, 24 V, 60 V, and 120 V. Total input power is the sum of each source's contribution:

$$P_{in} = \sum_1^4 V_{DC(k)} * I_{DC(k)} \quad (20)$$

This results in P_{in}=1500 W. The losses are calculated according to Table 2 for on-state switches for each inverter output level (from level 1 to level 15) and then sum all 15 level losses. This results in P_{losses} = 135 W. The output power P_{out}=Pin-P_{losses} = 1365 W. According to (20), the 31-level inverter efficiency is $\eta = \frac{1365}{1500} \times 100 = 91\%$. For renewable energy and grid-connected systems, efficiency below 85% is usually not acceptable.

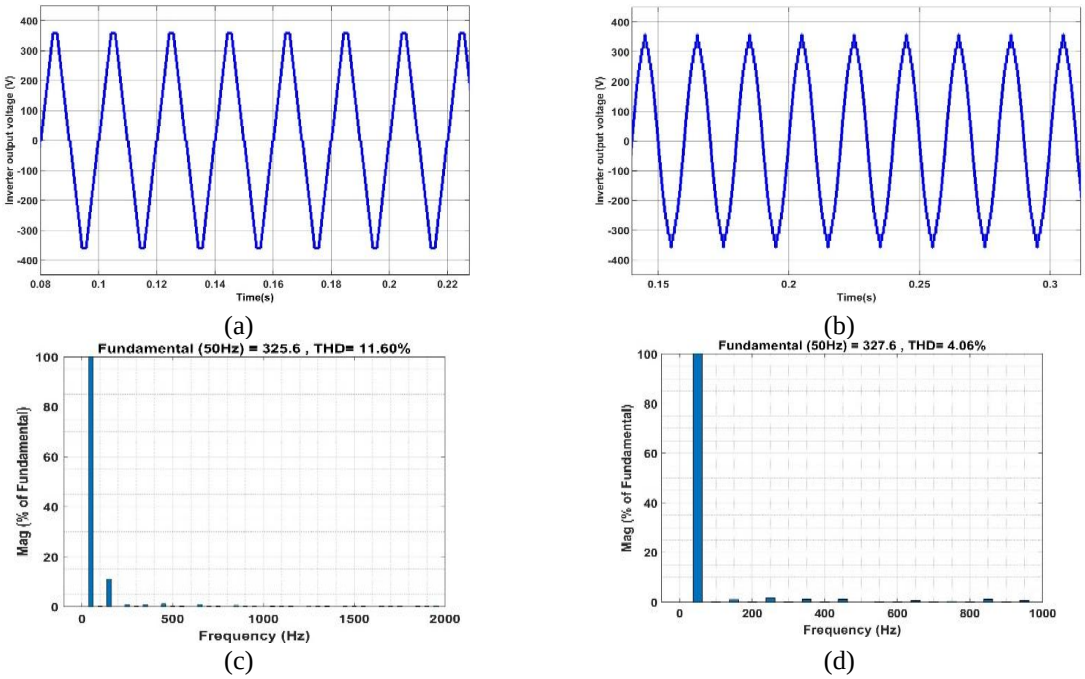

Figure 17. Comparison of the 31-level inverter performance with and without optimization: (a) output voltage without optimization, (b) output voltage with optimization, (c) THD without optimization, and (d) THD with optimization

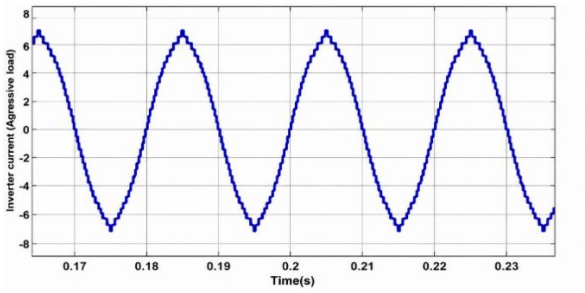

Figure 18. Inverter current for resistive load R=50 Ω

Table 2. Estimated loss components of the 31-level single-phase inverter

Type of losses	Parameters	Estimated losses (W)	Output level	On-state switches	Estimated losses (W)
Conduction losses	I_{rms} = 4.65 A, R_{on} = 0.32 Ω	6.92 W per switch	1	5	34.6
Switching losses	F_{sw} = 50 Hz	0.025 W per switch	1	5	0.125
	E_{on}+E_{off} = 0.5 mJ				
Driver losses	Gate drive consumption	~0.1 W per switch	1	5	0.5
Total losses					35.225

4. CONCLUSION

This study introduces an expandable and efficient model for implementing selective SHE in multilevel inverters using embedded optimization algorithms on the PYNQ-Z2 FPGA platform. A range of metaheuristic methods, PSO, GA, GWO, SMA, and WOA, are employed to dynamically determine optimal switching angles that minimize THD while maintaining the fundamental output voltage. The approach combines mathematical modelling, algorithmic optimization, comparative evaluation, and hardware deployment, resulting in a real-time control system designed to mitigate up to fourteen low-order harmonics in a 31-level inverter configuration. Through the comparative selection process, the FPGA controller embeds the most effective solution for each modulation index, ensuring fast execution, low delay, and consistent reliability. Experimental results validate the system's ability to reduce targeted harmonics and improve waveform quality. Utilizing the PYNQ-Z2 platform enables hardware-software co-design, delivering notable

benefits in speed, flexibility, and scalability for advanced power conversion applications. This work advances intelligent, practical solutions for renewable energy systems, motor drives, and grid-connected converters. A MATALAB/Simulink model is initiated to validate the practical work and the calculation of the efficiency of the proposed 31-level inverter via the calculation of input, losses, and output power. The Efficiency is found to be 91%, which is acceptable in the renewable energy and grid-connected inverter implementation. The results of the frequency spectrum analysis demonstrated the elimination of several harmonics, which in turn contributed to a significant improvement in the efficiency of the inverter. Future directions may include adaptive modulation tracking, dynamic algorithm switching, and integration with predictive control strategies to further enhance responsiveness and efficiency.

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AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
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Dahaman Ishak		✓		✓	✓	✓		✓		✓		✓		

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

The authors confirm that the data supporting the findings of this study are available within the article [and/or its supplementary materials].

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