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Hardware implementation of low-frequency selective harmonic elimination on multilevel inverter

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ABSTRACT

Multilevel inverters (MLIs) are widely used in medium- and high-power applications due to their improved output waveform quality and reduced voltage stress on semiconductor switches. However, low-order harmonics remain a significant challenge, particularly when low switching frequencies are employed. This research presents the hardware implementation of low-frequency selective harmonic elimination (SHE) for a multilevel inverter to improve output power quality while reducing switching losses. The nonlinear SHE equations are solved to determine appropriate switching angles for eliminating selected low-order harmonics while maintaining the required fundamental voltage. The obtained switching angles are implemented using a digital controller and gate-drive circuit, and the performance is validated through simulation and experimental hardware results. The simulation results achieve an overall total harmonic distortion (THD) of 17.23%, while the experimental prototype records a THD of 18.39%, showing a close correspondence between the simulated and practical results. The targeted 5th-order harmonic is effectively eliminated, and the measured fundamental voltage exhibits reduced deviation from the reference value. The close agreement between simulation and experimental results confirms the effectiveness of the proposed low-frequency SHE technique for improving harmonic performance while maintaining reduced switching activity and associated switching losses.

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1. INTRODUCTION

Multilevel inverters (MLIs) have become popular power-electronic converters in power system applications because of their capacity to lessen voltage stress on semiconductor switches, decrease harmonic distortion, and increase output voltage quality [1]. Power converters that are dependable and efficient are becoming more and more necessary as renewable energy and energy storage systems turn out to be more integrated. Because MLIs provide appropriate output voltage by combining multiple lower-level direct current (DC) sources, they are especially well-suited for medium power applications [2].

Particularly in grid-connected applications, conventional two-level inverters have higher harmonic content, higher voltage stress, and more filter requirements. For the purpose of integrating renewable energy, MLI topologies and modulation techniques have been the subject of numerous studies [3]–[5]. A thorough

analysis of MLI topologies, modulation methods, and control strategies for medium-voltage applications was provided by Malinowski *et al.* [6]. Despite these benefits, adding more voltage levels necessitates more switches, capacitors, and auxiliary parts, which raises the cost and complexity of the system [7], [8]. Moreover, grid-connected systems may experience power fluctuations and issues with power quality due to the intermittent nature of renewable energy sources [9]. The total efficiency of the system is also greatly impacted by switching and conduction losses of power converters.

The most commonly used low-frequency modulation method is selective harmonic elimination pulse width modulation (SHEPWM), which can lower switching losses while removing certain low-order harmonics. However, there is relatively little emphasis on realistic hardware implementation and experimental validation of low-frequency SHEPWM in the literature currently in publication. Instead, it mostly concentrates on mathematical solution techniques, optimization algorithms, and simulation-based research. Furthermore, resolving the nonlinear selective harmonic elimination (SHE) equations and precisely applying the acquired switching angles continue to be significant practical difficulties.

The current work focuses on low-frequency SHEPWM for a multilayer inverter's hardware implementation and experimental validation in order to close this gap. The suggested method suppresses some low-order harmonics while producing precise switching pulses at low switching frequencies to lower switching losses. Simulation and experimental results demonstrate the effectiveness and practical applicability of the proposed method.

2. OPERATING PRINCIPLE OF 5-LEVEL CHB MLI

The 5-level CHB-MLI consists of two H-bridges with series connection, and each H-bridge is powered by an isolated DC source. Eight electronic switches (MOSFETs/IGBTs) are used in two H-bridge units in Figure 1. Each H-bridge is made up of four bridge-connected MOSFET/IGBT switches. The modes in which the inverter functions are as follows and are also displayed in Figure 2.

- Mode 1: +2 V_{dc} - Figure 2(a) demonstrates an V_{out} of +2 V_{dc}. All switches S1, S4, S5, S8 are ON, and remaining S3, S2, S7, S6 are OFF.
- Mode 2: +V_{dc} - Figure 2(b) displays the mode of generating +V_{dc}. Here S1, S4, S8, S6 are turned ON and S3, S4, S7, S5 are OFF.
- Mode 3: 0 V - Figure 2(c) illustrates an operating mode that produces a zero-output voltage. Here, the lower-leg switches are activated, resulting in no current flow through the power circuit.
- Mode 4: −V_{dc} - Figure 2(d) illustrates an operating mode to obtain V_{out} of −V_{dc}. The switches S3, S2, S8, S6 are ON and S1, S4, S7, S5 are OFF.
- Mode 5: -2 V_{dc} - Figure 2(e) depicts mode for obtaining V_{out} of −2 V_{dc}. The switches S3, S2, S8, and S7 are ON and S1, S4, S6, and S5 are turned OFF.

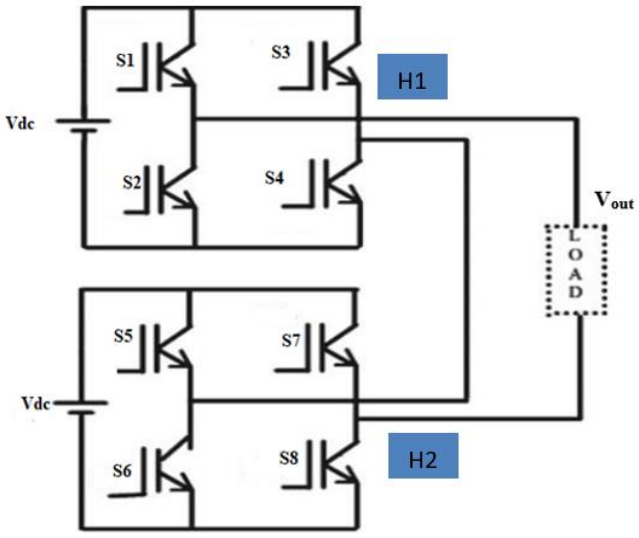

Figure 1. 1-phase five-level CHB MLI with 8 switches

Consequently, the CHB five-level inverter circuit achieves various voltage levels [10] because of the circuit's modularity, which allows for its multiplicity or redundant states. One intrinsic feature of DC link capacitors that can be utilized to redistribute losses or charge/discharge is multiplicity in the switching state. The various voltage levels with all potential multiplicities are compiled in Table 1. There is just one conceivable switching state when voltage is ±2 V_{dc}. Consequently, there is just one multiplicity and one possibility. Four multiplicities, or four switching options, are conceivable if the output voltage is ±V_{dc}. Likewise, six multiplicities are produced by zero voltage [11].

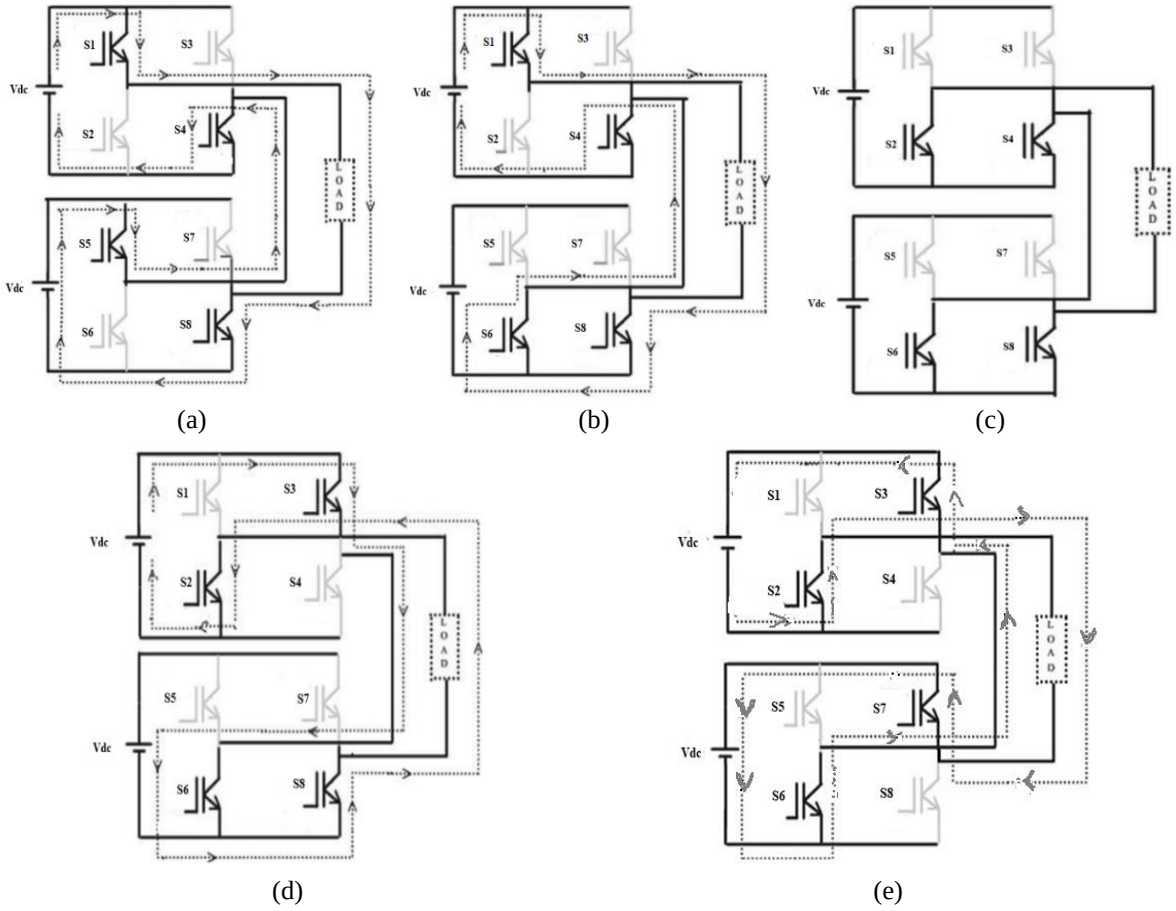

Figure 2. Inverter operating modes: (a) Mode 1 (+2 V_{dc}), (b) Mode 2 (+V_{dc}), (c) Mode 3 (0 V), (d) Mode 4 (−V_{dc}), and (e) Mode 5 (−2 V_{dc})

Table 1. Multiplicity of cascaded H-bridge five-level inverter

V_{out}	V_{H1}	V_{H2}	S1	S3	S5	S7	Multiplicity
$2V_{dc}$	(V_{dc})	(V_{dc})	High	0	High	0	1
(V_{dc})	(V_{dc})	0	High	0	0	0	4
			High	0	High	High	
	0	(V_{dc})	0	0	High	0	
			High	High	High	0	
0	0	0	High	High	0	0	6
			High	High	High	High	
			0	0	High	High	
			0	0	0	0	
	(V_{dc})	(-V_{dc})	High	0	0	High	
	(-V_{dc})	(V_{dc})	0	High	High	0	
(-V_{dc})	(-V_{dc})	0	0	High	0	0	4
			0	High	High	High	
	0	(-V_{dc})	0	0	0	High	
			High	High	0	High	
-$2V_{dc}$	(-V_{dc})	(-V_{dc})	0	High	0	High	1

3. MATHEMATICAL MODELLING OF LOW-FREQUENCY SELECTIVE HARMONIC ELIMINATION (SHE) FOR A CHBMLI

This technique uses a single output voltage cycle to carry out one or more semiconductor switch commutations. Generated waveforms are illustrated in Figure 3. Low-frequency inverters, which operate at 50 or 60 Hz, are mostly used in solar power systems and backup power systems. When it comes to powering more demanding appliances like air conditioners, refrigerators, and power tools, these inverters are the best choice [12]–[14]. In terms of electrical durability, these are the best.

It is challenging to find analytical solutions using the SHE techniques for nonlinear transcendental equations with trigonometric components. The LFSHE is an effective modulation method that takes the fundamental frequency into account. In order to remove lower harmonics and acquire the necessary set of solutions for nonlinear equations, the switching angle is determined. A nearly pure sine wave can be created by joining two H-bridges in series and using the proper modulation technique.

Fourier-series expression of the V_{out} waveform is:

$$V_{an}(\omega t) = \frac{4V_{dc}}{\pi}\sum_{n}^{\infty}(\cos(n\theta_1) + \cos(n\theta_2) + \cdots + \cos(n\theta_5))\sin(\omega t) \quad (1)$$

The non-linear equation is as (2).

$$\frac{4V_{dc}}{\pi}[\cos(\theta_1) + cos(\theta_2)] = n_1 \quad (2)$$

The 3rd- and 5th-order harmonic equations are (3) and (4).

$$\frac{4V_{dc}}{\pi}[\cos(3\theta_1) + cos(3\theta_2)] = n_3 \quad (3)$$

$$\frac{4V_{dc}}{\pi}[\cos(5\theta_1) + cos(5\theta_2)] = n_5 \quad (4)$$

In matrix form:

$$\theta = \begin{bmatrix}\theta 1\\ \theta 2\end{bmatrix} \quad (5)$$

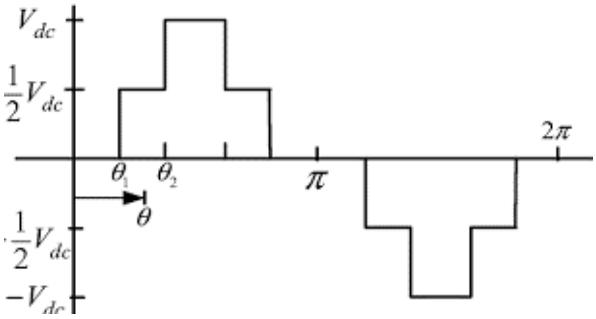

Figure 3. V_{out} of a 5-level CHBMLI at 50 Hz

Conventional SHE solution methods often rely on computationally intensive iterative numerical techniques, which typically yield only a single solution set and require an accurate initial guess and a suitable modulation index. Alternatively, analytical approaches based on symmetric polynomial and polynomial resultant theories can transform the transcendental SHE equations into polynomial forms. However, for cascaded H-bridge inverters with an increasing number of cells, the resulting polynomial order grows significantly, making analytical solution and computational implementation increasingly complex. Low-frequency conventional and optimized low-frequency SHE switching methods were presented by Dahidah *et al.* [12] and Buccella *et al.* [13]. It is highly beneficial for high/medium power converters that use fundamental switching frequency due to its design and focus on eliminating lower harmonics. A mathematical analysis shows that, for certain switching angle selections with corresponding DC sources, all harmonics are eliminated from the output voltage. Mohan *et al.* [14] offer a novel cascaded sources multilevel DC Link

(CSMLDCL) configuration for an H-bridge inverter, therefore lowering the number of components needed to achieve a desired voltage level. A number of low-frequency methods based on area equalization are suggested for multi-level inverters. Simulation and experimental data of a seven-level inverter are used to illustrate the working principle and advantages of the proposed method. Pragathi *et al.* [15] propose a novel idea for an asymmetrical hybrid single-phase multilevel inverter. LFI has an advantage over HFI:

i) Power capacity (maximum) and reliability: Low-frequency inverters (LFIs) are engineered to withstand higher power surges for extended durations compared to high-frequency inverters (HFIs). Specifically, LFIs can sustain peak power outputs of up to approximately 300% of their rated capacity for several seconds, whereas HFIs are typically limited to about 200% of their nominal power and only for very short time intervals.

ii) Reliability: LFIs with transformers are more robust and dependable than HFIs with MOSFETs, which are more vulnerable to damage from high power levels. The drawbacks of LFIs are their hefty weight (five times that of an HFI), low efficiency, and conversion efficiency of 60–70% (large self-loss) because of the low-frequency transformer. The power factor can spread up to 0.8 based on current technologies. For this reason, a lot of LFIs are designated as KVA. As harmonics depend on angles θ1, θ2, ... θn presented in Figure 3, they must be chosen wisely. The LFSHE is appropriate for choosing such angles [16], [17] by writing code in the MATLAB platform, from which the angles are calculated by reducing 3rd-order harmonics and eliminating 5th-order harmonics [18]. The analogous equations are also listed above. Even though this method is commonly employed, it is recognized that for certain specific ranges of modulation indices, a solution using the LFSHE method is not available. Thus, the angle can be found to minimize the combined contributions of the third, seventh, ninth, eleventh, and so on harmonics within these ranges.

The optimization process used to choose switching angles for the SHE approach is shown in Figure 4. First, the modulation index is changed from 0.001 to 1 with a 0.01 increment, and the switching angles and their acceptable limitations are established. The optimization task is designed to minimize the 5th-order harmonic component while meeting the fundamental-voltage restriction for every modulation-index value. The ideal switching angles within the given bounds are found using the MATLAB F_{mincon} technique. Each iteration's optimal angles are saved and used as the starting conditions for the upcoming iteration. The optimized switching-angle characteristics are plotted as a function of modulation index after this procedure is repeated until the modulation index hits unity. The output voltage waveform has odd quarter-wave symmetry.

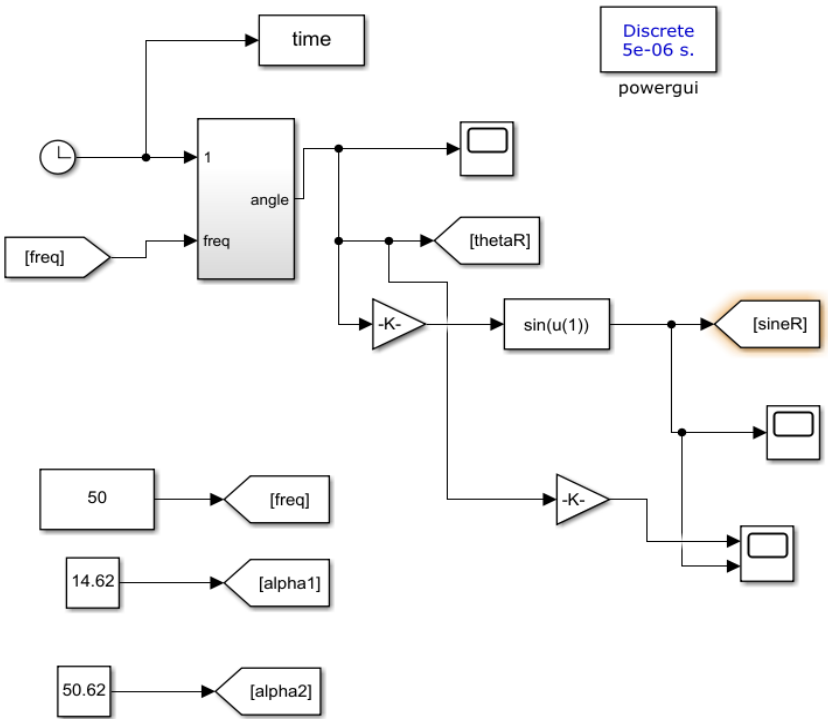

Figure 4. Switching pulse generation by SHE method (0.801 MI)

The Fourier series expansion of the output voltage V_{AO} can be written as (6).

$$f(\omega t) = \frac{4}{\pi} \int_0^{\pi/2} V_{AO}\,(\omega t)\ d\omega t, \text{ for n odd} \quad (6)$$

Where $A_n = 0$, for even n and $B_n = 0$, for all harmonic order:

$$V_{AO}(\omega t) = \sum_{n=1}^{+\infty} A_n \sin\,(n\omega t) \quad (7)$$

Where A_n - magnitude of nth harmonic:

$$A_n = \frac{4E}{n\pi} \sum_{i=1}^{p} \cos\,(n\theta i) \quad (8)$$

For N-level staircase V_{out}, number of switching angles p to be determined is given by $P = \frac{N-1}{2}$. Four harmonic components can be controlled or eliminated using a 5-level inverter (N=5) because there are four possible switching angles (N-1)=4). Theoretically, when all switching angles get closer to zero, the maximum fundamental voltage is reached.

$$A_{1max} = \frac{4p}{\pi} V_{dc1} = \frac{4}{\pi} E \quad (9)$$

In this instance, the fifth-order odd harmonic component is eliminated by determining two switching angles (θ1 and θ2). An iterative approach based on the Newton-Raphson (NR) method is one suggested solution.

$$\text{Cos}\,(\theta_1) + \text{Cos}\,(\theta_2) = \text{MI}\,\frac{\pi}{4} \quad (10)$$

The flowchart generates switching angles in MATLAB/Simulink as attached in Appendix A and displayed in Figure 5. The angles calculated for different modulation indices are attached in Appendix B for reference. The switching angles calculated are θ1=14.62°, θ2=50.62° (α1 and α2), employed in the simulation model at 0.801 MI. With these angles, the 5L inverter voltage and harmonics obtained are demonstrated in Figures 6 and 7, where only the 5th harmonic (H) is eliminated, with overall voltage THD around 17.27%.

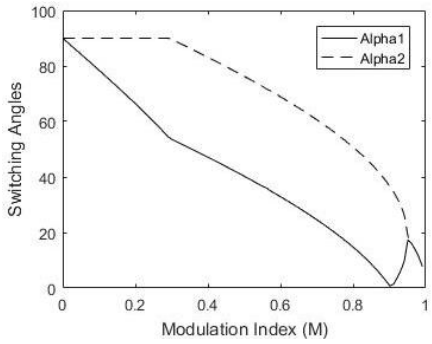

Figure 5. Switching angle versus MI

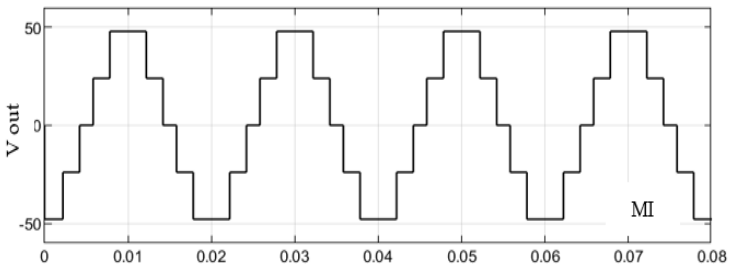

Figure 6. V_{out} waveform

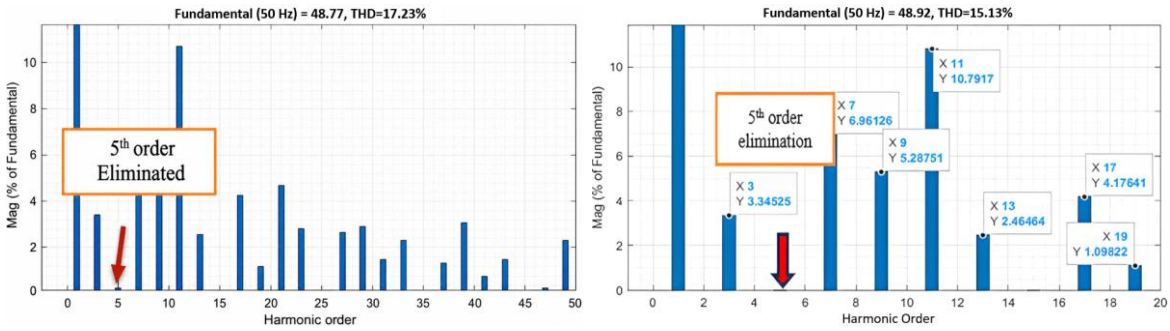

Figure 7. LFSHE PWM-generated harmonics with only fifth-order harmonic removal up to the 50th order: (a) 50th-order harmonic and (b) 20th-order harmonic

4. EXPERIMENTAL RESULTS AND DISCUSSION

Based on a MATLAB/Simulink circuit, an experimental model was built. Input DC levels, i.e., two DC supplies with corresponding values VDC1=VDC2=24 V, are employed [19]. MOSFET-equipped power modules (IRF3205) and suitable half-bridge driver circuits (IR2104) are utilized. The half-bridge driver has the following technical specifications: maximum offset voltage of 600 V; IO+/- = 130 mA/270 mA; output voltage of 10–20 V; on/off time of 680 and 150 ns; and dead time of 520 ns. A high-voltage, high-power MOSFET/IGBT driver with high-side and low-side output channels is the IR2104(S). The logic input allows for reduced 3.3 V logic operation and is compatible with normal CMOS levels. Figure 8 shows the usual electrical configuration of a gate drive circuit. A real-time ATMEGA 1280 microcontroller [20] generates gate signals for switches using reference and carrier waveforms at the fundamental frequency as specified in simulation research. Software is created in the Arduino IDE platform [20]-[23] to generate pulses to trigger MOSFET switches linked to a non-linear load of R=100 Ω and L=100 μH as a decade resistance and inductance box shown in Figure 9. The switching angles are displayed in Figure 5.

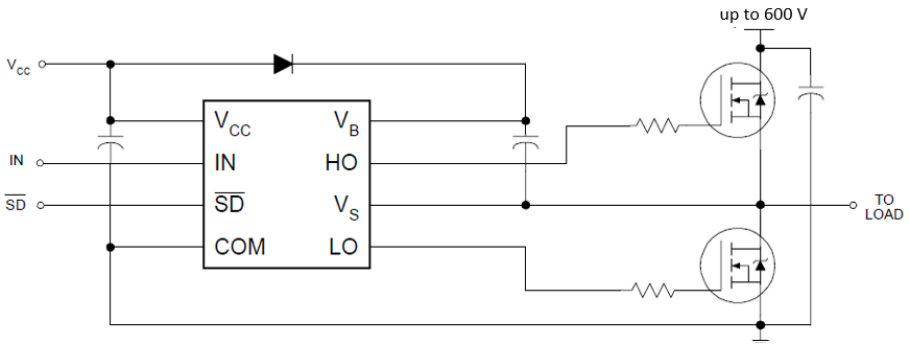

Figure 8. Gate-driver circuit electrical connection on the H-bridge board

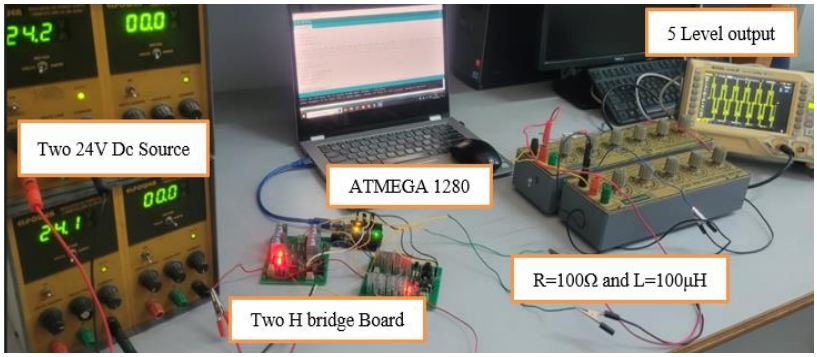

Figure 9. Working model of a multilevel inverter

The V_{out} across the load illustrated in Figure 10. The HIOKI PW3198 power quality analyzer (PQA) and RIGOL oscilloscope provide the data log of electrical parameters [24], [25]. The overall harmonics formed in the power quality analyzer are displayed in Figure 11, i.e., 18.39% obtained at 49.76 Hz. The (11) was used to determine harmonics up to the 20th order from Figure 11, with V3=0.54, V5=0.55, and so on. The result was 16.39%, which is in good agreement with simulation results.

$$\% \text{ THD} = \frac{\sqrt{V_3^2+V_5^2+V_7^2.....+V_{20}^2}}{V_1} \quad (11)$$

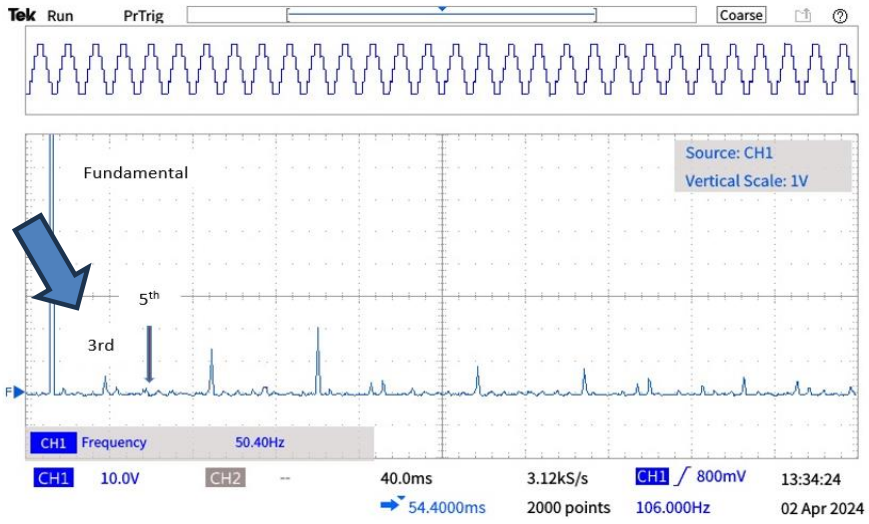

Figure 10. V_{out} and FFT analysis (REGIOL Oscilloscope)



Figure 11. Power quality analyzer: HIOKI PW 3198

5. CONCLUSION

This study presented the hardware implementation of low-frequency SHE for a multilevel inverter. The proposed switching angles were obtained by solving the SHE equations and implemented experimentally using a microcontroller-based setup. The simulation achieved a THD of 17.23%, while the experimental result was 18.39%, with a difference of only 1.16%, displaying a high degree of concordance between simulation and experimental findings. These results validate the practical feasibility of the proposed SHE technique for reducing harmonics at low switching frequency. Future work will focus on improving harmonic performance over wider operating conditions and implementing real-time SHE using FPGA technology.

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AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

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Keerti Kulkarni	✓		✓		✓	✓	✓	✓	✓	✓	✓	✓		
Priyadarshini K. Desai	✓	✓		✓	✓		✓	✓		✓	✓	✓		

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author [PNC], upon reasonable request.

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