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Design of a novel single-source 15-level inverter with self-balancing capacitors and sensorless PWM control

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ABSTRACT

Multilevel inverters (MLIs) are widely used in energy-conversion systems because they generate high-quality AC voltages with reduced harmonic distortion. However, existing MLIs often require numerous power devices, multiple DC sources, voltage sensors, or dedicated capacitor-balancing controllers, which increases both hardware cost and control complexity. This paper proposes a single-phase 15-level inverter derived from the Packed U-Cell structure. It employs a single DC source, three capacitors, and a reduced number of power switches. Based on the number of power switches, gate drivers, diodes, capacitors, DC sources, output levels, and total standing voltage per unit (TSVpu), the proposed topology achieves a lower cost function than the compared topologies reported in the literature. The proposed topology achieves a relatively low total standing voltage per unit (TSVpu) of 4.43. Sensorless open-loop SPWM offers inherent capacitor-voltage self-balancing, eliminating the need for voltage sensors or additional balancing loops. MATLAB/Simulink validation at 2 kHz and a modulation index of 1 covers steady-state operation, load transients, nonlinear loading, and DC-source voltage fluctuations. For a 50 Ω–20 mH load, the current THD is 2.20% without an output filter, confirming suitability for energy-conversion systems.

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1. INTRODUCTION

The widespread deployment of renewable energy technologies [1] and the integration of high -energy-density batteries into modern systems have greatly increased interest in multilevel inverters (MLIs) in power electronics [2]. Current applications (electric vehicles, microgrids, renewable energies, and charging infrastructure) necessitate high efficiency, compact power density, and low harmonic distortion, which MLIs effectively address through improved wave quality and reduced switching constraints [3].

However, conventional topologies [4], including cascaded H-bridge (CHB), neutral-point-clamped (NPC), and flying-capacitor (FC) inverters, have structural limitations: they require a large number of components, CHB often requires several isolated DC sources, and FC requires dedicated capacitor balancing mechanisms. Increasing the number of levels generally increases the number of switches, cost, footprint, and control complexity. This has led to the emergence of new configurations aimed at reducing components while maintaining wave quality [5]. However, reducing the number of switches can increase the total standing voltage (TSV) supported by certain semiconductors, with a possible impact on losses and reliability if the architecture is not optimized [6]. Another challenge associated with conventional multilevel inverters lies in the design of their control strategies. In this context, several advanced approaches have been developed, including robust adaptive control, integral sliding-mode control, fuzzy-observer-based sliding-mode control, and hybrid

reaching-law techniques [7]-[9]. However, these methods may increase computational burden, parameter-tuning requirements, and implementation complexity.

High-quality multilevel voltage generation generally requires numerous semiconductor devices and isolated DC sources [10]. However, multiple input sources increase converter cost, size, and implementation complexity. Single-source architectures are therefore preferred in applications such as electric vehicles and renewable-energy systems [11]. Accordingly, switched-capacitor MLIs generate multiple voltage levels from one DC source by charging and discharging capacitors through appropriate switching states under open-loop or closed-loop control [12]. The packed U-Cell (PUC) topology [13] effectively addresses the major constraints of multi-cell converters, such as single-source power supply, reduction in the number of components, TSV limitation, and minimization of harmonic distortion. Inheriting the advantages of cascaded H-Bridge (CHB) and flying capacitor (FC) structures, this hybrid architecture stands out for its advantageous TSV management [14].

Several inverter configurations derived from the PUC concept have been investigated, although several practical constraints remain. The topologies introduced in [15], [16] utilize redundant switching combinations to maintain the capacitor voltages at their required levels without the need for additional balancing controllers. Nevertheless, the use of two separate DC sources increases the supply requirements and reduces their suitability for applications based on a single DC bus. The capacitor voltages are regulated through a closed-loop scheme that depends on voltage and current measurements [17]. This solution improves controllability but requires sensing devices, signal-processing circuits, and additional control hardware, thereby increasing the implementation cost and system complexity. The converters reported in [18], [19] employ transformers to obtain the required voltage conversion and output levels. Although transformers provide galvanic isolation and voltage adaptation, they also add volume, weight, magnetic losses, and design constraints associated with turns ratios, leakage inductance, and insulation requirements. These drawbacks highlight the interest in a transformerless PUC-derived topology supplied by a single DC source and capable of achieving inherent capacitor-voltage balancing without sensors or dedicated closed-loop regulation.

In this work, a new 15-level inverter based on the PUC configuration is proposed to achieve a reduced component count, single-source operation, and good waveform quality. Its performance is evaluated using a cost function (CF), and the obtained results are validated in MATLAB/Simulink. The novelty of the proposed topology is demonstrated through a comparison with existing solutions. The main contributions include a reduced CF, low total harmonic distortion (THD), reduced total standing voltage (TSV), and a reliable sensorless control strategy. The remainder of the paper is organized as follows: i) Section 2 presents the proposed topology, operating modes, capacitor sizing, and switch-voltage stress; ii) Section 3 provides a comparative analysis; iii) Section 4 presents the simulation results; and iv) Section 5 concludes the paper.

2. METHOD

2.1. Proposed converter configuration and operating switching modes

The basic SPUC5 structure mentioned in [20] is based on five power switches. It is powered by a single DC source coupled to two capacitors, enabling the production of a five-step output voltage. As an extension of this design, a new configuration is introduced, as shown in Figure 1. The proposed solution combines the existing SPUC5 inverter with a PUC cell to increase the number of levels generated to fifteen. The resulting assembly incorporates nine switch positions, including one bidirectional switch, resulting in a total of ten IGBTs, a single DC source, and three capacitors. In addition, the switching pairs (T_1-T_2), (T_6-T_7), and (T_8-T_9) are used in a complementary manner. This arrangement enables a fifteen-level voltage output to be achieved by the developed inverter with a reduced number of components compared to conventional multilevel inverters.

The proposed inverter configuration utilizes a DC source and connects it to three capacitors. This configuration is able to generate fifteen voltage levels while at the same time ensuring the intrinsic balance of the voltages in the capacitors. The DC source and the capacitors are connected using controllable switches. These switches determine the current paths according to the output.

For testing purposes, the input source is set to $E = 6\ V_{dc}$. In open-loop operation, the capacitor voltages naturally converge to stable values of $V_{C1} = V_{C2} = E/2 = 3\ V_{dc}$ and $V_{C3} = E/6 = V_{dc}$. This is a confirmation of the topology's ability to self-balance in voltage. It is a verification of the proper distribution of the voltage, which allows us to achieve the fifteen levels of voltage.

The correspondence of each voltage level with its respective switch configuration is shown in Table 1. Figure 2 shows the current flow for the positive half-cycle. It is important to point out that the production of each of the levels is achieved by activating four switches, thereby reducing the number of devices in conduction and resulting in a high efficiency of the system.

The operating modes can be explained as follows: For the first output level (State 1), switches T_2, T_3, T_7, and T_8 are activated, as shown in Figure 2(a). This configuration allows capacitor C_3 to discharge, ensuring that a voltage of $7\ V_{dc}$ is produced at the output. In state 2, conduction is provided by T_2, T_3, T_6, and T_8,

generating an output voltage of 6 V_{dc} as shown in Figure 2(b). For state 3, switches T_2, T_3, T_6, and T_9 are activated as shown in Figure 2(c), causing capacitor C_3 to charge and producing a voltage of $5V_{dc}$. In variant 4, the simultaneous conduction of T_2, T_5, T_7, and T_8 causes capacitor C_2 to charge and C_3 to discharge, also ensuring an output of $4V_{dc}$ as shown in Figure 2(d). In state 5, switches T_2, T_5, T_6, and T_8 are activated, with C_1 in the discharging phase, resulting in an output level of $3V_{dc}$ as shown in Figure 2(e). In state 6, current flows through T_2, T_5, T_6, and T_9. Capacitors C_2 and C_3 are charged, ensuring the production of a voltage equivalent to $2V_{dc}$ as shown in Figure 2(f). In state 7, the conduction of T_2, T_4, T_7, and T_8 allows C_3 to discharge, which maintains the output at V_{dc} as shown in Figure 2(g). In state 8, to obtain the zero level, switches T_2, T_4, T_7, and T_9 are activated as shown in Figure 2(h). The other states of the negative alternation are shown in Table 1. It should be noted that there are two redundant states associated with a zero-output voltage.

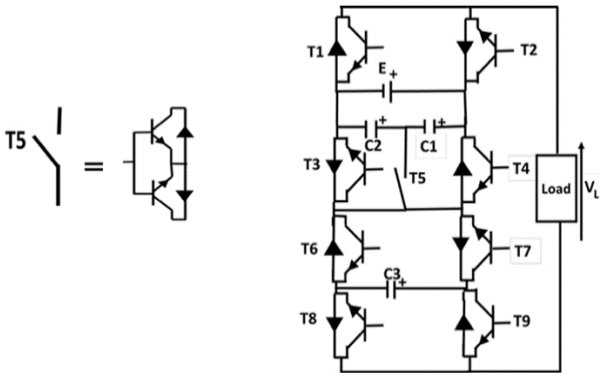


Figure 1. Proposed inverter

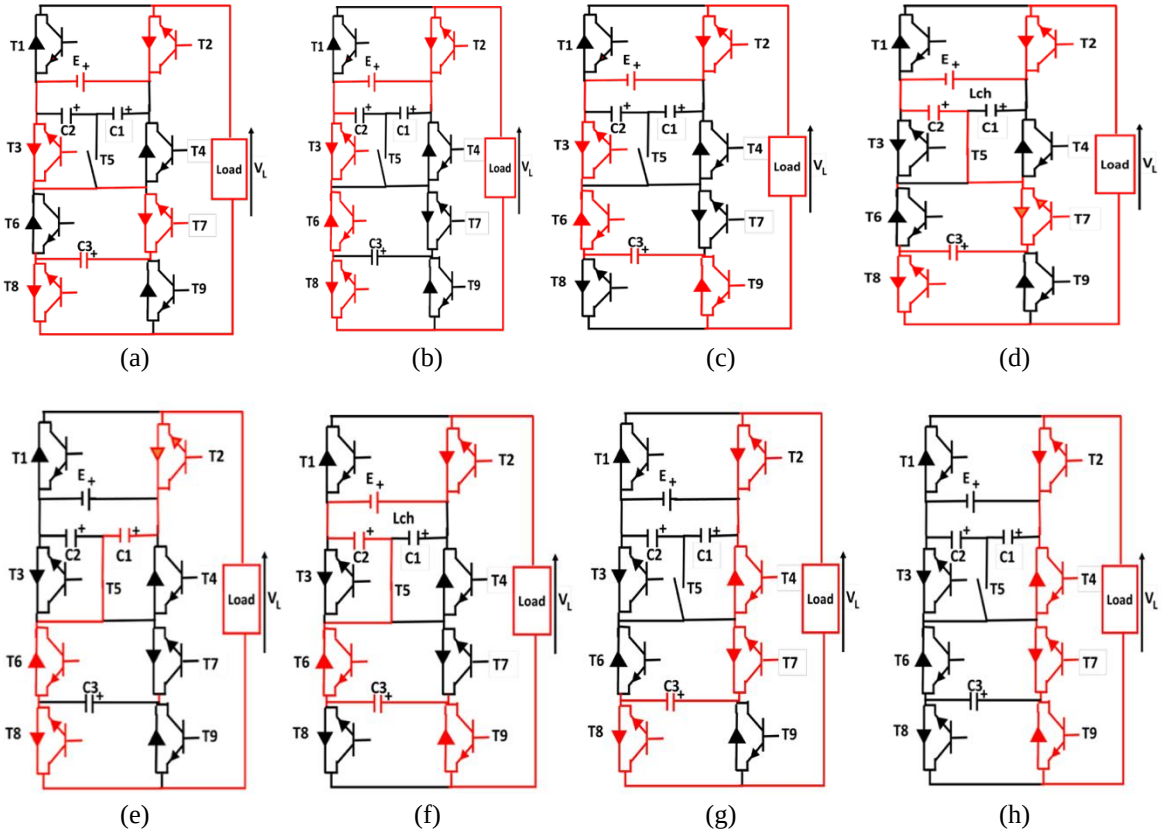


Figure 2. Operational modes and associated switching states: (a) $V_L = 7\ V_{dc}$, (b) $V_L = 6\ V_{dc}$, (c) $V_L = 5\ V_{dc}$, (d) $V_L = 4\ V_{dc}$, (e) $V_L = 3\ V_{dc}$, (f) $V_L = 2\ V_{dc}$, (g) $V_L = V_{dc}$, and (h) $V_L = 0$

Table 1. Operating and switching states

State	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9	C_1	C_2	C_3	Interconnexion	Voltage
1	0	1	1	0	0	0	1	1	0	-	-	Dis	$E+V_{c3}$	7 V_{dc}
2	0	1	1	0	0	1	0	1	0	-	-	-	E	6 V_{dc}
3	0	1	1	0	0	1	0	0	1	-	-	Ch	$E-V_{C3}$	5 V_{dc}
4	0	1	0	0	1	0	1	1	0	-	Ch	Dis	$E-V_{c2}+V_{c3}$	4 V_{dc}
5	0	1	0	0	1	1	0	1	0	Dis	-	-	V_{c1}	3 V_{dc}
6	0	1	0	0	1	1	0	0	1	-	Ch	Ch	$E-V_{C2}-V_{C3}$	2 V_{dc}
7	0	1	0	1	0	0	1	1	0	-	-	Dis	V_{C3}	V_{dc}
8	0	1	0	1	0	0	1	0	1	-	-	-	0	0
8’	1	0	1	0	0	1	0	1	0	-	-	-	0	0
9	1	0	1	0	0	1	0	0	1	-	-	Dis	$-V_{C3}$	$-V_{dc}$
10	1	0	0	0	1	0	1	1	0	Ch	-	Ch	$-E+V_{c1}+V_{c3}$	-2 V_{dc}
11	1	0	0	0	1	0	1	0	1	-	Dis	-	$-V_{C2}$	-3 V_{dc}
12	1	0	0	0	1	1	0	0	1	Ch	-	Dis	$-E+V_{c1}-V_{C3}$	-4 V_{dc}
13	1	0	0	1	0	0	1	1	0	-	-	Ch	$-E+V_{C3}$	-5 V_{dc}
14	1	0	0	1	0	0	1	0	1	-	-	-	-E	-6 V_{dc}
15	1	0	0	1	0	1	0	0	1	-	-	Dis	$-E-V_{c3}$	-7 V_{dc}

Dis: Discharging. Ch: Charging.

2.2. Capacitor design

One of the major problems in multilevel inverters is the problem of balancing the voltages of floating capacitors, which is solved using some control algorithms. In the suggested 15-level inverter, this problem has been automatically addressed with the help of a self-balance feature that obviates the need for sophisticated control algorithms. Despite that, in any kind of inverter, one of the causes of power loss is the voltage ripples of the capacitors as they charge and discharge in sequence. The voltage ripples should not exceed a limit of 5% to 10% for the output voltage to remain of high quality. As shown in Figure 3, which depicts the variations of capacitor voltage and their maximum discharge period, the variation is dependent on the value of capacitance, the discharge current, and the time interval. Thus, there should be a study of the operation cycle and constraints on current to accurately size the capacitors. Using this approach, it is feasible to regulate the peak-to-peak ripple of the voltage of capacitor Ci, which can be expressed as (1):

$$\Delta vc_i = \frac{\Delta Qc_i}{c_i} = \frac{1}{c_i}\int_{ta}^{tb} i_L(t)dt \quad (1)$$

where i_L(t) denotes the load current for a series R–L load operating under sinusoidal steady-state conditions, and is expressed as (2).

$$i_L(t) = I_m \sin(\omega t - \varphi) \quad (2)$$

The peak current I_m is given by (3).

$$I_m = \frac{V_m}{\sqrt{R^2+(\omega L)^2}} \quad (3)$$

Where ω is the angular frequency and φ is the phase lag of the current relative to the voltage, and V_m is the peak value of the voltage.

The ripple voltages of the capacitors at the MDPCi time intervals are determined using (4)-(6).

$$\Delta vc_1 = \frac{\Delta Qc_1}{C_1} = \frac{1}{C_1}\int_{t_3}^{t4} I_m \sin(\omega t - \varphi)dt \quad (4)$$

$$\Delta vc_2 = \frac{\Delta Qc_2}{c_2} = \frac{1}{c_2}\int_{t_{17}}^{t18} I_m \sin(\omega t - \varphi)dt \quad (5)$$

$$\Delta vc_3 = \frac{\Delta Qc_3}{C_3} = \frac{1}{C_3}\int_{t_1}^{t2} I_m \sin(\omega t - \varphi)dt \quad (6)$$

The capacitor values were determined by solving (4), (5), and (6) with the design criterion that the voltage ripple must not exceed 10% of the desired value, considering a load composed of a 50 Ω resistor connected in series with a 20 mH inductor, with a fundamental frequency of 60Hz, and an input DC voltage of *E=180 V*. Based on this analysis, the capacitances were set to $C_1 = C_2 = 1200$ µF and $C_3 = 2000$ µF. These chosen values guarantee adequate voltage stability across both capacitors and maintain their fluctuations within tolerable bounds under all operating conditions.

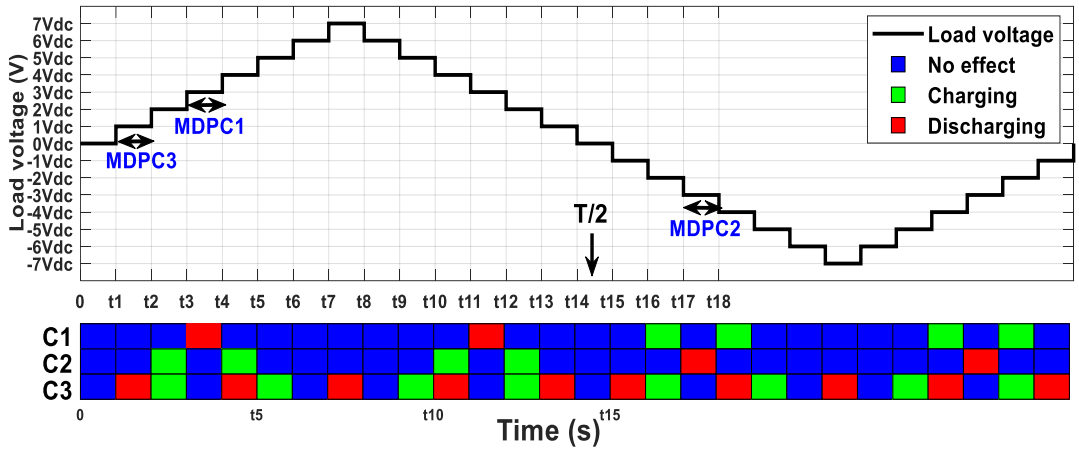


Figure 3. Waveform of the load voltage with capacitor charging-discharging

2.3. Voltage stress

For the proposed fifteen-level inverter topological configuration, a set of nine power switches has been included, of which a bidirectional switch has been incorporated into the architecture. The voltage stress of each device has been obtained by considering the operating modes of the proposed novel configuration. The blocking voltage of each device is as (7)-(9).

$$V_{T1}=V_{T2}=V_{T3}=V_{T4}=E \quad (7)$$

$$V_{T6}=V_{T7}=V_{T8}=V_{T9}=V_{C3} \quad (8)$$

$$V_{T5}=V_{C1} \quad (9)$$

The aggregate blocking voltage sustained by all semiconductor devices, designated as the total blocking voltage (TBV), is mathematically formulated as:

$$TBV=4E+V_{C1}+4V_{C3} \quad (10)$$

Regarding the voltage ratios adopted throughout this study, E = 6 V_{dc}, V_{C1} = 3 V_{dc}, and V_{C3} = V_{dc}, the total blocking voltage is determined as (11).

$$TBV=31\ V_{dc} \quad (11)$$

2.4. Gain of the designed inverter

The voltage amplification factor of the introduced topology is mathematically defined as (12).

$$G=\frac{7\,V_{dc}}{6\,V_{dc}}=1.17 \quad (12)$$

2.5. Control strategy

The proposed 15-level inverter is controlled using a sinusoidal pulse-width modulation (SPWM) scheme, selected for its simple implementation and accurate generation of the required switching instants. Figure 4 presents the complete modulation arrangement. Figure 4(a) illustrates the comparison of a sinusoidal reference signal with fourteen carrier signals having identical amplitudes and frequencies, whereas Figure 4(b) shows the electrical circuit used to generate the corresponding gate pulses. The implemented circuit operates without voltage or current sensors and does not require a dedicated capacitor-voltage control loop. According to the generated switching signals, the capacitors are periodically connected to the DC source and the load through suitable charging and discharging paths. This periodic energy exchange maintains the capacitor voltages close to their desired values while selecting the appropriate switching states required to synthesize the fifteen output-voltage levels.

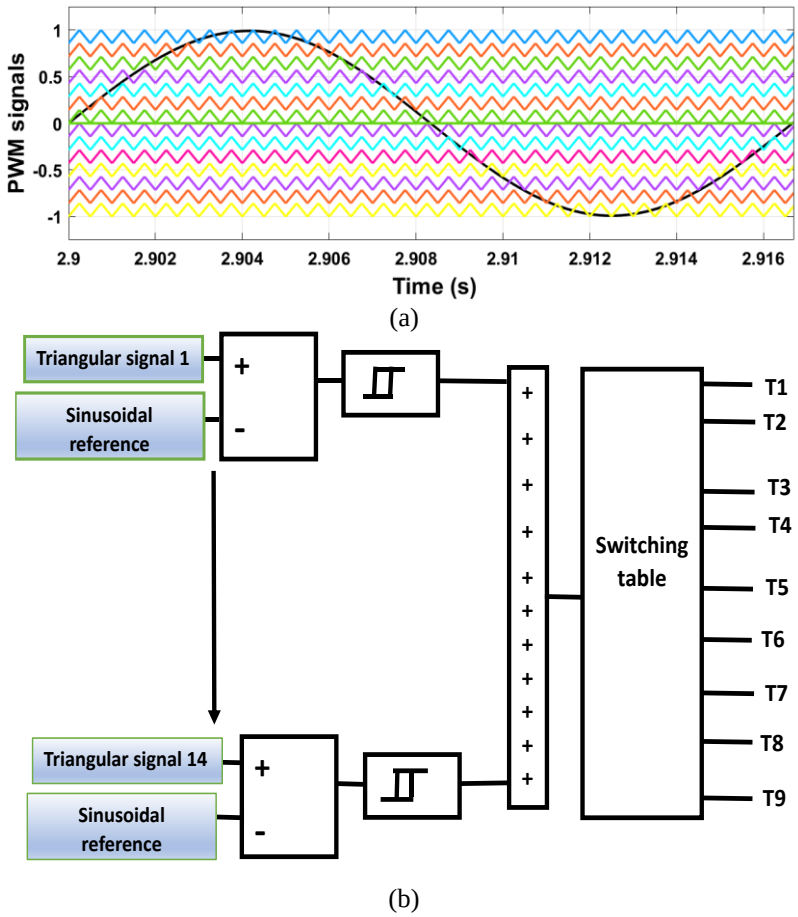


Figure 4. SPWM: (a) reference and carrier signals and (b) sensorless gate-pulse generation circuit

3. COMPARATIVE STUDY

A detailed benchmarking evaluation process is performed to objectively quantify the performance-to-cost ratio of various MLIs. The benchmarking criteria are based on a set of specific structural and technological parameters, which are widely used to compare the performance of various power conversion systems, the number of independent DC sources (N_{dc}), the total number of powers IGBTs devices (N_{Sw}), the number of diodes (N_d), the maximum number of voltage levels (N_L), the number of gate driver circuits (N_{Gd}), and the number of capacitors (N_C). Moreover, an additional parameter, total Standing Voltage per unit (TSVpu), has also been introduced to quantify the voltage stress of power devices. All of the aforementioned parameters are integrated into a single Cost Function (CF), which enables a fair comparison of the various MLI topologies presented in the existing literature. The weighting coefficient α adjusts the relative importance of semiconductor voltage stress with respect to hardware complexity. A lower value of α emphasizes component count, whereas a higher value assigns greater importance to TSVpu. The mathematical expression governing the cost function is formulated as [2]:

$$F_c = \frac{(N_{Sw}+N_d+N_{Gd}+N_c+\alpha TSVpu)N_{dc}}{N_L} \quad (13)$$

The TSV_{pu} of the introduced inverter is presented by (14) [21].

$$TSVpu = \frac{TBV}{V_{max}} = \frac{31V_{dc}}{7V_{dc}} = 4.43 \quad (14)$$

Table 2 presents a comparative analysis of the proposed topology and other multilevel inverter topologies reported in the literature, based on the cost function defined previously. The weighting coefficient α controls the relative importance assigned to the total standing voltage and hardware component count. A higher value of α = 1.5 gives greater importance to semiconductor voltage stress, whereas α = 0.5 emphasizes component reduction. Therefore, a sensitivity analysis is performed using both weighting conditions.

As shown in Table 2, the cost function of the proposed topology increases from 1.61 at α = 0.5 to 1.91 at α = 1.5. This moderate variation shows the influence of the total standing voltage on the cost function. Nevertheless, the proposed topology maintains a favorable cost-function value under both weighting conditions, confirming a robust compromise between hardware complexity and semiconductor voltage stress.

Table 2. Comparison with other topologies

Topology	Year	N_L	N_{dc}	N_c	N_{Sw}	N_{Gd}	N_d	TSVpu	CF(α=0.5)	CF(α=1.5)
[22]	2023	7	2	4	8	8	2	5.66	7.09	8.71
[23]	2024	7	1	2	7	7	2	5	2.93	3.64
[2]	2025	7	1	2	8	8	2	5.67	3.26	4.07
[24]	2022	13	1	3	15	15	0	5	2.73	3.12
[25]	2022	13	1	3	14	13	4	5.50	2.83	3.25
[21]	2025	13	1	3	11	10	3	6.33	2.32	2.81
[16]	2026	15	2	1	10	9	0	4.43	2.96	3.55
[26]	2022	15	2	1	10	10	1	4.86	3.26	3.91
[27]	2025	15	3	0	10	10	0	3.42	4.34	5.03
[28]	2023	19	2	2	9	9	6	7.2	3.12	3.87
[29]	2025	19	2	2	10	10	4	6.55	3.08	3.77
Proposed	---	15	1	3	10	9	0	4.43	1.61	1.91

4. RESULTS AND DISCUSSION

An exhaustive assessment concerning the performance of the introduced inverter, which is operating in pulse width modulation (PWM) mode, has been performed by conducting simulations in MATLAB/Simulink software. The assessment has been performed in two phases. First, the inverter has been simulated in its nominal operating conditions, and then the robustness of the system and the efficacy of the control scheme have been validated by introducing changes in the operating parameters of the inverter.

4.1. Simulation under constant parameters

Table 3 provides a comprehensive overview of the simulation setup parameters. Figure 5 illustrates the temporal variation of the load voltage V_L along with the capacitor voltages V_{C1}, V_{C2}, and V_{C3}. The results demonstrate that the proposed inverter is capable of generating a fifteen-level output voltage. In addition, the capacitor voltages are accurately regulated around their reference values, namely $V_{C1} = V_{C2} = E/2 = 90$ V and $V_{C3} = E/6 = 30$ V. Maintaining these voltage levels is essential to ensure proper operation and to achieve a high-quality output voltage. This inherent voltage balancing preserves uniform voltage steps and supports the nearly sinusoidal load current shown in Figure 6. Figure 7 presents the harmonic spectra, where Figure 7(a) shows an output-voltage THD of 9.41%, while Figure 7(b) indicates a load-current THD of 2.20%. These reduced THD values result from the stable capacitor voltages and accurate generation of the fifteen output levels, while the inductive nature of the R–L load further attenuates high-frequency current harmonics levels.

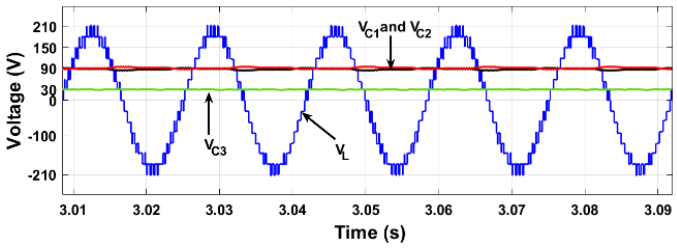


Figure 5. Waveforms of the load voltage (V_L) and the capacitor voltages (V_{C1}, V_{C2}, and V_{C3})

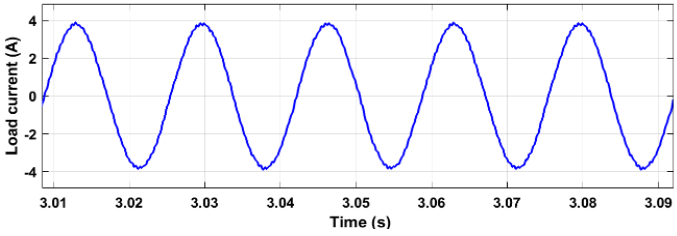
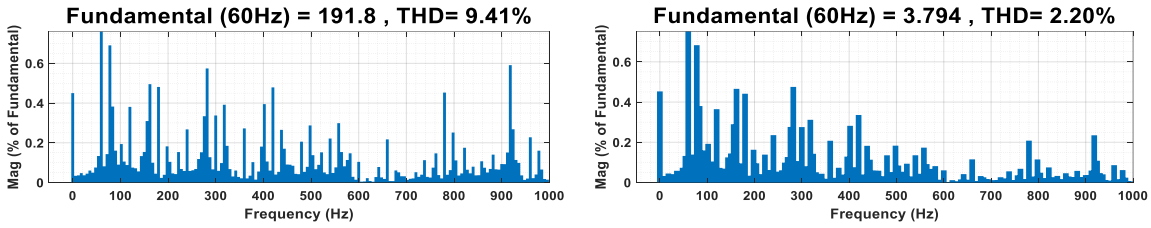


Figure 6. Waveform of load current

Table 3. Simulation sittings

Parameters	E	R	L	C1	C2	C3	Switching frequency	Modulation index	Sampling frequency
Values	180 V	50 Ω	20 mH	1200 µF	1200 µF	2000 µF	2000 Hz	1	20 kHz



(a) (b)

Figure 7. FFT-based frequency analysis of (a) the load terminal voltage and (b) the load current waveform

4.2. Response to DC supply voltage fluctuation

To assess the dynamic robustness of the designed topology, the DC input voltage E was stepped from 180 V to 90 V at t = 3 s. The capacitor and load voltages are shown in Figure 8. Figure 9 provides a close-up view of the load and capacitor voltages before and during the disturbance. Initially, V_{C1} and V_{C2} remain close to E/2, while V_{C3} remains near E/6, confirming stable sensorless voltage balancing. The sudden voltage drop creates a temporary energy imbalance in the capacitors and causes short voltage deviations. However, the PWM switching states restore the periodic charging and discharging process, allowing the capacitor voltages to recover their reference values after approximately 0.35 s, as shown in Figure 10. This transient duration represents the time required to restore the capacitor energy balance. Moreover, the preserved 15-level output waveform confirms correct voltage-level generation during and after the disturbance.

Figure 11 shows the load-current response, while Figures 12 and 13 provide enlarged views before, during, and after the input-voltage disturbance. Immediately after the voltage drop, the current exhibits a transient deviation caused by the sudden variation in the power transferred to the load. The current then recovers its quasi-sinusoidal waveform after approximately 0.35 s, indicating that stable operation is restored. This transient duration corresponds to the time required for the converter and the load to reach a new operating equilibrium. The inductive load limits current variations, while sensorless pulse width modulation (PWM) maintains the switching sequence, thus ensuring capacitor voltage regulation and a satisfactory dynamic response in case of input voltage disturbances.

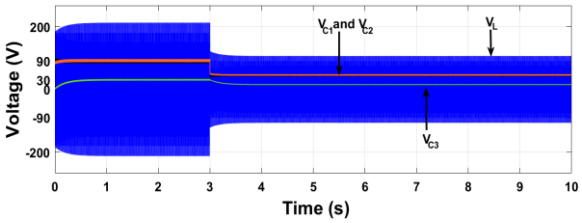


Figure 8. Waveforms of the load voltage (V_L) and the capacitor voltages (V_{C1}, V_{C2}, and V_{C3}) during the change of the DC source

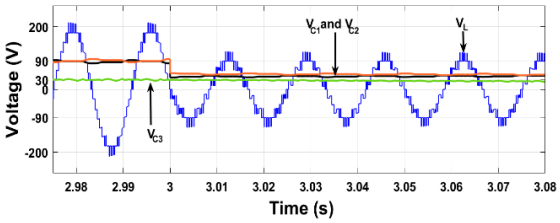


Figure 9. Zoom on the waveforms of the load voltage (V_L) and the capacitor voltages (V_{C1}, V_{C2}, and V_{C3}) before and during the change of the DC source

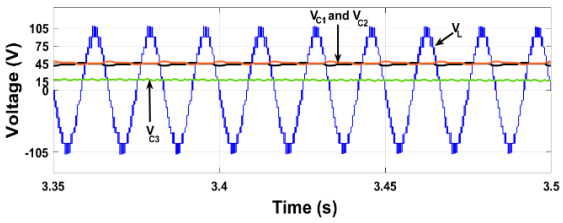


Figure 10. Zoomed-in waveforms of the load voltage (V_L) and the capacitor voltages (V_{C1}, V_{C2}, and V_{C3}) after the change of the DC source

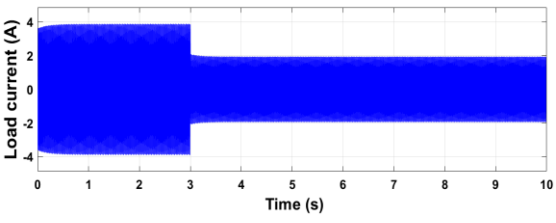


Figure 11. Waveform of the load current during the change of the DC source

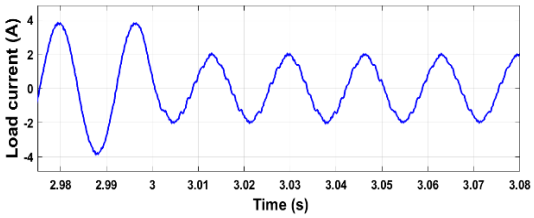


Figure 12. Zoom-in on the waveform of the load current during the change of the DC source

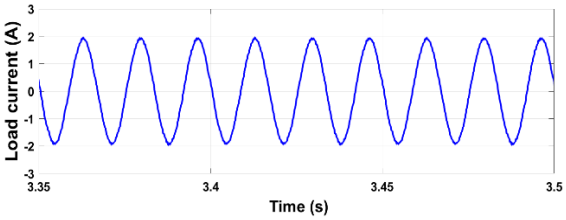


Figure 13. Zoom in on the waveform of the load current after the change of the DC source

4.3. Operation under fluctuating load conditions

It is very important to assess the performance of the inverter in variable load condition for ensuring its performance under practical working situations. In this regard, the perturbation in the form of a variation of both resistance and inductance values at the same time occurred at t = 3 s, when the resistance value increased from 50 Ω to 90 Ω, and the inductance value increased from 20 mH to 300 mH.

Unlike in normal cases, this variation does not create a noticeable transient state. The capacitor voltages adapt almost instantly to their new working conditions due to the system's very high adaptability. This behavior is explained by the effectiveness of the sensorless PWM control strategy, which ensures optimal selection of switching states and immediate load balancing.

In steady state, the capacitor voltages converge toward their reference values, with V_{C1} and V_{C2} stabilizing around E/2 = 90 V and V_{C3} close to E/6 = 30 V. This rapid stabilization confirms the robustness of the self-balancing mechanism, even in the presence of significant variations in load parameters. Maintaining these voltage levels ensures that a 15-level multilevel output voltage is preserved, both before and after the disturbance, as shown in Figure 14.

Figure 15 shows the waveform of load current. Although there are different load parameters, the waveform of load current remains sinusoidal in nature. The reason behind this phenomenon lies in the fact that the load acts as an inductor, which improves filtering action and suppresses fast fluctuations.

Ultimately, it is evident from these results that the suggested inverter topology offers superior robustness against any changes in the load. The instantaneous stabilization of capacitor voltages and the maintenance of a 15-level output voltage with excellent current quality are indicative of the reliability of the suggested topology.

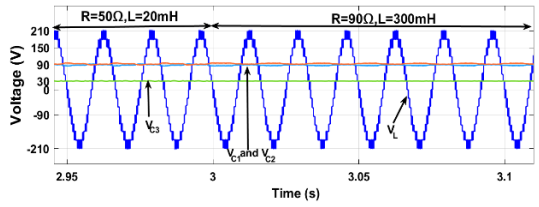


Figure 14. Waveforms of the load voltage (V_L) and the capacitor voltages (V_{C1}, V_{c2} and V_{C3}) during the change of the load

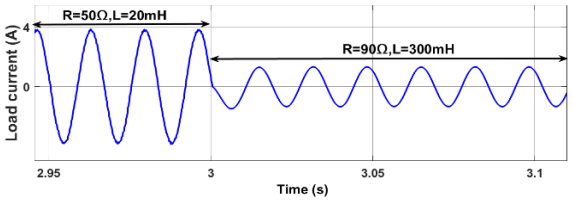


Figure 15. Waveform of the load current during the change of the load

4.4. Operation under nonlinear load conditions

Evaluating the performance of an inverter under nonlinear load conditions is essential, as these conditions are representative of real-world power electronics applications. For the analysis of the robustness of the suggested 15-level inverter, a simulation analysis is performed with consideration of a transition to a nonlinear load. Initially, a purely resistive load is connected. At time t = 3 s, it is replaced by a nonlinear load with a diode rectifier.

As shown in Figure 16, the capacitor voltages remain properly balanced and stabilize around their reference values despite the applied disturbance. This result demonstrates the efficiency of the controller scheme in achieving balanced voltages under nonlinear current conditions. Additionally, the output voltage maintains its multilevel stepped waveform, typical of a 15-level inverter, thereby proving the reliability of the suggested topology.

Figure 17 shows that the nonlinear load introduces additional harmonic components through the rectifier, increasing the load-current THD from 9.25% to 10.45%. Despite this disturbance, the current remains quasi-sinusoidal, and the THD increase is limited to 1.20 percentage points. This result indicates that the proposed inverter maintains stable voltage-level generation and satisfactory harmonic performance under nonlinear loading, confirming the effectiveness of the sensorless modulation and capacitor-voltage-balancing mechanism.

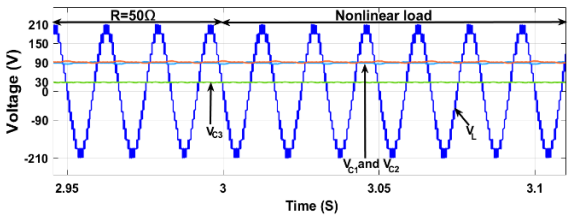


Figure 16. Waveforms of the load voltage (V_L) and the capacitor voltages (V_{C1}, V_{c2} and V_{C3}) during nonlinear load operation

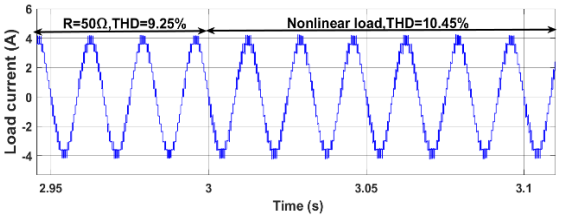


Figure 17. Waveform of the load current during the nonlinear load operation

5. CONCLUSION

This paper has presented a new 15-level inverter topology derived from the Packed U-Cell structure and supplied by a single DC source. The proposed configuration employs three capacitors and a reduced number of power components, resulting in a lower cost function compared with several multilevel inverter topologies reported in the literature. A sensorless PWM strategy ensures the natural self-balancing of the capacitor voltages without requiring voltage sensors or additional balancing control loops. The proposed inverter achieves a low THD, confirming its effectiveness under the investigated operating conditions.

The suggested converter was tested on different scenarios, including variable loads, different DC voltages, and non-linear loads. It can be seen that there is an excellent balance between the capacitors' voltages, with stability observed during both static and dynamic states. Due to its ease of control and superior power quality, it is a suitable choice for renewable energy, electric traction, and smart grids. Nevertheless, some limitations exist. On the one hand, the absence of a common ground may complicate its integration into photovoltaic systems. On the other hand, the voltage gain is relatively low, and this limits its possible applications in structures where a voltage booster is needed, given that G = 1.17. These limitations suggest several directions for future research. Future efforts will focus on developing structures with a common reference point, improving voltage gain while maintaining a compact structure and low component count, and performing detailed conduction and switching loss analyses. Model predictive control and experimental validation under practical operating conditions will also be investigated.

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AUTHOR CONTRIBUTIONS STATEMENT

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Youssef Ounejjar		✓		✓						✓		✓	✓	

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

Simulation data related to this study are available from the corresponding author.

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