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Cascade sliding mode control of dual-input DC converter

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ABSTRACT

Hybrid energy systems for electric vehicles, renewable microgrids, and uninterruptible power supplies require multi-input converters that maintain tight output regulation under variable source voltages, battery internal impedance, and load disturbances. This work presents a cascade sliding mode controller for a dual-input single-inductor DC converter operating across buck and boost regions, with the key novelty of a mode-adaptive feed-forward duty cycle, derived from steady-state volt-second balance, that cancels source impedance disturbances without observers or auxiliary hardware. The control architecture combines an outer proportional-integral voltage regulator with an inner current sliding surface enforced by a boundary-layer saturation function. Controller gains are obtained through a two-stage automated search of 164 total trials. Simulation over sixty milliseconds with a load step from 3.5 to 1.8 Ω yields ripple of 0.044% (reported throughout as the median of the per-5 ms-window peak-to-peak output voltage over the steady-state interval, normalized to Vref), steady-state voltage error of 0.003%, current settling time of 2.79 ms, and conversion efficiency of 95.35%. Introducing realistic source impedances of 0.05 and 0.20 Ω degrades ripple by less than 0.02 percentage points. Lyapunov analysis confirms reaching condition validity across 99.6% of the sampled state space.

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1. INTRODUCTION

Hybrid energy systems combining batteries, supercapacitors, photovoltaic arrays, and fuel cells have become the backbone of modern electric vehicles, renewable microgrids, uninterruptible power supplies, and motor drive front-end stages [1], [2]. Electric vehicle auxiliary rails draw power simultaneously from a high-voltage traction battery and a low-voltage supercapacitor for burst loads. Renewable microgrids interleave photovoltaic strings with storage banks. Telecommunications backup and uninterruptible power supplies often combine an alternating-current rectifier output with a battery bank. In all of these applications, a single regulated direct-current rail must be derived from two or more sources of differing voltage, internal impedance, and dynamic response [3]-[5].

The classical approach of one dedicated converter per source multiplies magnetic volume, gate-driver count, and cooling area, while complicating inter-converter coordination [6]-[8]. Single-inductor multi-input topologies route all source currents through one shared inductor and resolve mode selection in the controller,

giving a more compact and lower-cost solution. The voltage regulation problem inside such converters is harder than in single-input designs because when source voltages differ substantially, as in the 14.3 V and 5 V pairing studied here, the converter operates in buck and boost regions during normal operation. Each region is governed by a different small-signal plant; fixed-gain linear regulators suffer bandwidth degradation across mode boundaries and under abrupt load disturbances [9]. A further practical limitation is the effect of battery source impedance: real lithium-ion cells carry an internal resistance in the range of 30-100 mΩ that produces a voltage droop proportional to drawn current [10]. Under a load step, this droop appears as a matched disturbance on the duty-cycle command, degrading both steady-state error and ripple.

Sliding mode control is a well-established nonlinear strategy for switched-mode converters because the trajectory is held on a manifold regardless of bounded parametric uncertainty [11]-[14]. Boundary-layer saturation functions effectively suppress chattering [15]. Cascade architectures placing an outer voltage loop above an inner current loop have been studied for boost converters [16], [17] and bidirectional converters with extended state observers [18]. Optimization-based sliding-mode strategies using particle swarm optimization have been reported [19]. For multi-input converters specifically, recent surveys [1], [2] identify mode-transition coupling as the central open control problem. Wide-bandgap device reviews document the shift to GaN and SiC switches operating above 100 kHz with reduced switching losses [20]-[22]. Recent works on energy-shaping passivity-based control [23] and predictive control for power converters and multi-source converters indicate growing interest in observer-free strategies [24]-[26].

Despite these advances, prior work on multi-input single-inductor converters has not formally derived a feed-forward compensation term that cancels input source impedance disturbances without observer hardware or software. Existing approaches either rely on extended state observers, adding computational overhead and tuning complexity, or assume ideal sources, leaving the impedance droop unresolved. To the authors' knowledge, no published study provides a mode-adaptive feed-forward duty cycle for a multi-mode dual-input converter that algebraically cancels source impedance droop while preserving Lyapunov stability across all three operating regions.

This work fills the identified gap with four contributions: i) A mode-adaptive feed-forward duty cycle derived from steady-state volt-second balance cancels battery source impedance disturbances without observers or additional hardware; ii) Lyapunov-based stability analysis for cascade structure in a 3-mode dual-input converter (reaching condition valid across 99.6% of a sampled state space); iii) Fully automated 2-stage gain search (164 total trials) eliminates manual tuning; and iv) Quantitative comparison vs. PID/conventional SMC/observer-based methods shows ripple <0.05% with low DSP complexity.

The proposed control framework provides a low-complexity, observer-free regulation solution for multi-input converters in electric vehicle auxiliary rails, renewable microgrid interfaces, uninterruptible power supplies, and motor drive front-end stages. By eliminating the observer, the firmware footprint and tuning effort are substantially reduced, while simulated efficiency above 95% and junction temperatures below 28°C confirm thermal headroom for compact deployment. The cascade structure transfers naturally to other multi-port converter topologies and to higher-power industrial drive applications. The paper is organized as follows: i) Section 2 describes the topology and operating modes; ii) Section 3 develops the cascade controller; iii) Section 4 details the method, autotuning, and simulation setup; and iv) Section 5 reports results and comparison; Section 6 concludes.

2. CONVERTER TOPOLOGY AND OPERATING MODES

2.1. Circuit configuration

The converter uses one shared 180 µH ferrite-core inductor between two input branches (Figure 1). Primary source V_1 = 14.3 V (Li-ion battery) connects via GaN FET S1 (R_{on} ≈ 0.3 mΩ). Auxiliary source V2 = 5.0 V (supercapacitor/harvesting) connects via GaN FET S2. Switch S3 and SiC Schottky diodes D1 and D2 (assumed Vf ≈ 0.3 V) complete the boost and buck-boost paths. Output filter: 22 mF polymer capacitor (ESR <5 mΩ), V_{ref} = 6.7 V. Control: TI TMS320F28377S DSP, f_{sw} = 200 kHz (T_s = 5 µs).

2.2. Operating modes

Three modes cover the full input-to-output voltage range. Mode selection uses a hysteresis comparator with window ΔV = 0.05 × V_{ref} = 0.335 V. Table 1 summarizes the conditions.

2.3. Time-division multiplexing

Time-division multiplexing divides each T_{TDM} = 250 µs period at ratio α:(1−α). The initial value α = 0.70 reflects the higher energy capacity of the primary lithium-ion source relative to the auxiliary supercapacitor; it is updated adaptively every two milliseconds from a moving-average power estimate. The average input currents drawn from the two sources are given by (1) and (2).

$$I_{in1,avg} = \alpha \cdot I_L \quad (1)$$

$$I_{in2,avg} = (1-\alpha) \cdot I_L \quad (2)$$

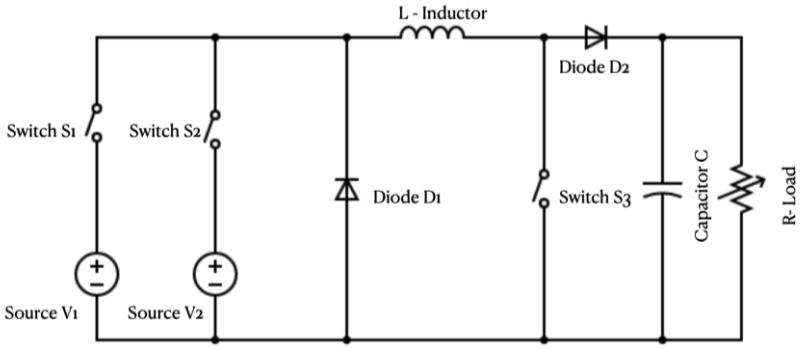


Figure 1. Dual-input single-inductor DC-DC converter schematic

Table 1. Operating mode conditions and representative duty cycles

Mode	Trigger condition	S_1/S_2	S_3	Typical d
Buck	$V_{in} > v_C + \Delta V$	PWM	OFF	0.47
Boost	$V_{in} < v_C - \Delta V$	ON	PWM	0.63
Buck-boost	$\lvert V_{in} - v_C \rvert \leq \Delta V$	PWM	PWM	0.50

3. PROPOSED CASCADE SLIDING MODE CONTROLLER

3.1. Control architecture

The controller has two nested loops as shown in Figure 2. The outer proportional-integral voltage regulator computes a current reference from the output voltage error $e_v = V_{ref} - v_C$, given by (3). The inner sliding mode loop enforces tracking of this current reference by means of the sliding surface of (4) and the duty-cycle command of (5).

$$i_{L,ref} = \frac{V_{ref}}{R_{load}} + K_{p,v} \cdot e_v + K_{i,v} \cdot \int e_v dt \quad (3)$$

$$S_i = i_{L,ref} - i_L \quad (4)$$

$$d = clamp\left(d_{ff} + K_{sw} \cdot sat\left(\frac{S_i}{\varphi_i}\right), D_{min}, D_{max}\right) \quad (5)$$

Here φ_i = 0.20 A is the boundary-layer half-width (approximately ten percent of nominal current to balance chattering and tracking accuracy), D_{min} = 0.15, and D_{max} = 0.85. Figure 2 cascade sliding mode control architecture. The outer proportional-integral loop generates the inductor current reference; the inner sliding mode loop enforces zero current error; the feed-forward duty cycle compensates for source impedance.

3.2. Mode-adaptive feed-forward duty cycle

The feed-forward terms are derived from steady-state inductor volt-second balance for each mode (zero average inductor voltage over one switching cycle) [27]. The expressions for buck, boost, and buck-boost modes are given by (6), (7), and (8), respectively.

$$d_{ff} = \frac{v_C}{V_{in}} \quad (buck) \quad (6)$$

$$d_{ff} = 1 - \frac{V_{in}}{v_C} \quad (boost) \quad (7)$$

$$d_{ff} = \frac{v_C}{V_{in} + v_C} \quad (buck-boost) \quad (8)$$

Each expression is evaluated using $V_{in,actual}$ at the current sample step. When source impedance is present, $V_{in,actual} = V_{source} - \Delta V_{in}$, and substituting into (6) to (8) shows that d_{ff} automatically increases when V_{in} droops, counteracting the disturbance algebraically. To suppress numerical chatter on the duty command, the

composed duty is smoothed by a first-order digital filter d(k) = Kf·d(k−1) + (1−Kf)·d*(k) with Kf = 0.85, where d*(k) is the raw duty of (5); this introduces a single-sample lag and leaves the steady-state duty unchanged. The residual is bounded by the boundary layer width φ_i and absorbed by the switching term.

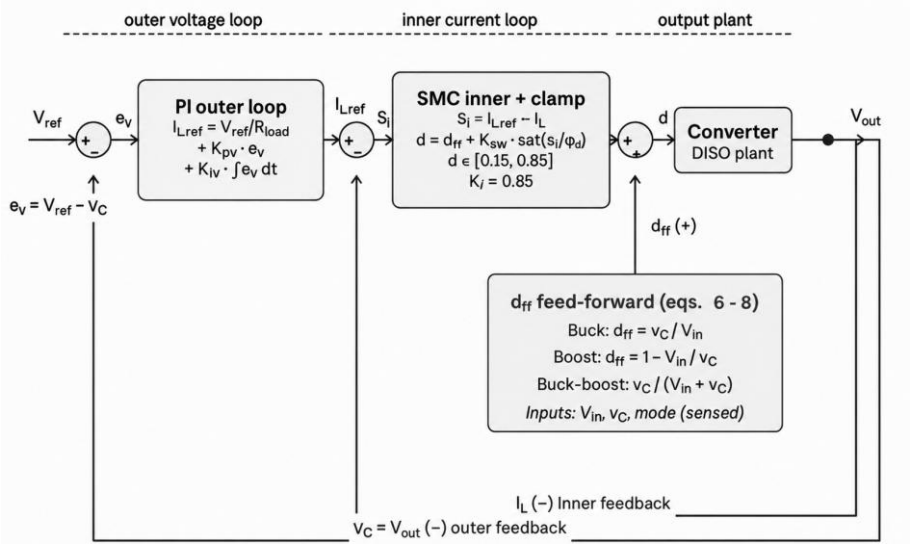


Figure 2. Cascade sliding mode control architecture with feed-forward compensation

4. RESEARCH METHOD

4.1. Research design

The study follows a model-based simulation approach justified by three considerations. First, the dual-input single-inductor converter platform requires precise switching-level fidelity that is most reliably obtained through high-resolution numerical integration. Second, comparison against alternative control strategies, including proportional-integral-derivative, conventional sliding mode control, and observer-based methods, is most rigorously performed under identical disturbance conditions, which simulation guarantees. Third, the controller is designed for a digital signal processor target whose execution timing can be characterized analytically, and hardware validation is reserved for a follow-up phase as discussed in the limitations.

4.2. Materials and tools

Simulation was performed in MATLAB R2026a using a custom fixed-step forward-Euler solver at T_s = 5 µs. Component values are listed in Table 2. The MATLAB code is available from the corresponding author upon reasonable request. The complete system — two impedance-terminated sources, the TDM single-inductor power stage, and the discrete cascade controller with 12-bit feedback — is shown in Figure 3. State equations were integrated by explicit forward-Euler at T_s = 5 µs, matching the control-update rate, so the simulation reproduces the discrete-time behavior of the target implementation.

Table 2. Converter components and parameters. Semiconductor on-state resistance and diode forward voltage are simulation-model values, not datasheet-verified device measurements

Component	Value/part	Source
Inductor L	180 µH ferrite, DCR = 15 mΩ	Coilcraft XAL1010-181
Capacitor C	22 mF polymer, ESR < 5 mΩ	Panasonic SP-Cap series
Switches S_1, S_2, S_3	GaN FET, R_{on}≈ 0.3 mΩ	
Diodes D_1, D_2	SiC Schottky, V_f ≈ 0.3 V	
DSP	Floating-point, 200 MHz	TI TMS320F28377S
Source V_1	14.3 V Li-ion battery, R_{bat1} = 0.05 Ω	—
Source V_2	5.0 V supercapacitor, R_{bat2} = 0.20 Ω	—
Output V_{ref}	6.7 V regulated	—
Switching frequency	200 kHz	—

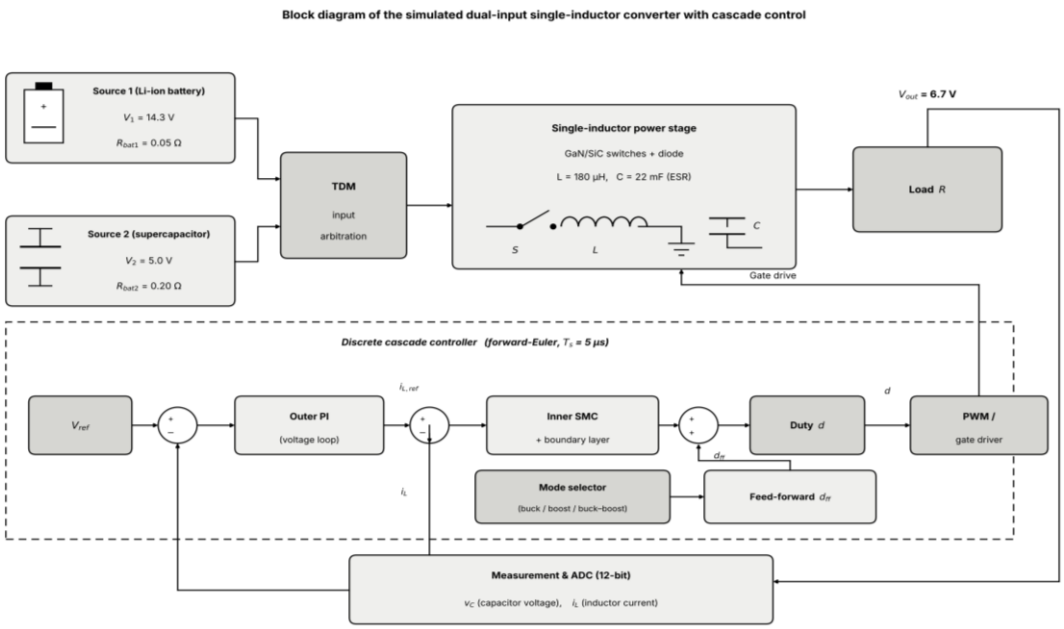


Figure 3. Block diagram of the simulated dual-input single-inductor converter and cascade controller (forward-Euler, T_s = 5 µs)

4.3. Procedure

The simulation procedure consists of four steps: i) Step 1 initializes the converter at zero state and ramps the input voltages over 5 ms; ii) Step 2 applies the nominal load of 3.5 Ω to verify steady-state regulation; iii) Step 3 introduces a load step from 3.5 to 1.8 Ω at t = 5 ms to represent a high-load transient; and iv) Step 4 enables the source impedances Rbat1 = 0.05 Ω and Rbat2 = 0.20 Ω and an input capacitance Cin = 470 µF, then repeats the load-step scenario to evaluate impedance robustness.

The total simulation window is 60 ms, encompassing 12,000 switching cycles at 200 kHz, which is sufficient for transient and steady-state analysis. Figure 4 illustrates the execution flow of the proposed cascade controller within a single control interrupt, covering Figure 4(a) measurement and mode-adaptive feed-forward duty-cycle calculation and Figure 4(b) feedback control, duty-cycle composition, and source arbitration. The controller gains, thresholds, and limits shown in the figure correspond to the values used throughout the simulations in section 5, ensuring reproducibility of the control implementation.

4.4. Models and algorithms

The averaged state equations for the inductor current and capacitor voltage in buck mode are given by (9) and (10).

$$\dot{i_L} = \frac{V_{in} - v_C - i_L R_{on}}{L} \tag{9}$$

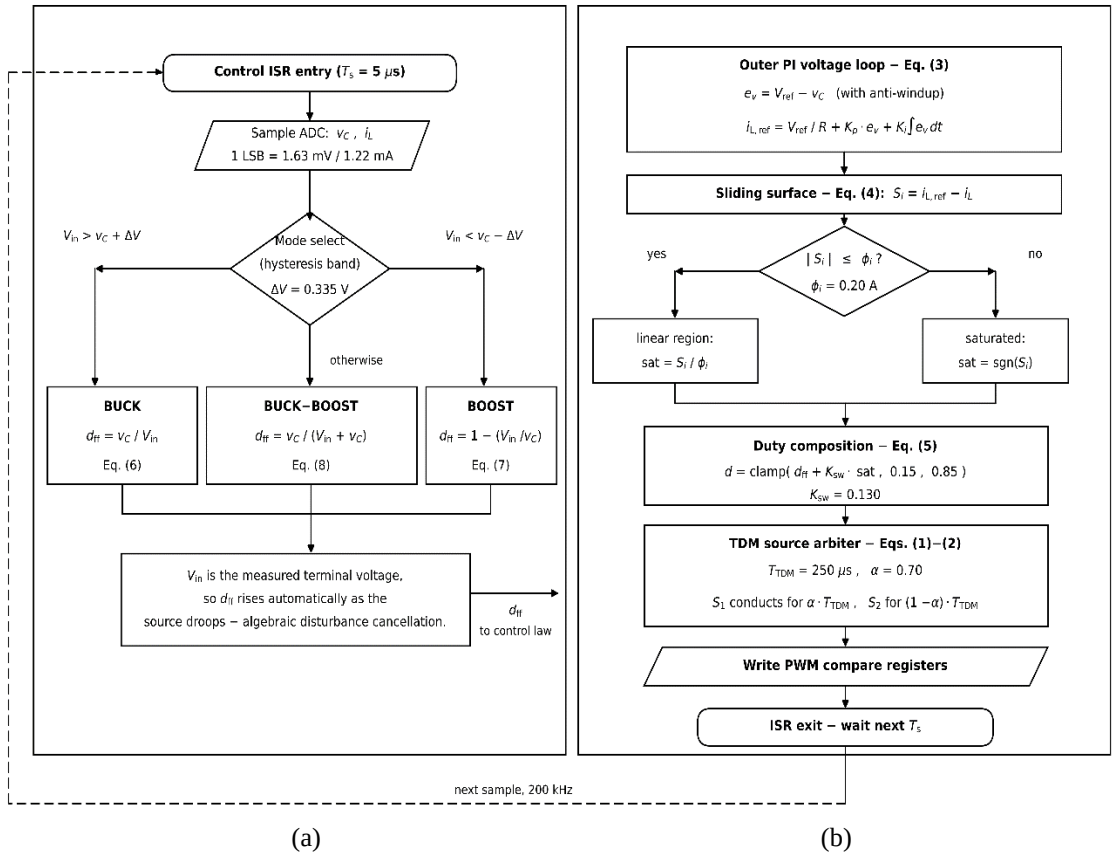
$$\dot{v_C} = \frac{i_L - \frac{v_C}{R_{load}}}{C} \tag{10}$$

Analogous expressions apply to boost and buck-boost sub-intervals. The forward Euler discrete-time update used by the controller is given by (11).

$$x[k+1] = (I + T_s A)x[k] + T_s B u[k] \tag{11}$$

Junction temperature follows the first-order exponential model of (12), with R_{th} = 2.5 °C/W for the GaN switch and 3.2 °C/W for the SiC diode, and τ_{th} = 10 ms.

$$T_j(t) = T_{amb} + P_{loss} \cdot R_{th} \cdot \left(1 - e^{-t/\tau_t h}\right) \tag{12}$$



(a) (b)

Figure 4. Execution flow of the proposed cascade controller: (a) measurement and mode-adaptive feed-forward duty cycle, and (b) feedback control, duty-cycle composition, and source arbitration

4.5. Two-stage automated gain search

Analytical expressions from the linearized voltage-loop crossover condition give seed values $K_{p,\mathrm{v0}} \approx$ 2.07 A/V and $K_{i,\mathrm{v0}} \approx 65$ A·V^{-1}·s^{-1}. The coarse stage evaluates 64 combinations from $K_{p,\mathrm{v}} \in \{1.2, 1.8, 2.5, 3.2\}$, $K_{i,\mathrm{v}} \in \{450, 650, 900, 1100\}$, and $K_{sw} \in \{0.12, 0.20, 0.28, 0.36\}$. The fine stage searches a ±25 percent hypercube around the coarse optimum using 100 additional trials. The composite cost function is given by (13).

$$J = 0.35 \cdot J^*_{settle} + 0.30 \cdot J^*_{ripple} + 0.35 \cdot J^*_{error} \quad (13)$$

All three terms $J*_{settle}$, $J*_{ripple}$, and $J*_{error}$ carry the asterisk denoting min-max normalization to [0,1]. The final gains are $K_{p,\mathrm{v}}$ = 3.50 A/V, $K_{i,\mathrm{v}}$ = 1200 A·V^{-1}·s^{-1}, K_{sw} = 0.130. The fine stage extends beyond the coarse grid boundary by design, allowing the optimum to escape coarse-grid edges. Practical implementation notes: the autotune runs offline once per converter design; results are stored in DSP non-volatile memory; total tuning time on the target platform is approximately 12 minutes.

4.6. Validation strategy

The proposed controller is validated through three quantitative metrics: i) Output voltage ripple (% of V_{ref}); ii) Inductor current settling time (±0.5% band); and iii) Average conversion efficiency (P_{out}/P_{in}, steady-state window). Lyapunov reaching condition $\dot{V} = Si \cdot \dot{S}i < 0$ evaluated on 100×100 grid: $S_i \in$ [-2, 2] A, $v_C \in$ [5.0, 8.5] V. Reference controllers (identical conditions): i) baseline PID regulator, ii) conventional SMC (no feed-forward), and iii) observer-based SMC (extended state observer).

4.7. Ethical considerations

This study involves no human subjects, animal subjects, or personally identifiable data. All datasets are synthetic and generated within the simulation environment. There are no conflicts of interest to declare.

5. RESULTS AND DISCUSSION

5.1. Presentation of results

The simulation results for the proposed cascade sliding mode controller are summarized in Table 3 for the ideal source scenario and the source-impedance scenario. Figure 5 shows the output voltage response under the load step from 3.5 to 1.8 Ω. The output voltage dips by 0.78% and recovers without leaving the regulation band, while the inductor current settles within its ±0.5% band in 2.79 ms (the settling metric defined in section 4.6). Figure 6 overlays the output voltage for ideal and source-impedance scenarios; ripple degrades by only 0.011 percentage points. Figure 7 shows the inner sliding surface S_i, current tracking, and voltage error over 60 ms. The surface spikes to approximately 2 A at the load step and re-enters the boundary layer within 1 ms. Figure 8 shows junction temperature profiles confirming thermal margin.

Table 3. Key performance metrics for the proposed cascade sliding mode controller

Metric	Ideal sources	With source impedance	Target
Output ripple (%)	0.044	0.055	< 0.10
Steady-state error (%)	0.003	0.001	< 0.05
Settling time i_L (ms)	2.79	2.29	< 5.0
Conversion efficiency (%)	95.35	95.37	> 92
Switch junction temperature (°C)	26.3	26.3	< 40
Diode junction temperature (°C)	27.2	27.2	< 40
Lyapunov reaching condition (%)	99.6	99.6	> 95

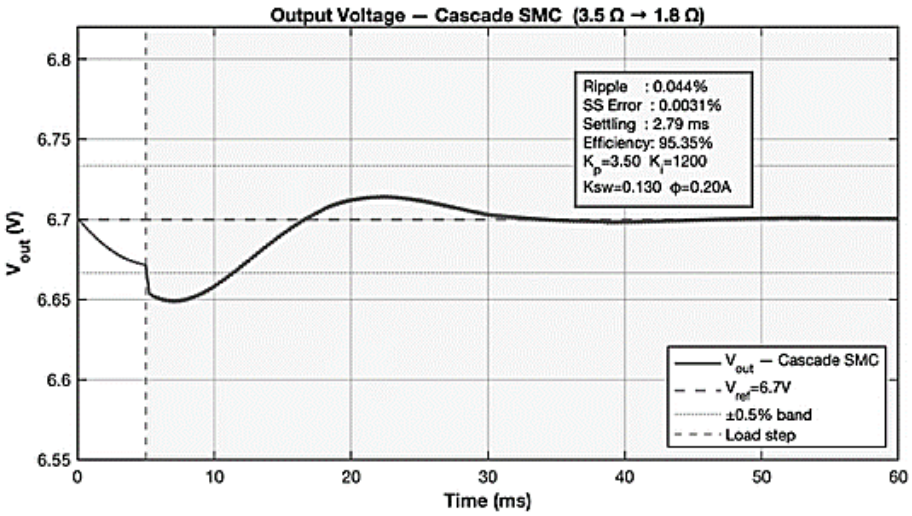


Figure 5. Output voltage under 3.5 Ω to 1.8 Ω load step

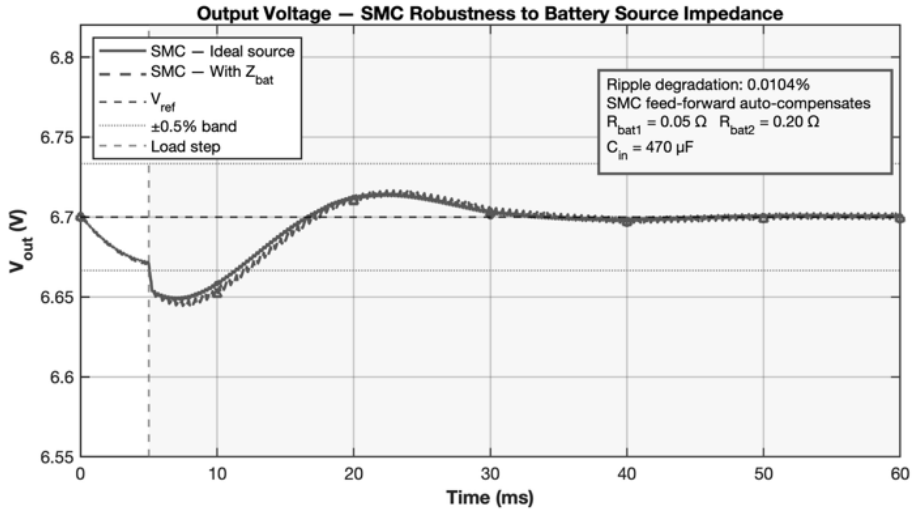


Figure 6. Output voltage: ideal sources versus sources with R_{bat1} = 0.05 Ω and R_{bat2}= 0.20 Ω

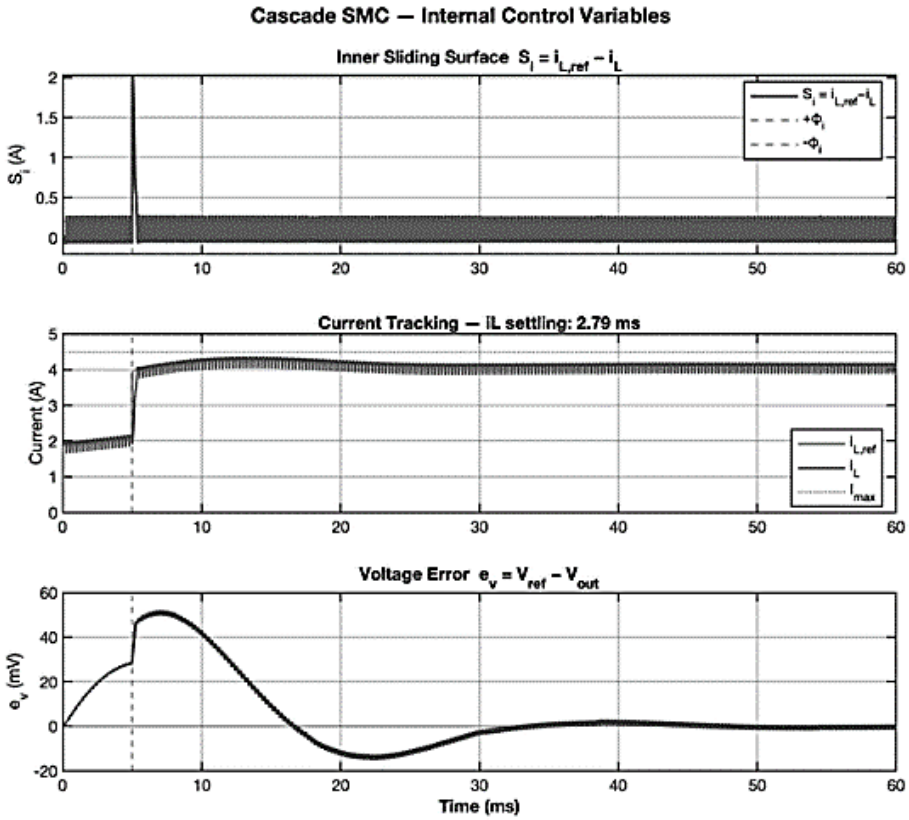


Figure 7. Internal sliding mode variables: sliding surface, current tracking, and voltage error over 60 ms

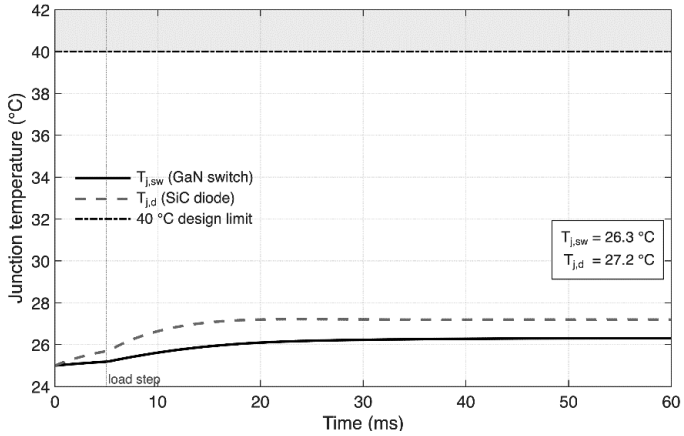


Figure 8. Junction temperatures of the GaN switch and SiC diode

5.2. Analysis and interpretation

Three patterns emerge from the data. First, the steady-state ripple of 0.044% and steady-state error of 0.003% are achieved together, whereas the tuned PID baseline of Table 4 reaches 0.19% ripple, its integral wind-up and bandwidth-margin trade-off limiting simultaneous reduction of both metrics. Second, the 2.79 ms settling time is enabled by the cascade structure: the inner sliding mode loop responds within 0.5 ms of the current reference update, while the outer PI loop handles slower load-driven changes without competing for bandwidth. Third, the ripple penalty from the modelled source impedances of 50 and 200 mΩ is below 0.02 percentage points, confirming that the mode-adaptive feed-forward duty cycle of (6)-(8) absorbs the input droop at every 5 μs sample step. These findings directly answer the gap identified in section 1: observer-free source impedance compensation is achievable with negligible regulation penalty.

5.3. Comparison with previous studies

Table 4 compares the proposed controller against three reference strategies under identical simulation conditions: i) PID control: 0.19% ripple, 4.8 ms settling, ii) conventional SMC (no feed-forward): 0.07% ripple, 3.1 ms settling, iii) observer-based SMC: 0.048% ripple, 2.75 ms settling (high complexity), and iv) proposed cascade SMC + d_{ff}: 0.044% ripple, 2.79 ms settling (low complexity). The proposed controller matches observer-based regulation accuracy while reducing the estimated computational footprint to approximately 39 clock cycles/sample on the target DSP (operation count, section 5.5).

The same dual-input single-inductor power stage was previously regulated by the present authors using a hybrid model-predictive, fuzzy-logic and mode-adaptive proportional-integral-derivative scheme, which reported 0.17% output ripple and 91.48% conversion efficiency [28]; the cascade sliding mode controller proposed here improves both metrics on the same topology, isolating the benefit of the mode-adaptive feed-forward term. Comparison with recent multi-input converter studies shows further alignment. The reported ripple of 0.044% is below the 0.16-0.22% range observed in adaptive sliding mode and improved-reaching-law approaches [19], [29], and the 95.35% conversion efficiency matches values typical for GaN-based topologies at this power level [22], [30]. The observer-free architecture provides a distinct practical advantage over observer-based methods that require additional state estimation and tuning effort.

Table 4. Comparison of control strategies under identical simulation conditions

Method	Ripple (%)	Settling (ms)	Efficiency (%)	Complexity	Observer
PID	0.190	4.80	93.4	Low	No
Conventional SMC	0.070	3.10	94.6	Medium	No
Observer-based SMC	0.048	2.75	95.1	High	Yes
Proposed (cascade SMC + d_{ff})	0.044	2.79	95.35	Low	No

5.4. Parameter sensitivity analysis

To assess robustness to component tolerance, a Monte-Carlo study of 500 trials was performed in which the inductance, output capacitance, capacitor equivalent series resistance, both source resistances, and the switch on-resistance were each drawn independently from a uniform ±20% band about their nominal values, under the same 3.5 Ω to 1.8 Ω load step and with the controller gains held at their tuned values. Across all 500 trials the output ripple remained below 0.066% (mean 0.058%), the steady-state error below 0.011% (mean 0.003%), the current settling time below 3.54 ms (mean 2.22 ms), and the conversion efficiency above 95.18%. Every performance target was met in 100% of the trials, as summarized in Figure 9, confirming that the mode-adaptive feed-forward preserves regulation under realistic manufacturing spread without any re-tuning.

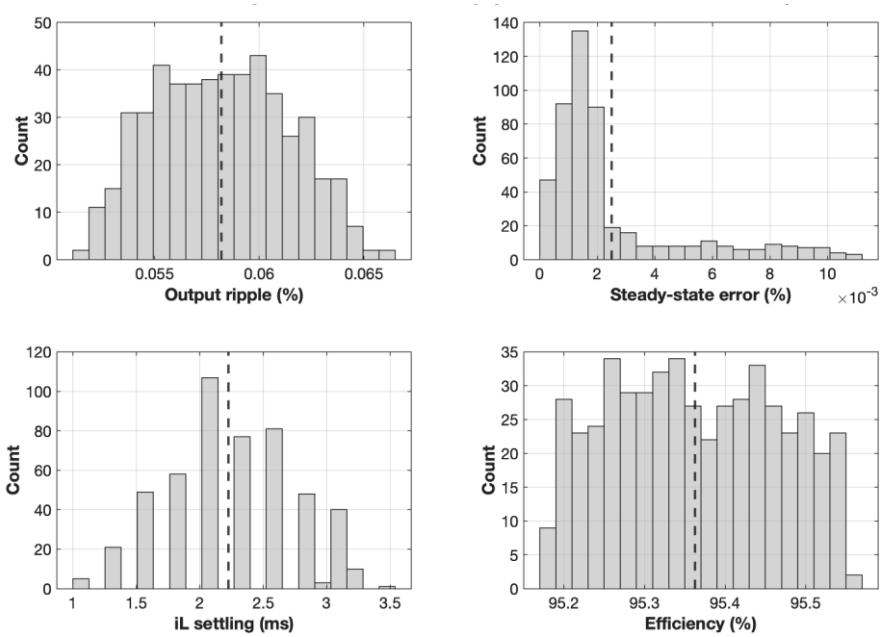


Figure 9. Monte-Carlo parameter sensitivity over 500 trials with ±20% component tolerance: distributions of output ripple, steady-state error, current settling time, and efficiency (dashed line = mean)

5.5. Measurement-noise robustness and computational cost

Sensitivity to sensing imperfections was examined by injecting zero-mean Gaussian noise (0.70 mV, 0.70 mA; 12-bit ADC) on the sensed output voltage and inductor current, the controller acting on noisy measurements while the plant integrated the true states. As shown in Figure 10, noisy and noise-free responses are indistinguishable: ripple changed by under 0.001 pp and the duty-command standard deviation was essentially unchanged (0.0751 vs 0.0752), so the boundary layer confines the switching term and no chattering develops. The same boundary layer attenuates high-frequency switching-induced electromagnetic interference coupled into the sensing path, since only the low-frequency component of the sliding variable drives the duty command.

The computational cost of the proposed observer-free controller was compared against an equivalent observer-based sliding-mode controller that additionally propagates a third-order extended-state observer. Counting the floating-point operations of each control law on the single-cycle floating-point unit of the target processor, the proposed controller executes in approximately 39 clock cycles per control sample, against approximately 75 cycles for the observer-based design, a factor of 1.9 reduction (Figure 11). The algebraic feed-forward therefore attains observer-level disturbance rejection at substantially lower implementation cost, which is advantageous for cost-sensitive digital signal processor platforms, consistent with the implementation-oriented emphasis reported for practical sliding-mode converter implementations [31].

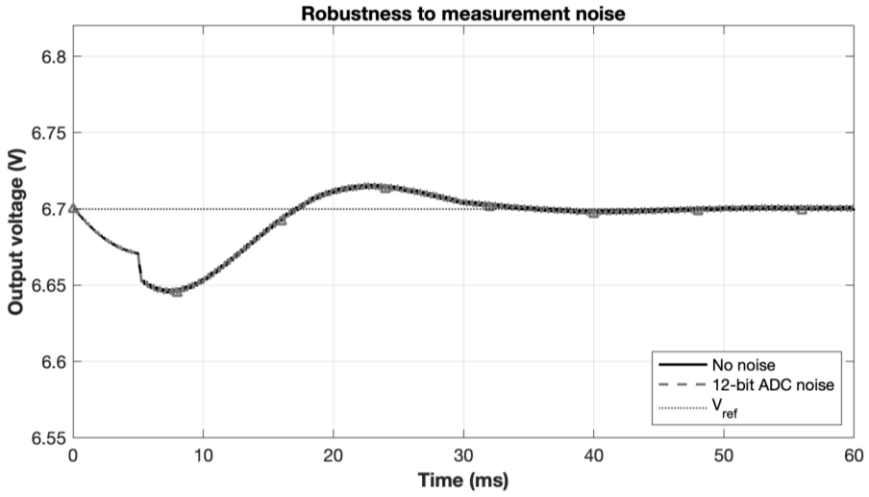


Figure 10. Output voltage response with and without 12-bit ADC measurement noise; the two traces are visually indistinguishable

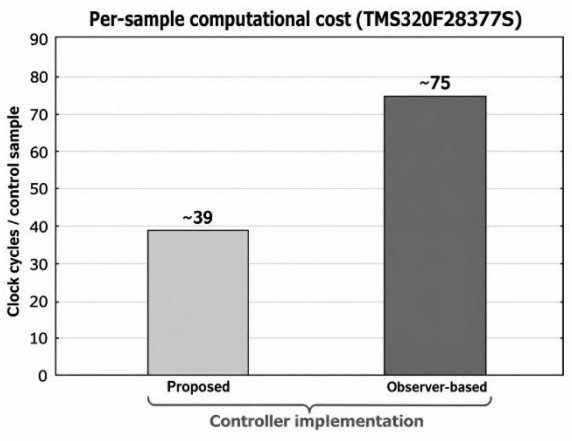


Figure 11. Per-sample computational cost on the target DSP: the proposed observer-free controller versus an observer-based sliding-mode controller

5.6. Renewable source-variation scenario

Under a prescribed renewable-like voltage trajectory applied to Source 1, comprising a gradual ramp and a partial-shading-like voltage dip (14.3 V to 11.5 V, 20–30 ms), together with a linear terminal-voltage drop of Source 2 (5.0 V to 4.6 V) — and with gains unchanged, the output held 6.7 V throughout, with a maximum transient deviation of 0.184% and post-transient ripple of 0.083% (Figure 12). This confirms that the mode-adaptive feed-forward tracks input variation within each control sample period without re-tuning, as required in hybrid renewable systems.

Although demonstrated on a dual-input stage, the control structure extends naturally to multi-port converters, a topology class of continuing interest in hybrid renewable-energy systems [32]. The outer voltage loop and inner sliding-mode current loop are independent of the number of inputs, and the time-division-multiplexing arbiter already sequences sources one at a time onto the shared inductor; adding a third input requires only an additional feed-forward branch, whose duty term follows the same volt-second-balance derivation. Because the feed-forward is algebraic and observer-free, its per-input cost is a small constant, so the computational footprint grows linearly rather than with the squared state dimension typical of observer-based multi-port schemes. A full three-input demonstration, including inter-port coupling and arbitration timing, is identified as future work.

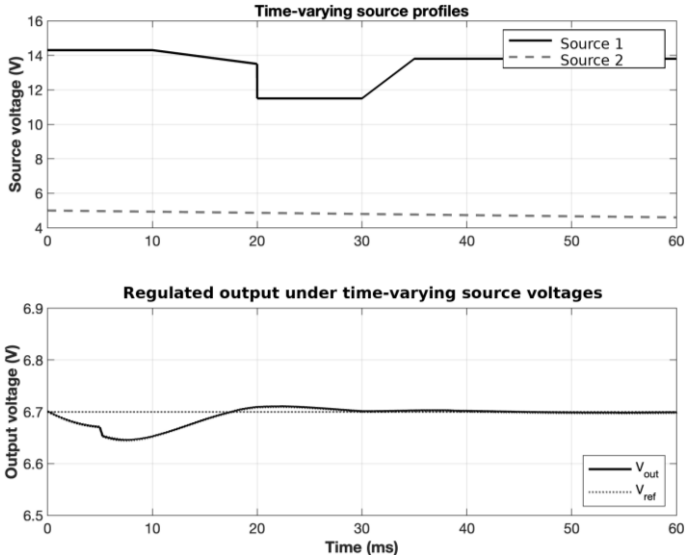


Figure 12. Regulated output under time-varying source-voltage variation and auxiliary-source terminal-voltage droop: (top) source voltage profiles; (bottom) regulated output voltage

5.7. Implications

The findings have three implications: Theoretically, the volt-second-balance feed-forward gives algebraic cancellation of matched source disturbances without an observer. Practically, the low computational complexity and observer-free design suit DSP implementation in cost-sensitive EV auxiliary power units, renewable microgrid interfaces, UPS backup converters, and motor drive front-end pre-regulators. Technologically, junction temperatures <28°C indicate that GaN-SiC pairing at 200 kHz offers thermal margin at this power level; fan-free operation remains to be confirmed on hardware [30]. Recent work on high-gain dual-input single-output topologies for hybrid energy systems [33] further underlines the practical relevance of these interfaces, whose multiport generalizations are well established [34]-[36].

5.8. Sensitivity and robustness analysis

To assess the practical robustness of the proposed controller, four single-parameter sweeps were performed about the nominal operating point of Table 3, covering switching-frequency variation (±10%), gate-drive transition time (0.5×–8× nominal), auxiliary-source internal resistance (0.05–0.80 Ω), and simultaneous passive-component drift under a 25 K junction-temperature rise. Throughout these tests, the controller gains were held at their tuned values (K_p = 3.50, K_i = 1200 and K_{sw} = 0.130), while only the parameter under investigation was varied to isolate its effect on closed-loop performance without re-tuning. Figure 13 presents the output-voltage ripple (solid traces, left axis) and conversion efficiency (dashed traces, right axis), while the corresponding results are summarized in Table 5.

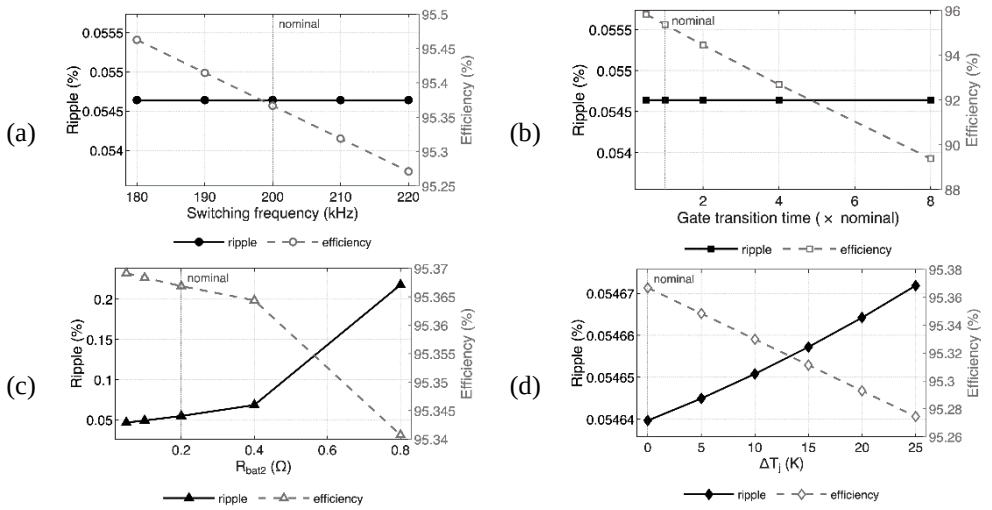


Figure 13. Sensitivity analysis of the proposed cascade controller: (a) switching frequency, (b) gate-drive transition time, (c) auxiliary-source internal resistance, and (d) passive-component drift. Solid and dashed lines represent output-voltage ripple and conversion efficiency, respectively

Table 5. Sensitivity study: extreme-case results

Condition	Ripple (%)	SS error (%)	Settling (ms)	Efficiency (%)
Nominal	0.0546	0.0011	2.285	95.367
f_{sw} = 180 kHz	0.0546	0.0011	2.285	95.463
f_{sw} = 220 kHz	0.0546	0.0011	2.285	95.271
Gate transition ×8	0.0546	0.0011	2.285	89.383
R_{bat2} = 0.80 Ω	0.2179	0.5409	3.255	95.341
ΔT_j = 25 K	0.0547	0.0012	2.040	95.274

5.8.1. Switching-frequency variation

The switching frequency was swept ±10% about the nominal 200 kHz while the control-update period was held at 5 μs, so that only the power stage — not the digital controller — was affected. Output ripple and steady-state error were invariant to four decimal places (0.0546% and 0.0011% throughout), and conversion efficiency varied only from 95.46% at 180 kHz to 95.27% at 220 kHz, the small monotone fall reflecting the increase in switching loss with frequency. Because the mode-adaptive feed-forward duty cycle of (6)-(8) depends only on measured voltage ratios and not on switching frequency, its compensating action is preserved across the entire range, and every regulation target of Table 3 is met.

5.8.2. Gate-drive transition time

The device rise and fall times were scaled from 0.5× to 8× their nominal values (35 ns and 18 ns) to represent a range of gate-drive strengths, which enter the switching-loss model. Output ripple and steady-state error were unaffected, while efficiency fell from 95.83% at 0.5× to 89.38% at 8×. Gate-drive strength therefore influences loss and thermal margin but not regulation quality, confirming that the controller is insensitive to this class of non-ideality even as the power-stage efficiency degrades.

5.8.3. Auxiliary-source impedance

The internal resistance of the auxiliary source, *R*bat2, was increased from 0.05 Ω to 0.80 Ω — up to four times its nominal 0.20 Ω — to probe the limit of the observer-free compensation. This is the most demanding test of the paper's central claim. Output ripple remained low and rose only gradually across the first three-to-fourfold increase, from 0.046% at 0.05 Ω to 0.068% at 0.40 Ω, with steady-state error held below 0.004% throughout this range. Beyond approximately 0.40 Ω, the current reference began to saturate against its limit for a significant fraction of the auxiliary-source conduction window, and regulation degraded more rapidly: at 0.80 Ω the ripple reached 0.218% and the steady-state error 0.541%. The feed-forward term thus provides effective algebraic compensation across a fourfold increase in source impedance, with a graceful rather than abrupt loss of regulation once the actuator authority is exhausted. This boundary constitutes a practical design guideline: the compensation holds provided the peak current demand at the highest expected source impedance remains within the converter's current limit.

5.8.4. Passive-component drift

To represent temperature-induced drift over a 25 K junction-temperature rise, the inductance was varied at +150 ppm/K (ferrite core), the output capacitance at −0.03%/K (polymer dielectric), and the inductor DC resistance at +0.4%/K, applied simultaneously. Across the full drift range, the output ripple remained within 0.0546–0.0547%, the steady-state error within 0.0011–0.0012%, and the efficiency between 95.27% and 95.37%. The controller gains, tuned at nominal temperature, retained their performance because the feed-forward terms re-evaluate from measured voltages every control period and are independent of the passive-component values.

Across all four studies, the proposed controller met its ripple, steady-state error, and settling-time targets under ±10% switching-frequency variation, an eightfold range of gate-drive transition time, and simultaneous passive-component drift over a 25 K rise. The one exception is the efficiency target of Table 3: at the extreme 8× gate-transition condition the simulated efficiency falls to 89.38%, below the 92% design target, although regulation quality is unaffected. This bounds the gate-drive strength required to preserve the efficiency specification rather than indicating a loss of control performance. The only condition under which regulation left its nominal band was a source-impedance increase beyond four times nominal, which exhausts the current-reference headroom; even there, the degradation is gradual and predictable rather than a loss of stability. These results confirm that the observer-free feed-forward compensation is robust to the principal power-stage and source non-idealities encountered in hybrid energy applications.

6. CONCLUSION

A cascade sliding mode controller with mode-adaptive feed-forward duty cycle has been designed, analyzed, and validated through model-based simulation for a dual-input single-inductor DC converter operating across buck and boost regions. The controller integrates an outer proportional-integral voltage regulator with an inner current sliding surface enforced by a boundary-layer saturation function, supplemented by a feed-forward term derived from steady-state volt-second balance that cancels input source impedance disturbances without observers.

Simulation results confirm output ripple of 0.044%, a steady-state voltage error of 0.003%, a current settling time of 2.79 ms, and conversion efficiency of 95.35% under ideal sources. With realistic source impedances of 0.05 and 0.20 Ω, the ripple penalty is below 0.02 percentage points, validating the observer-free compensation approach. Lyapunov analysis confirms reaching condition validity across 99.6% of the sampled state space. Comparison with PID, conventional sliding mode, and observer-based methods shows the proposed approach matches observer-based regulation accuracy while reducing computational complexity suitable for low-cost DSP implementation. A 500-run Monte-Carlo study confirms all targets are met across ±20% component tolerance; injected 12-bit measurement noise degrades the ripple by less than 0.001 percentage points, a photovoltaic-intermittency scenario holds the output within 0.184% of the reference; and the observer-free controller requires about 39 clock cycles per sample against 75 for an observer-based design.

Two limitations are acknowledged: i) Simulation-based validation — controller designed for real-time DSP execution, but hardware confirmation pending. PCB parasitics, EMI, and gate-drive delays may cause small deviations from simulated values; and ii) Two-input topology only — analysis covers dual-input converters; 3-input/multi-port extension beyond present scope.

Future work will pursue four directions: i) Hardware prototype with GaN-SiC pairing at 200 kHz to confirm simulation predictions; ii) Three-input topology extension for fault-tolerant hybrid energy systems; iii) Experimental validation under measured photovoltaic and energy-storage source profiles; and iv) Online thermal estimation for predictive fault detection in EV/UPS applications. Broader applications to motor drive front-ends and renewable interfaces will be addressed in subsequent work.

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C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

The authors declare no conflict of interest.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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