International Journal of Power Electronics and Drive System (IJPEDS)
Vol. 17, No. 3, September 2026, pp. 1794~1807
ISSN: 2088-8694, DOI: 10.11591/ijpeds.v17.i3.pp1794-1807

Adaptive internal model control-proportional integral for robust control of three-phase active front-end rectifiers

Azizah Abdul Razak[1], Norjulia Mohamad Nordin[1], Razman Ayop[1], Hazlina Selamat[1], Abobaker Kikki Abobaker[1], Nik Rumzi Nik Idris[1], Tole Sutikno[2,3]
[1]Faculty of Electrical Engineering, Universiti Teknologi Malaysia, Johor, Malaysia
[2]Department of Electrical Engineering, Faculty of Industrial Technology, Universitas Ahmad Dahlan, Yogyakarta, Indonesia
[3]Embedded System and Power Electronics Research Group, Yogyakarta, Indonesia

Article Info

Article history:

Received May 1, 2026
Revised Aug 8, 2026
Accepted Aug 14, 2026

Keywords:

Active front-end rectifier
Adaptive control
Cascaded control
Dynamic response
Internal model control
Lyapunov
Robust control

ABSTRACT

Three-phase active front-end (AFE) rectifiers are widely deployed in motor drives, electric vehicle chargers, and grid-connected renewable energy systems, where precise DC-link voltage regulation is essential for stable converter operation. In practice, DC-link capacitance degrades over time, and load profiles vary dynamically, both degrading the DC-link voltage regulation performance. Conventional proportional-integral (PI) outer voltage controllers are designed based on nominal operating conditions, with limited stability margins resulting in sluggish or oscillatory DC-link voltage responses under significant load and parameter variations. This paper proposes an adaptive internal model control-proportional integral (AIMC-PI) outer voltage loop controller for a three-phase AFE rectifier. It extends the conventional IMC-PI structure by incorporating an active damping term, an internal feedforward gain, a reference filter, and a Lyapunov-based adaptation law that updates the embedded plant model and IMC filter time constant online ensuring closed-loop stability and bounded tracking error. Simulation results show that AIMC-PI achieves a faster dynamic response than PI and performance comparable to IMC-PI and linear active disturbance rejection control (LADRC) under nominal conditions. As DC-link capacitance degrades to 0.5C, AIMC-PI maintains a well-damped DC-link voltage, whereas LADRC exhibits noticeable oscillations. Experimentally, AIMC-PI successfully eliminates the AC-supply current and DC-link voltage ripples present in fixed-λ IMC-PI.

Corresponding Author:

Norjulia Mohamad Nordin
Faculty of Electrical Engineering, Universiti Teknologi Malaysia
81310, Skudai, Johor, Malaysia
Email: norjulia@utm.my

1. INTRODUCTION

The DC-link voltage of an active front-end rectifier acts as an energy buffer between the AC supply and the DC-side load, and its regulation critically affects the performance of motor drives, electric vehicle chargers, vehicle-to-grid interfaces, and renewable energy and energy storage systems supplied by the rectifier [1]–[8]. In these applications, the rectifier is rarely operated at a fixed operating point: load profiles vary under dynamic conditions, the DC-link capacitor degrades over time, and system parameters drift over the converter lifetime. With the increasing integration of renewable energy sources and the rapid growth of electric vehicle adoption, active front-end rectifiers are increasingly required to provide tight DC-link voltage

regulation, low current total harmonic distortion, near-unity power factor, and reliable bidirectional power flow, even under wide operating ranges and conditions that cannot be fully anticipated at the design stage.

In voltage regulation, the most common control strategy for AFE rectifiers employs a cascaded control structure where an outer voltage loop regulates the DC-link voltage while inner current loops control the input currents. The two loops are intentionally decoupled in bandwidth, where the outer loop is set 10 to 50 times slower than the inner loop, while the inner loop is placed 10 to 20 times below the switching frequency to reject switching harmonics. In this structure, most disturbances like model mismatch and load variations manifest as DC link voltage fluctuations that are primarily corrected by the outer voltage controller, with the inner loop providing fast current shaping and damping. The traditional choice of a PI controller in the outer loop is attractive for its zero steady-state error under nominal conditions, but its bandwidth is fixed at the design operating point, therefore its response degrades when the operating point varies significantly [9]–[16].

Several control strategies have been proposed in the literature to compensate for this fixed-bandwidth limitation, such as integrating fuzzy logic to adaptively adjust PI gains under varying operating conditions. For example, [11] proposes a double fuzzy PI controller for the outer voltage loop of an AFE rectifier operating across a wide range of AC and DC voltages. The control structure combines a main fuzzy block that adjusts PI gains based on the DC-link voltage error and its rate of change with a sub fuzzy block that applies corrections based on the AC supply and DC reference voltages. Although this approach significantly improves both dynamic and steady-state performance, constructing two separate sets of membership functions and rule bases across multiple operating points demands extensive offline calculation, simulation, and experimental tuning, leading to implementation complexity in practice.

A second direction applies sliding mode control (SMC), valued for its fast dynamic response and strong robustness against parameter uncertainties and external disturbances [17]. However, conventional SMC suffers from chattering-high-frequency oscillations in the control signal that degrade performance. Study in [18] incorporates a fractional double power convergence rate in the inner loop to resolve the chattering issue without sacrificing robustness, achieving a fast dynamic response and low steady-state error. Despite these advances, existing approaches that simultaneously address chattering suppression, fast dynamic response, and steady-state accuracy still rely on complex algorithms, additional state variables, multiple tuning parameters, and increased real-time computation burden.

Another method that replaces the PI outer loop is active disturbance rejection control (ADRC), which lumps unmodeled dynamics, parameter variations, and external disturbances as a single disturbance term, estimated online by an extended state observer (ESO) and actively compensated by the control action. ADRC and its linearized version, linear active LADRC, improve the DC-link voltage dynamics and disturbance rejection over PI control [19], [20] and only require the plant's relative order and high-frequency gain, making them structurally simple and robust to model uncertainty.

However, ADRC performance depends on careful bandwidth and gain tuning, and on the accuracy of the disturbance estimation [21], and minimal plant information can be insufficient when the system has more complex dynamics [22]. Researchers in [22] address this by showing that LADRC is equivalent to a two-degree-of-freedom (2-DOF) IMC structure, in which the LADRC bandwidth tuning parameters correspond to the setpoint and disturbance-rejection filter time constant of IMC. This analysis provides a theoretical basis for the LADRC control behavior and suggests methods for incorporating additional plant dynamics to further enhance control performance.

Building on this IMC-LADRC equivalence, researchers in [23] proposed an enhanced LADRC scheme for servo systems that integrates IMC principles with active damping and SMC techniques. This approach resolves the inherent IMC trade-off between fast reference tracking performance and strong disturbance rejection. By adding active damping, disturbance rejection is improved without increasing controller order or bandwidth, while SMC improves robustness against uncertainties. The IMC-based tuning procedure also simplifies the design process, making LADRC easier to implement in practice. Although the IMC framework offers an attractive alternative to conventional PI tuning by taking advantage of the established IMC-PI equivalence and estimating disturbances from the mismatch between the plant and internal model [24], conventional IMC is still designed around a specific operating point, in the same way as PI control.

The internal plant model and the filter are both fixed at the design stage; for example, when the capacitance degrades or AC-side impedance drifts over the converter lifetime, the embedded model no longer matches the actual plant, and the disturbance estimate derived from the model is no longer accurate. Since λ remains fixed, this tradeoff cannot be adjusted online when the operating conditions change. The controller therefore must be tuned conservatively, which can limit either the dynamic response or the available robustness margin. Consequently, traditional IMC still suffers from a fixed-bandwidth limitation and therefore cannot consistently maintain the desired performance across the wide and time-varying operating conditions without incorporating an online adaptation mechanism.

To address these shortcomings of fixed-parameter PI and IMC, this paper proposes a hybrid cascaded control architecture for AFE rectifiers consisting of an adaptive internal model control–PI (AIMC-PI) outer voltage loop and a predictive deadbeat (PDB) inner current loop. The proposed outer loop differs from conventional IMC in four ways. First, active damping is incorporated into the IMC structure to improve disturbance rejection without increasing controller order or bandwidth. Second, an internal feedforward gain is added to enhance dynamic tracking. Third, a separate reference filter is incorporated, making the structure a two-degree-of-freedom (2-DOF) IMC so that tracking speed and disturbance rejection can be tuned independently rather than being coupled through a single λ. Fourth, instead of using fixed filter parameters, a Lyapunov-based adaptation law is employed to update both the embedded plant model and parameter λ online.

This ensures closed-loop stability and bounded tracking error while enabling the controller to adjust to real-time operating conditions, which cannot be achieved with fixed-λ IMC. Together, these modifications address parameter uncertainty, external disturbances, and operating point variations within the outer loop structure. Since this paper focuses on the outer voltage loop, the inner loop current is kept identical across all comparisons so that performance differences are attributed to the outer voltage loop alone. The proposed AIMC-PI/PDB scheme is validated by MATLAB/Simulink simulation under load changes, reference variations, and DC-link capacitance mismatch. The remainder of the paper is organized as follows: i) Section 2 presents the AFE rectifier model; ii) Section 3 details the AIMC-PI controller design; iii) Section 4 reports the simulation and experimental results and discussion; and iv) Section 5 presents the conclusion.

2. MODELLING OF ACTIVE-FRONT END RECTIFIER

A conventional three-phase AFE rectifier consists of input line inductors, a DC-link capacitor, and six bidirectional power switches, as illustrated in Figure 1. The line inductors and DC-link capacitor provide input current filtering and reduce the DC voltage ripple, respectively. During each switching cycle, the input inductors and DC-link capacitor continuously exchange energy, thereby regulating the source current and maintaining the DC-link voltage.

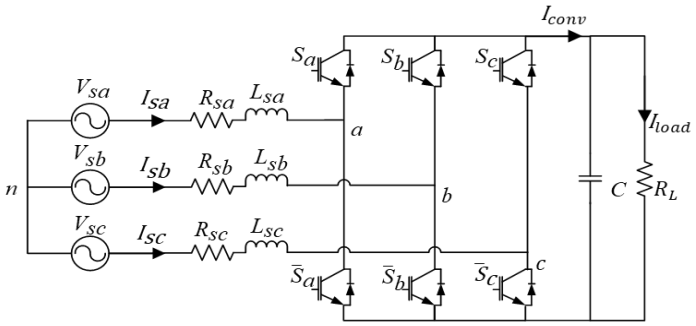

Figure 1. Three-phase AFE rectifier topology

In this design, the three-line inductors are assumed identical, including their equivalent series resistances (ESRs). Thus, the phase-a, phase-b, and phase-c inductances are set equal $L_{sa}=L_{sb}=L_{sc} = L_s$, and their corresponding series resistance are also set equal, $R_{sa}=R_{sb}=R_{sc} = R_s$. Furthermore, for the purpose of control design, the grid supply is modelled as a balanced, three-phase sinusoidal voltage source without harmonic distortion or unbalanced voltage. This assumption is a standard practice in AFE rectifier control design. Applying Kirchhoff's voltage law (KVL), the mathematical model of the three-phase AFE rectifier in the abc-frame could be derived as (1).

$$\begin{bmatrix} V_{sa}(t) \\ V_{sb}(t) \\ V_{sc}(t) \end{bmatrix} = R_s \begin{bmatrix} I_{sa}(t) \\ I_{sb}(t) \\ I_{sc}(t) \end{bmatrix} + L_s \frac{d}{dt} \begin{bmatrix} I_{sa}(t) \\ I_{sb}(t) \\ I_{sc}(t) \end{bmatrix} + \begin{bmatrix} V_{an}(t) \\ V_{bn}(t) \\ V_{cn}(t) \end{bmatrix} \quad (1)$$

Where V_{sa}, V_{sb}, V_{sc} are the three-phase source voltages, I_{sa}, I_{sb}, I_{sc} are the three-phase source currents, and V_{an}, V_{bn}, V_{cn} are converter phase voltages. By Kirchhoff's current law (KCL) at the DC-link node, the converter DC-side current can be expressed as (2).

$$I_{conv}(t) = I_{load}(t) + C\frac{dV_{dc}(t)}{dt} \quad (2)$$

Where I_{conv} is the converter DC-side current, I_{load} is the load current, C is the DC-link capacitance, and $\frac{dV_{dc}(t)}{dt}$ is the rate of change of the DC-link voltage.

3. OVERALL CONTROL ARCHITECTURE

The overall block diagram of the proposed control method is shown in Figure 2. The outer voltage loop regulates the DC-link voltage using the proposed Lyapunov-based AIMC-PI, in which an inner feedback gain pair improves both dynamic response and disturbance rejection, and an adaptive filter parameter λ provides robustness to plant uncertainties. In addition, a separate reference filter is also added after the reference input, allowing more control on reference tracking performance. The output of the outer loop serves as the d-axis current reference for the inner current loop, which is implemented using PDB control. The desired switching signals are generated using space-vector pulse width modulation (SVPWM) by synthesizing the converter output voltage, $\vec{V}_{ref}$.

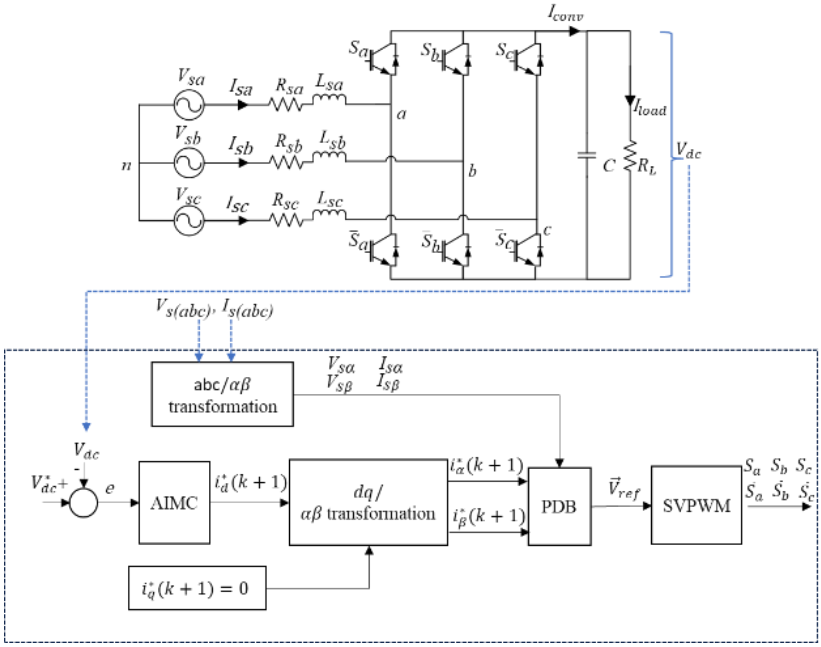

Figure 2. Overall block diagram of the proposed method

3.1. Outer voltage loop

This section presents the detailed design of the proposed Lyapunov-based AIMC-PI controller. The proposed method integrates: i) An IMC-PI structure with enhanced disturbance rejection and dynamic response via internal feedback and feedforward gains; ii) A separate reference filter is incorporated to improve tracking speed performance; and iii) Online plant parameter estimation using a Lyapunov-stable adaptation law and adaptive tuning of the IMC filter parameter λ, enabling self-tuning behavior.

3.1.1. IMC-PI

The IMC-PI structure offers the advantage of achieving zero steady-state error and effective disturbance rejection with a simple implementation, as illustrated in the IMC system block diagram in Figure 3. From the block diagram, the output to input relationship of the IMC is given by (3).

$$Y(s)/Y^*(s) = \frac{G_i(s)G_p(s)}{1-G_i(s)G_m(s)+G_i(s)G_p(s)} \quad (3)$$

While output to disturbance relationship of the IMC is given by (4).

$$Y(s)/V(s) = \frac{1-G_i(s)G_m(s)}{1-G_i(s)G_m(s)+G_i(s)G_p(s)} \quad (4)$$

Where the $G_m(s)$, $G_i(s)$, and $G_p(s)$ denote the model, inverse model, and plant transfer functions, respectively. To make $G_i(s)=1/G_{m(s)}$ realizable, a low-pass filter $F(s)=1/(\lambda s+1)^1$ is introduced. Because the plant has a pole at the origin that yields a sluggish response, an inner feedback gain k_f and an inner feedforward gain k_g are added, which provide active damping that improves disturbance rejection and improves transient response, respectively.

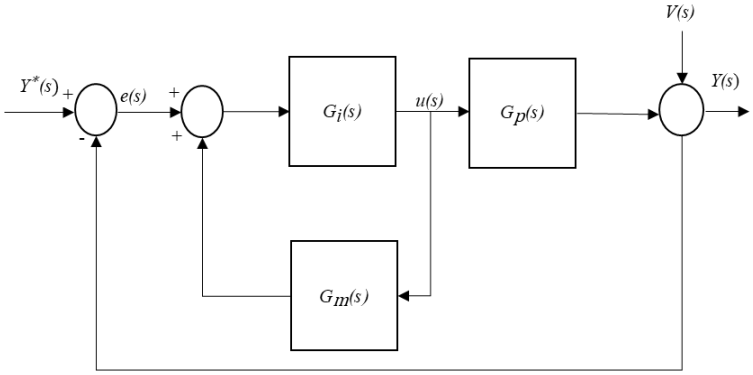

Figure 1. IMC block diagram

The model of the plant transfer function is given as (5).

$$G_m(s)=K_m/s \tag{5}$$

The compensated plant model, $G_{comp}(s)$ transfer function after introducing an inner feedback gain k_f and an inner feedforward gain, k_g as shown in Figure 4, is given by (6).

$$G_{comp}(s) = \frac{1}{k_f}\left(\frac{1}{\frac{1}{k_f}\frac{1}{K_m}\frac{1}{k_g}s+1}\right) = K_{m2}\left(\frac{1}{T_{m2}s+1}\right) \tag{6}$$

Using the pole placement method, the value of k_f is determined by placing the pole at the desired outer-loop bandwidth. Meanwhile, the value of k_g is selected to be 1.25 times lower than the value of the inner feedback gain. To ensure stability and proper outer-loop bandwidth separation, the value of k_g is chosen such that $k_g \leq \frac{\alpha_v}{k_m.k_f}$, where α_v represents the desired outer loop bandwidth.

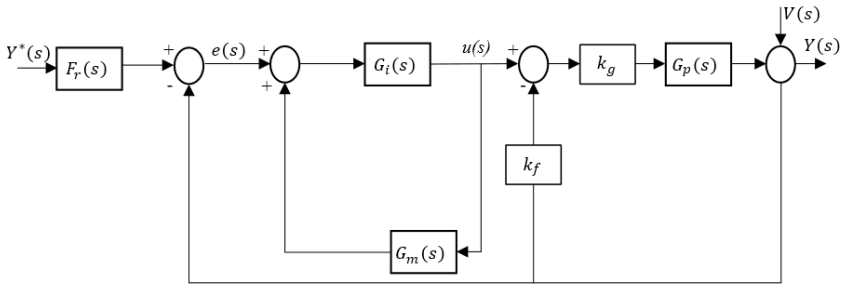

Figure 4. Closed-loop system with compensated process and setpoint filter $F_r(s)$

The equivalent controller transfer $G_c(s)$ function can be obtained as (7).

$$G_c(s) = \frac{G_i(s)}{1-G_i(s).G_{comp}(s)} \tag{7}$$

With $G_i(s)=\frac{1}{G_{comp}(s)}.F(s)$, thus, the proportional and integral gains can be expressed as (8).

$$K_p = \frac{\sqrt{a}}{\sqrt{\lambda . K_m}} \text{ and } K_i = \frac{1}{K_m . \lambda^2} \quad (8)$$

The adaptive filter parameter λ can be expressed as presented in (9) [10], [25].

$$\lambda = \lambda_0 (1 + \int_{tr}^{ts} |e| \frac{|e_m|}{[y_m]} dt) \quad (9)$$

The initial value λ_0 is selected as the minimum permissible value based on cascaded control design guidelines to ensure fast transient response while avoiding undesirable dynamic interaction between the inner and outer loops.

From (8) and (9), it can be observed that the controller gains K_p and K_i, are implicitly tuned as functions of both tracking error and modelling error. Here, the tracking error is defined as $e = y - r$, while the modelling error is defined as $e_m = y - y_m$, where y and y_m represent the outputs of the plant and the plant model, respectively, and r denotes the reference signal. Furthermore tr and ts denote the instants at which the adaptation of λ starts and stops. When either the tracking error or modelling error becomes large, the λ will also increase, which in turn reduces the controller aggressiveness against the model mismatch and unmodeled dynamics by reducing the IMC-PI gains, K_p and K_i. The $F_r(s)$ in Figure 4 is realised as a first-order low-pass filter,

$$F_r(s) = \frac{1}{\lambda_r(s)+1} \quad (10)$$

with $\lambda_r = \beta_R \lambda_0$, and where $\beta_r \geq 1$ sets the pre-filter bandwidth relative to λ_0.

3.1.2. First-order discrete-time identification model

In this paper, the plant is approximated by a first-order system to reduce the computational burden during online parameter identification. The discrete-time tunable plant model is expressed as (11).

$$\hat{y}(k) = -a_1 \hat{y}(k-1) + b_1 \hat{u}(k-1) = \hat{\theta}^T \emptyset(k) \quad (11)$$

Where $\hat{y}$ is the predicted model output, $\hat{u}$ is the model input, $\hat{\theta}$ is the estimated parameter vector, and $\emptyset(k)$ is the regressor. The index (k) denotes the current sampling instant, while $(k-1)$ denotes the previous sampling instant. The parameter vector and regressor are defined as (12).

$$\hat{\theta}^T = [a_1, b_1] \text{ and } \emptyset(k) = [y(k-1), u(k-1)] \quad (12)$$

3.1.3. Lyapunov-based adaptation law

In this section, the Lyapunov function is derived using a continuous-time representation to simplify the analysis, and for notational simplicity, time dependence (t) is omitted. Consider the first-order plant dynamics:

$$\dot{y} = -ay + bu \quad (13)$$

The corresponding estimated plant model is defined as (14).

$$\dot{y}_m = -a_m y_m + b_m u \quad (14)$$

The model estimation error is expressed as (15).

$$\dot{e}_m = [-ay + bu] - [-a_m y_m + b_m u] \quad (15)$$

Solving (15), the model estimation error is simplified:

$$\dot{e}_m = -a_m e_m - \tilde{a}\, y + \tilde{b} u \quad (16)$$

where $(a_m - a) = \tilde{a}$ and $(b - b_m) = \tilde{b}$ denote the parameter estimation errors. To derive the adaptation law for a_m and b_m, the Lyapunov candidate is defined as (17).

$$V = \frac{1}{2} {e_m}^2 + \frac{1}{2\gamma_a} \tilde{a}^2 + \frac{1}{2\gamma_b} \tilde{b}^2 \quad (17)$$

with $\gamma_a > 0$, $\gamma_b > 0$. To check Lyapunov stability, the next step is to differentiate the Lyapunov function with respect to time and examine the sign of its derivative along system trajectories:

$$\dot{V} = e_m \dot{e_m} + \frac{1}{\gamma_a}\tilde{a}\dot{\hat{a}} + \frac{1}{\gamma_b}\tilde{b}\dot{\tilde{b}} \quad (18)$$

Substituting (16) into (18) yields:

$$\dot{V} = -a_m {e_m}^2 - \tilde{a} e_m y + \tilde{b} e_m u + \frac{1}{\gamma_a}\tilde{a}\dot{\hat{a}} + \frac{1}{\gamma_b}\tilde{b}\dot{\tilde{b}} \quad (19)$$

To cancel the energy injection terms, set $\frac{1}{\gamma_a}\tilde{a}\dot{\hat{a}} = \tilde{a} e_m y$ and $\frac{1}{\gamma_b}\tilde{b}\dot{\tilde{b}} = -\tilde{b} e_m u$, yielding the continuous-time adaptation laws:

$$\dot{\hat{a}} = \gamma_a e_m y \text{ and } \dot{\tilde{b}} = -\gamma_b e_m u \quad (20)$$

Next is to substitute (20) into (19); consequently:

$$\dot{V} = -a_m {e_m}^2 \leq 0 \quad (21)$$

Since $\dot{V}(t) \leq 0$ is negative semi-definite, the Lyapunov function is non-increasing and bounded below by zero. Therefore $V(t)$ is bounded for all $t \geq 0$.

3.2. Inner current loop: predictive deadbeat controller

In this section, the predictive deadbeat current controller employed in the inner loop is described in detail. The current references i_d^* and i_q^* are provided by the outer voltage loop is assumed to be $i_d^*(k+1)$ and $i_q^*(k+1)$ respectively. These references in dq-frame are then transformed to the $\alpha\beta$-frame. By imposing the deadbeat condition $I_{s\alpha}(k+1) = I_{s\alpha}^*(k+1)$ and $I_{s\beta}(k+1) = I_{s\beta}^*(k+1)$ using the forward Euler approximation, the desired converter output voltages can be derived as (22) and (23).

$$\begin{aligned} V_{conv\alpha}^*(k) &= V_{s\alpha}(k) - \left(R_s \times I_{s\alpha}(k)\right) - \left(\frac{L_s}{T_s} \times \left(I_{s\alpha}^*(k+1) - I_{s\alpha}(k)\right)\right. \text{ and} \\ V_{conv\beta}^*(k) &= V_{s\beta}(k) - \left(R_s \times I_{s\beta}(k)\right) - \left(\frac{L_s}{T_s} \times \left(I_{s\beta}^*(k+1) - I_{s\beta}(k)\right)\right. \end{aligned} \quad (22)$$

$$\vec{V}_{ref} = (V_{conv\alpha}^* + jV_{conv\beta}^*), \text{and } \theta^* = \tan^{-1}\frac{V_{conv\beta}^*}{V_{conv\alpha}^*} \quad (23)$$

The desired converter voltage vector is synthesized by space-vector pulse-width modulation (SVPWM) at a constant switching frequency to generate switching pulses.

4. RESULT AND DISCUSSION

This section presents simulation and experimental results to validate the proposed AIMC control method under various operating conditions, including capacitance changes, load disturbances, and DC-link voltage reference changes. The simulation and experimental parameters are summarized in Table 1. The proposed AIMC-PI outer loop controller is benchmarked against three baseline controllers that share the same PDB inner loop current control: a conventional PI controller, fixed-λ IMC-PI, and LADRC. Controller performance is quantified using rise time and settling time. The evaluation proceeds in three stages: section 4. examines the dynamic response under nominal conditions, section 4.2 stresses the controllers with a DC-link capacitance mismatch of 0.5 C to assess robustness to capacitor ageing and tolerance, and section 4.3 validates the simulation findings on a hardware prototype of a three-phase AFE rectifier. In the proposed method, the bandwidth of the outer voltage loop is selected at 50 Hz, identical to those of the benchmark methods, ensuring a fair comparison. For the PI method, the outer voltage loop PI controller is designed by taking into account the dynamics of the inner loops; therefore, it is considered an optimal design [26]. The tuning parameters for all controllers are summarized in Table 2.

4.1. Dynamic response under nominal conditions

The dynamic performance of the proposed AIMC-PI control strategy is first evaluated under nominal system parameters and compared with the benchmark controllers. The evaluation considers the

ability of each controller to track changes and to reject load disturbances. In this test, the DC-link voltage reference is stepped from 180 V to 220 V at t = 0.2 s, while the load resistance is changed from 50 Ω to 100 Ω at t = 0.4 s. The corresponding DC-link voltage responses are shown in Figure 5, while the quantitative performance measures are summarized in Tables 3 and 4. As shown in Figure 5 and Table 3, the proposed AIMC-PI achieves a rise time of 22 ms, which is substantially faster than the conventional PI controller at 55 ms and slightly faster than the IMC-PI controller at 24 ms. Although LADRC provides the shortest rise time of 20 ms, the difference is relatively small.

The disturbance rejection performance is further evaluated by applying a load change at t = 0.4 s. As summarized in Table 4, the proposed AIMC controller restores the DC-link voltage to its reference value within 11 ms, compared with 15 ms for IMC-PI and 95 ms for the conventional PI controller. Although LADRC achieves the shortest settling time of 9 ms, the settling time of AIMC is only 2 ms longer, demonstrating a comparable disturbance-rejection capability. In contrast, the conventional PI indicates a sluggish recovery, highlighting its limited bandwidth under sudden load variations.

Table 1. Simulation parameters

Description	Value of parameter	
Input voltage (V_{LN})	55 (RMS)	V
Grid frequency	50	Hz
Load (R)	50	Ω
DC voltage	180	V
Capacitor (C)	850	μF
Input filter inductance (L_s)	6.45	mH
Input filter resistance (R_s)	0.094	Ω
Switching frequency (F_{sw})	10000	Hz
Sampling frequency (Ts)	10000	Hz
Power semiconductor devices	IGBT	-

Table 2. Tuning parameters for outer voltage loop controller

Method	Gain
PI	$K_p = 0.23$ $K_i = 6.85$
IMC-PI	$K_p = 0.718$ $K_i = 129.426$ $\beta_R = 2$
AIMC-PI	$K_p = 0.718$, $K_i = 129.426$ (initial value) $\beta_R = 2$ $\gamma_a = 0.2$, $\gamma_b = 300$
LADRC	$\omega_c = 50.2.\pi$, $\omega_o = 4.\omega_c$

Table 3. Rise time under nominal design parameters

Control method	Rise time (ms)
AIMC-PI	22
IMC-PI	24
LADRC	20
PI	55

Table 4. Settling time under nominal design parameters

Control method	Settling time (ms)
AIMC-PI	11
IMC-PI	15
LADRC	9
PI	95

Figure 6 shows the disturbance response when the DC-link voltage regulated at 180 V, with the load resistance changing from 50 Ω to 100 Ω at t=0.2 s under nominal conditions, with the corresponding settling times summarized in Table 5. Under this disturbance condition, IMC-PI (2.8 ms) exhibits a slightly faster voltage recovery than the proposed method (3.5 ms). This difference can be attributed to the adaptive mechanism of the proposed controller, in which both the embedded plant model and the λ are continuously adjusted according to the plant-model error, and the adaptation law needs time to converge before its updated parameters take effect.

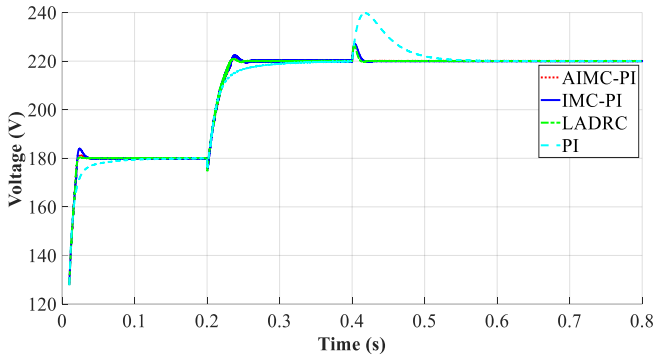

Figure 5. DC-link voltage response at nominal design parameters: reference step from 180 V to 220 V at t = 0.2 s and load step from 50 Ω to 100 Ω at t = 0.4 s

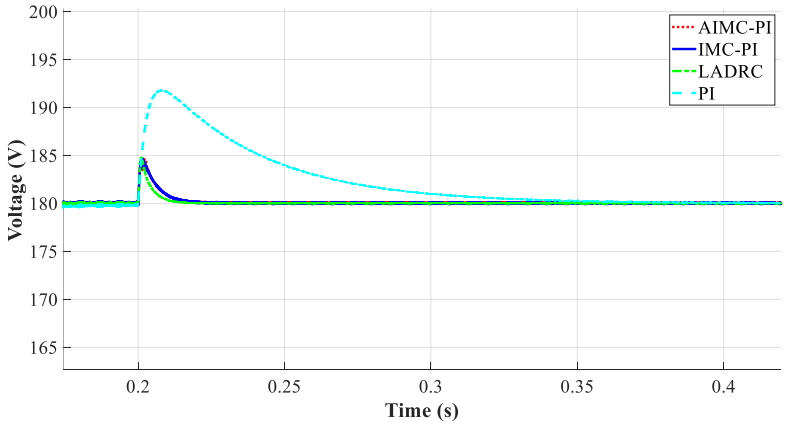

Figure 6. DC-link voltage response under nominal conditions: load step from 50 Ω to 100 Ω at t = 0.2 s, DC-link at 180 V baseline

Table 5. Settling time under nominal conditions: DC-link at 180 V baseline

Control method	Settling time (ms)
AIMC-PI	3.5
IMC-PI	2.8
LADRC	1.8
PI	53.3

4.2. Dynamic response under capacitance variations

To evaluate the robustness of the controller against DC-link capacitance uncertainties, the DC-link capacitance is reduced from its nominal value of 850 µF to 425 µF (0.5C). This represents a significant capacitance degradation and introduces a mismatch between the nominal controller design and the actual plant dynamics. As shown in Figure 7, the DC-link voltage reference is increased from 180 V to 220 V at t = 0.2 while the load resistance is changed from 50 Ω to 100 Ω at t = 0.4 s. Under these conditions, AIMC-PI, IMC-PI, and LADRC controllers maintain relatively fast voltage regulation based on rise times of 15 ms, 16 ms, and 14 ms, respectively, as summarized in Table 6.

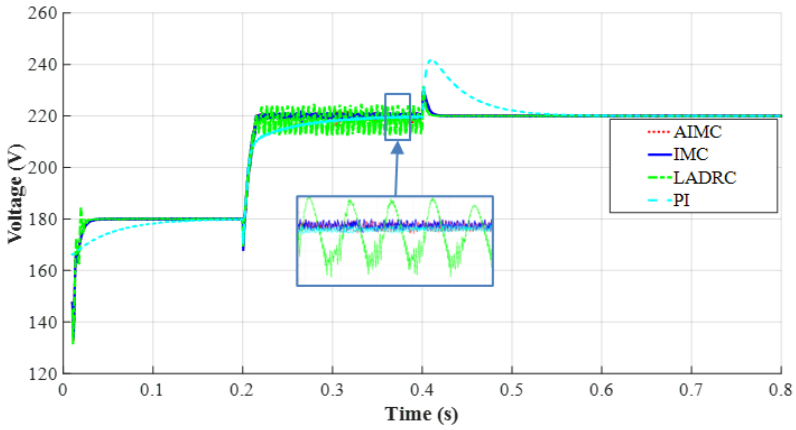

Figure 7. DC-link voltage response under capacitance degradation 0.5 C: reference step from 180 V to 220 V at t = 0.2 s and load step from 50 Ω to 100 Ω at t = 0.4 s

Although LADRC provides the fastest rise time, its response exhibits a noticeable voltage oscillation on the DC-link voltage during the reference change at t=0.2 s. In comparison, the proposed AIMC-PI achieves slightly slower response than LADRC but maintains smoother and well damped voltage trajectory. The IMC-PI controller also provides a comparable rise time of 16 ms with no oscillations, indicating that the IMC-based controllers are less sensitive to the capacitance variation. In contrast, the

conventional PI shows significant slower response in this case, with a 55 ms rise time. During disturbance rejection at t = 0.4 s, all three AIMC-PI, IMC-PI, and LADRC show comparable performance as detailed in Table 7, with LADRC, AIMC-PI, and IMC-PI settling times of 3.8 ms, 5.3 ms, 6.1 ms, respectively. The conventional PI requires 70.7 ms to settle, which is considerably longer than the other controllers.

Table 6. Rise time under capacitance mismatch

Control method	Rise time (ms)
AIMC-PI	15
IMC-PI	16
LADRC	14
PI	55

Table 7. Settling time under capacitance mismatch (0.5C)

Control method	Settling time (ms)
AIMC-PI	5.3
IMC-PI	6.1
LADRC	3.8
PI	70.7

4.3. Experimental validation

To further evaluate the practical implementation of the proposed control, an experiment has been implemented. The hardware experimental setup is shown in Figure 8. The prototype three-phase AFE rectifier comprises the line inductors, IGBT, gate driver, DC-link capacitor, load resistor, voltage and current sensing with their associated analog-to-digital converter (ADC) driver circuit, and a three-phase supply. The controller used in this experiment is a microcontroller (TMS320F28379D) to perform the control algorithm.

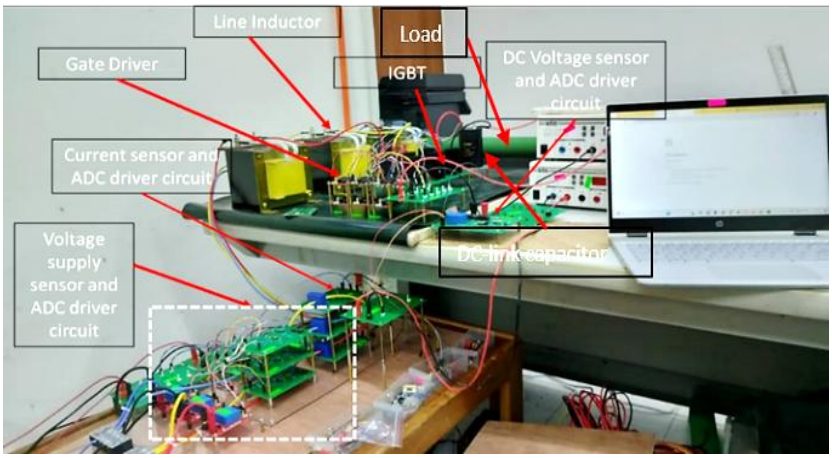

Figure 8. Experimental setup of the system

The first experimental condition evaluates the performance of the fixed-λ IMC-PI controller. The controller gains and parameters are selected consistently with those used in simulation. As shown in Figure 9, the fixed-λ IMC-PI exhibits significant ripple in three-phase AC supply currents. A corresponding ripple can also be observed in the DC-link voltage. This behavior may be caused by model or parameter mismatch between the actual hardware and the simulation model, noise from the voltage and current sensors, and the finite resolution and update latency of the digital PWM, which introduce a persistent mismatch between the assumed and actual plant dynamics that a fixed-λ and fixed embedded model cannot compensate for. The same tuning parameters are applied to the AIMC-PI controller to provide a consistent comparison with the fixed-λ. The experimental results are shown in Figure 10. Compared with the fixed-λ IMC-PI response in Figure 9, the proposed AIMC-PI controller significantly reduces the ripple in the three-phase supply currents, while the DC-link voltage exhibits a more stable and smoother response in steady-state conditions. These results demonstrate the effectiveness of the adaptive mechanism in improving the practical voltage regulation performance in real time. Nevertheless, a minor discrepancy exists between experimental and simulation results: at nominal capacitance, the measured rise time is 1.4x longer than the simulated value (Table 3). In the next scenario at 0.5C, the experimental result can be observed in Figure 11. The rise time value from the experiment is 23.28 ms compared to the simulation value of 15 ms (Table 6), which is 1.5 times longer than in the simulation. These discrepancies are primarily attributable to model mismatches between ideal simulation and physical converter setup, alongside digital control latencies such as ADC sampling and PWM update delays.

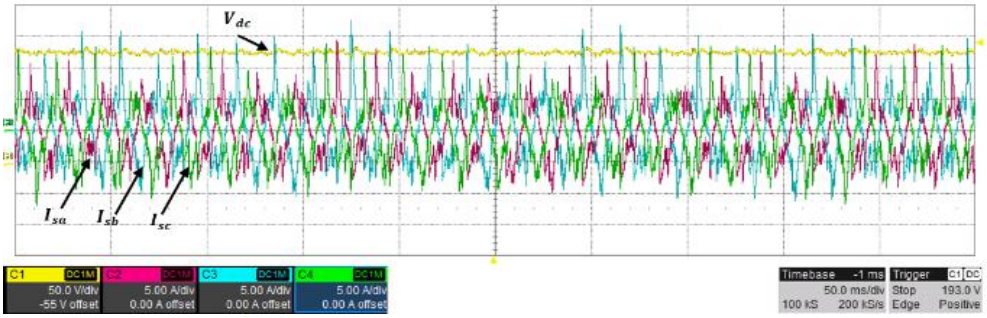

Figure 9. Experimental steady-state response of the fixed-λ IMC-PI controller under nominal operating conditions

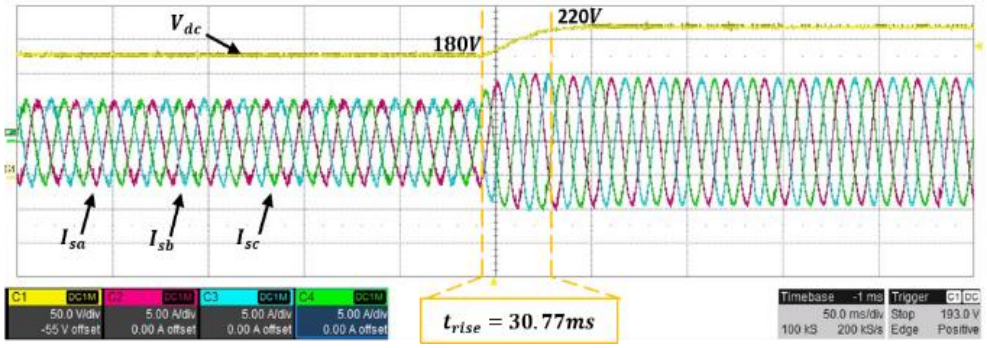

Figure 10. Experimental results of the dynamic response of AIMC when the reference changes from 180 V to 220 V at nominal design

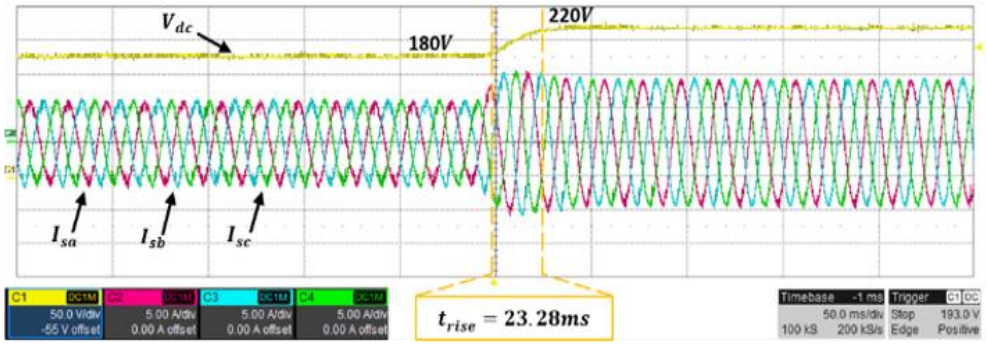

Figure 11. Experimental results of the dynamic response of AIMC when the reference changes from 180 V to 220 V at 0.5 C

5. CONCLUSION

This paper presented an adaptive internal model control-proportional integral and predictive deadbeat (AIMC-PI&PDB) control strategy for three-phase active front-end (AFE) rectifiers. By utilizing a Lyapunov-based adaptation mechanism, the outer-voltage loop dynamically updates its internal plant model and filter time constant, λ, in real time. Comparative evaluation against PI, fixed-λ IMC-PI, and LADRC methods demonstrates that the proposed AIMC-PI maintains fast disturbance rejection and strong voltage regulation under both nominal and severe capacitance degradation (0.5 C).

Hardware experiments validate that AIMC-PI effectively mitigates AC current and DC-link voltage ripples under fixed- λ IMC-PI control. A minor discrepancy in transient rise time was observed between simulation and hardware (1.4x and 1.5x under nominal and 0.5 C, respectively), driven primarily by physical model mismatch and digital control latencies. Addressing these implementation constraints to further improve transient performance will be the focus of future work.

FUNDING INFORMATION

Authors state no funding involved.

AUTHOR CONTRIBUTIONS STATEMENT

This journal uses Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
Azizah Abdul Razak	✓	✓	✓	✓	✓	✓		✓	✓	✓			✓	✓
Norjulia Mohamad Nordin	✓	✓		✓	✓	✓				✓		✓	✓	
Razman Ayop	✓	✓		✓	✓	✓				✓		✓		
Hazlina Selamat	✓	✓		✓	✓	✓				✓		✓		
Abobaker Kikki Abobaker	✓		✓	✓		✓				✓	✓			
Nik Rumzi	✓	✓		✓	✓	✓				✓				
Tole Sutikno					✓					✓	✓			

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

The data that support the findings of this study are openly available from the first author, [AAR], upon request.

REFERENCES

[1] H. Abu-Rub, S. Bayhan, S. Moinoddin, M. Malinowski, and J. Guzinski, "Medium-voltage drives: challenges and existing technology," *IEEE Power Electronics Magazine*, vol. 3, no. 2, pp. 29–41, Jun. 2016, doi: 10.1109/MPEL.2016.2551802.

[2] A. Sharma and S. Sharma, "Review of power electronics in vehicle-to-grid systems," *Journal of Energy Storage*, vol. 21, pp. 337–361, Feb. 2019, doi: 10.1016/j.est.2018.11.022.

[3] J. M. Carrasco *et al.*, "Power-electronic systems for the grid integration of renewable energy sources: a survey," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 4, pp. 1002–1016, Jun. 2006, doi: 10.1109/TIE.2006.878356.

[4] A. Colmenar-Santos, A.-R. Linares-Mena, J. F. Velázquez, and D. Borge-Diez, "Energy-efficient three-phase bidirectional converter for grid-connected storage applications," *Energy Conversion and Management*, vol. 127, pp. 599–611, Nov. 2016, doi: 10.1016/j.enconman.2016.09.047.

[5] M. S. Alam, M. Singh, and P. Agarwal, "Advancing V2G technology: design of an adaptive bi-directional three phase AFE converter for high-power applications," *Journal of Energy Storage*, vol. 92, 2024, doi: 10.1016/j.est.2024.112138.

[6] A. Zhaksylyk *et al.*, "Review of active front-end rectifiers in EV DC charging applications," *Batteries*, vol. 9, no. 3, p. 150, Feb. 2023, doi: 10.3390/batteries9030150.

[7] A. Haidar, J. Macaulay, and Z. Zhou, "Grid-connected bidirectional off-board electric vehicle fast-charging system," *Energies*, vol. 18, no. 22, p. 5913, Nov. 2025, doi: 10.3390/en18225913.

[8] J. R. Rodriguez, J. W. Dixon, J. R. Espinoza, J. Pontt, and P. Lezana, "PWM regenerative rectifiers: state of the art," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 1, pp. 5–22, Feb. 2005, doi: 10.1109/TIE.2004.841149.

[9] S. Borafker, P. Strajnikov, and A. Kuperman, "Design of dual-notch-filter-based controllers for enhancing the dynamic response of universal single-phase grid-connected power converters," *Applied Sciences*, vol. 13, no. 18, p. 10144, Sep. 2023, doi: 10.3390/app131810144.

[10] P. Chen *et al.*, "Adaptive internal model control based on parameter adaptation," *Electronics*, vol. 11, no. 23, p. 3842, Nov. 2022, doi: 10.3390/electronics11233842.

[11] W. Zhang, Y. Fang, R. Ye, and Z. Wang, "Analysis and design of a double fuzzy PI controller of a voltage outer loop in a reversible three-phase PWM converter," *Energies*, vol. 13, no. 15, p. 3778, Jul. 2020, doi: 10.3390/en13153778.

[12] I. Ben Ali, M. W. Naouar, and E. Monmasson, "Design of an active front-end rectifier controller with an accurate estimation for the dynamic of its deadbeat current control loop," *SN Applied Sciences*, vol. 2, no. 6, p. 1054, Jun. 2020, doi: 10.1007/s42452-020-2869-y.

[13] R. Nahavandi, M. Asadi, and J. M. Guerrero, "First-order integral switching surface sliding-mode control method of active front end rectifier for fast charger applications," *IET Power Electronics*, vol. 13, no. 17, pp. 3900–3909, Dec. 2020, doi: 10.1049/iet-pel.2020.0340.

[14] M. Israr and P. Samuel, "Performance improvement of front-end PFC controller with small DC-link capacitance for light EV charger applications," *Energy*, vol. 324, p. 135930, Jun. 2025, doi: 10.1016/j.energy.2025.135930.

[15] M. M. Ibrahim, L. Ma, Y. Zhao, S. Cheng, T. Bo, and H. Liu, "H∞ Loop shaping based on internal model current control structure for single-phase PWM rectifier," *Electrical Engineering*, vol. 106, no. 3, pp. 3217–3230, Jun. 2024, doi: 10.1007/s00202-023-02069-x.
[16] X. Liu, D. Wang, and Z. Peng, "Improved finite-control-set model predictive control for active front-end rectifiers with simplified computational approach and on-line parameter identification," *ISA Transactions*, vol. 69, pp. 51–64, Jul. 2017, doi: 10.1016/j.isatra.2017.04.009.
[17] C. Hisar, G. Balta, I. Sefa, and N. Altin, "Sliding mode-based active damping control of LCL-filtered three-phase PWM rectifier," *Arabian Journal for Science and Engineering*, vol. 50, no. 21, pp. 17845–17862, Nov. 2025, doi: 10.1007/s13369-025-10119-8.
[18] T. Wang, X. Li, J. Zhang, S. Chen, J. Ma, and C. Lin, "Fractional sliding mode observer control strategy for three-phase PWM rectifier," *World Electric Vehicle Journal*, vol. 15, no. 7, p. 316, Jul. 2024, doi: 10.3390/wevj15070316.
[19] M. Defdaf, D. Ziane, A. Chebabhi, S. Barkat, M. F. Benkhoris, and A. Kessal, "Enhanced linear state observer–based PLL-less vector-oriented control method for a three-phase PWM rectifier," *International Transactions on Electrical Energy Systems*, vol. 2024, no. 1, Jan. 2024, doi: 10.1155/etep/7191464.
[20] H. He, T. Si, L. Sun, B. Liu, and Z. Li, "Linear active disturbance rejection control for three-phase voltage-source PWM rectifier," *IEEE Access*, vol. 8, pp. 45050–45060, 2020, doi: 10.1109/ACCESS.2020.2978579.
[21] B. V. Martínez, J. Sanchis, S. García-Nieto, and M. Martínez, "Tuning rules for active disturbance rejection controllers via multiobjective optimization—a guide for parameters computation based on robustness," *Mathematics*, vol. 9, no. 5, p. 517, Mar. 2021, doi: 10.3390/math9050517.
[22] W. Tan and C. Fu, "Linear active disturbance rejection control: analysis and tuning via IMC," *IEEE Transactions on Industrial Electronics*, p. 1, 2015, doi: 10.1109/TIE.2015.2505668.
[23] P. Li, K. Guo, and M. Zhang, "Linear active disturbance rejection control of servo systems via IMC principle with active damping and sliding mode techniques," *ISA Transactions*, vol. 129, pp. 663–672, Oct. 2022, doi: 10.1016/j.isatra.2022.02.035.
[24] M. Morari, "Internal model control - theory and applications," *IFAC Proceedings Volumes*, vol. 16, no. 21, pp. 1–18, 1983, doi: 10.1016/S1474-6670(17)64183-1.
[25] H.-P. Huang, M.-L. Roan, and J.-C. Jeng, "On-line adaptive tuning for PID controllers," *IEE Proceedings - Control Theory and Applications*, vol. 149, no. 1, pp. 60–67, Jan. 2002, doi: 10.1049/ip-cta:20020099.
[26] F. Blaabjerg, *Control of power electronic converters and systems*. Academic Press, 2021.

BIOGRAPHIES OF AUTHORS

Azizah Abdul Razak received the B.Sc. degree in electrical engineering (computer) from UTHM (Universiti Tun Hussein Onn Malaysia), in 2006, and an M.Eng. degree in electrical power from UTM (Universiti Teknologi Malaysia) in 2018. She is currently pursuing her Ph.D. degree with the Department of Electrical Engineering at Universiti Teknologi Malaysia (UTM); her current research interests include power electronics and control systems. She can be contacted at email: azizah48@graduate.utm.my.

Norjulia Mohamad Nordin received her degree in Bachelor of Engineering in Electrical Engineering from the Universiti Teknologi Malaysia (UTM) in 2006 and a Master of Engineering Science (energy system) from the University of New South Wales in 2008. She then received her Ph.D. in Electrical Engineering from UTM in 2016. Currently, she is a senior lecturer at the Faculty of Electrical Engineering, Universiti Teknologi Malaysia (UTM). Her current research interests are in AC motor drives/electrical drives, bidirectional converters, wide-bandgap devices for power electronics converters, power electronic applications, electrical machines, and renewable energy conversion. She can be contacted at email: norjulia@utm.my.

Razman Ayop received his B.Eng. degree in electrical engineering with First Class Honors, M.Eng. degree in electrical engineering, and Ph.D. degree in electrical engineering from Universiti Teknologi Malaysia in 2013, 2015, and 2018, respectively. His research interests include renewable energy, power electronics, photovoltaic emulators, and maximum power point tracking converters. He can be contacted at email: razman.ayop@utm.my.

Hazlina Selamat received the B.Eng. degree in electrical and electronic engineering from Imperial College London, U.K., in 1998, and the M.Eng. and Ph.D. degrees in electrical engineering from Universiti Teknologi Malaysia (UTM) in 2000 and 2007, respectively. She is currently a professor and Professional Engineer at the Faculty of Electrical Engineering, UTM, and the former Director of the Control and Mechatronics Engineering Department. Her research interests include control system engineering, artificial intelligence, modelling and simulation, with applications in robotics, transportation, and biomedical systems. She has co-authored Malaysia's National Artificial Intelligence Roadmap 2021–2025 and serves as Malaysia's Focal Point for the ASEAN Sub-Committee on Microelectronics and IT. She received the Leaders in Innovation Fellowship from the U.K. Royal Academy of Engineering in 2017 and the US-ASEAN Science and Technology Fellowship in 2018. She can be contacted at email: hazlina@utm.my.

Abobaker Kikki Abobaker received the B.Sc. degree in electrical engineering from The College of Technical Sciences, Sabha, Libya, in 2002, and an M.S. degree in electrical engineering from Sam Higginbottom University of Agriculture, Technology and Sciences (SHUATS), Allahabad, India, in 2017. He is currently pursuing a Ph.D. degree at Universiti Teknologi Malaysia (UTM). He has taught courses in control engineering and electrical systems. He is also a full-time faculty member at The Higher Institute of Technical Sciences, Ghat. His research interests include model predictive control of power converters and drives. He can be contacted at email: kikki@graduate.utm.my.

Nik Rumzi received the B.Eng. degree in electrical engineering from the University of Wollongong, Wollongong, Australia, the M.Sc. degree in power electronics from Bradford University, Bradford, West Yorkshire, U.K., and the Ph.D. degree from Universiti Teknologi Malaysia, Skudai, Malaysia, in 1989, 1993, and 2000, respectively. He is a senior member of the IEEE and was a past chair (2014-2016) of the IEEE Power Electronics Malaysia Chapter. Currently, he is a professor at the Faculty of Electrical Engineering, Universiti Teknologi Malaysia, and an associate editor to the IEEE Transactions on Power Electronics. His research interests include AC drive systems and DSP applications in power electronic systems. He can be contacted at email: nikrumzi@fke.utm.my.

Tole Sutikno is a full professor in the Department of Electrical Engineering at Universitas Ahmad Dahlan (UAD) in Yogyakarta, Indonesia. He has held this position since 2023, having previously served as an associate professor from 2008. He earned his bachelor's degree from Universitas Diponegoro in 1999, his master's degree from Universitas Gadjah Mada in 2004, and his Ph.D. in Electrical Engineering from Universiti Teknologi Malaysia in 2016, where his doctoral research focused on advanced digital power electronics and intelligent control systems. From 2016 to 2021, he served as the Director of the Institute for Scientific Publishing and Publications (LPPI) at UAD, where he led initiatives to strengthen research visibility, journal management, and international collaboration in scholarly publishing. Since 2024, he has served as the head of the master's program in electrical engineering at UAD, following his leadership of the undergraduate program in electrical engineering in 2022. He is also the founding leader of the Embedded Systems and Power Electronics Research Group (ESPERG), which actively collaborates with both national and international institutions on topics such as fault-tolerant embedded systems, FPGA-based control, and renewable energy integration. He is widely acknowledged for his contributions to digital design, industrial electronics, motor drives, robotics, intelligent systems, and AI-based automation. His interdisciplinary research emphasizes practical deployments in industrial and healthcare contexts, covering FPGA applications, embedded systems, power electronics, and digital libraries. He has published 380 peer-reviewed articles in high-impact journals and conferences indexed by Scopus. As of 2025, Google Scholar indicates over 6,000 citations, with an h-index of 36 and an i10-index of 174. In recognition of his global research impact, he has been listed among the Top 2% of Scientists Worldwide by Stanford University and Elsevier BV from 2021 to the present, a distinction based on standardized citation metrics across all scientific disciplines. He can be contacted at email: tole@te.uad.ac.id.