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Efficiency improvement of single-phase asymmetric multilevel inverters

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ABSTRACT

This study evaluates the efficiency and harmonic performance of single-phase asymmetric cascaded multilevel inverters that use binary (1:2) DC source ratios to raise the output voltage-level count while reducing component count. Switching, conduction, harmonic, and control-circuit losses are quantified separately using datasheet parameters of a commercial IGBT (TO-247, 600 V, 40 A) at a power factor of 0.95. The sinusoidal switching angle technique ($\theta = \sin^{-1}(V_o/V_m)$) is evaluated at all levels, both with and without LC filtering. The 7-level design attains 74.79% efficiency with 8 switches, but the 11-level configuration achieves 74.96% efficiency with 12 switches. Total harmonic distortion (THD) decreases from 37.28% to 10.77% as levels rise with filtering. The 5-level design offers the best cost-to-performance balance, whereas the 7 and 11-level designs give the strongest efficiency gain per added switch.

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1. INTRODUCTION

Multilevel inverters (MLI) are highly significant parts of renewable energy systems, motor drives and grid-connected applications because to their improved harmonic performance and lower voltage stress on semiconductor devices [1], [2]. The MLI is a power-electronic circuit that can generate a specific alternating voltage output with different magnitude and frequency from a single direct current (DC) source or several lower-level DC inputs. The three-level converter is usually regarded as the basic structure that led to the development of this field [3]. The asymmetric cascaded H-bridge architecture produces a drastic improvement over conventional symmetric multilevel inverters in terms of increased number of voltage levels with less switching devices with the use of unequal DC source ratios. This arrangement provides better output voltage precision and at the same time reduces the complexity and cost of the system. It has been recently found that sinusoidal switching-angle approaches create high-quality output waveforms with negligible total harmonic distortion (THD) when paired with asymmetric DC voltage sources [4]. The appropriate modulation of the switching angle is necessary to reduce the harmonic distortion and to have efficient power conversion in asymmetric multilevel inverters [5], [6].

Standard multilevel topologies have intrinsic problems. Neutral-point-clamped inverters demand a quite high number of semiconductors switching devices, flying-capacitor schemes require active voltage balancing on their capacitors, and cascaded H-bridge topologies generally need more isolated DC sources as the number of levels increases [7], [8]. To overcome these issues, researchers have proposed several alternative topologies such as reduced-switch asymmetric structures, switched-capacitor boost inverters, and hybrid T-type designs, which achieve large level counts with a minimum amount of physical DC sources.

Despite this progress, most published work considers either symmetric configurations or single loss components in isolation, with relatively few works providing a switching-angle technique and a detailed device-level power loss analysis for the same set of asymmetric topologies.

This work addresses that deficiency in two complimentary ways. A detailed comparative analysis of power loss in 3, 5, 7, 9, and 11-level asymmetric cascaded multilevel inverters is presented initially. Realistic device specifications and operating conditions are used instead of ideal switches. Secondly, it advances the initial study by directly comparing the sinusoidal switching-angle technique at all voltage levels before and after LC filtering [9]. This comparison shows how much of the observed harmonic augmentation with increasing number of levels is attributable to the number of levels itself, rather than the switching-angle approach. The main goals of this extensive study are: i) To compute the four power loss components for five asymmetric MLI structures with minimal switch counts; ii) To assess the efficiency enhancements obtainable by increasing the level count through asymmetric structure; iii) To compare THD performance with and without LC filtering; and iv) To suggest practical, switch-count-conscious selection criteria based on efficiency, cost, and harmonic performance. This experiment uses commercial IGBTs and runs at a power factor of 0.95, typical for industrial motor-drive conditions. The novelty of this work, relative to the studies cited above, lies in combining for the same set of asymmetric topologies, a device-level four-component loss model (switching, conduction, harmonic, and control-circuit losses) with a direct comparison of the sinusoidal switching-angle technique before and after LC filtering; most prior studies address only one of these aspects, or a single loss mechanism in isolation. The resulting efficiency-versus-switch-count guidance is intended to help designers select an appropriate asymmetric MLI topology for low-power renewable-energy and motor-drive applications, where both efficiency and component count are constrained.

2. ASYMMETRIC MLI TOPOLOGY

2.1. Configuration principle of MLI

Asymmetric MLIs, unlike symmetric MLIs, employ non-uniform DC source voltages to achieve higher outputs with a smaller number of H-bridge cells [10] and different voltage ratios (often 1:2, 1:3, or 1:2:4). In this paper, we use a binary ratio (1:2) configuration to have a 7-level output with only 2 H-bridges (8 switches) instead of 3 H-bridges (12 switches) for a symmetric 7-level system. Similarly, 3 H-bridges are used to produce an 11-level output, instead of 5. Table 1 shows the circuit configuration for each asymmetric voltage level analyzed. The DC voltages for two-bridge systems are 12 V and 24 V, and 12 V and 24 V variants for three-bridge systems.

Table 1. Asymmetric MLI circuit configuration

Level	H-Bridge	N_{sw}	DC voltages	V_{out}(pk)	Level
3	1	4	12 V	±12 V	3
5	2	8	12 V, 12 V	± 24 V	5
7	2	8	12 V, 24 V	±36 V	7
9	3	12	12 V, 12 V, 12 V	±36 V	9
11	3	12	12 V, 12 V, 24 V	±48 V	11

2.2. Modulation strategy

The switching angle or conduction angle is an important parameter to generate the gating signals. The gating signals are used by the power switching devices of a multilayer inverter (MLI). This analysis defines the switching angle as the time during which each switch remains ON and OFF.

Through the sinusoidal switching technique, the conduction period between ON and OFF states can vary directly with the instantaneous value. The ideal switching points are derived from (1).

$$\theta = sin^{-1}(V_o / V_m) \quad (1)$$

V_o is the output voltage level at a certain angle, and V_m is the peak voltage level. This approach maintains the fundamental frequency at 50 Hz and reduces THD. The switching technique focuses on the zero-crossings of the reference sine wave. This is where the staircase approximation differs most from a true sinusoid [5].

3. POWER LOSS ANALYSIS METHOD

All computations are based on commercially available IGBTs that possess the following features. The asymmetric cascaded H-bridge multilevel inverter operates within a power range of 57 W to 304 W to get optimal output voltage levels with minimal component usage. It accomplishes this by employing

commercially available IGBT (TO-247, 600 V/40 A) switches with an asymmetric DC source ratio of 1:2. The subsequent critical electrical parameters were extracted from the datasheets: V_{ce}(sat) = 1.7 V, I_C = 20 A, r_{on} = 0.045 Ω (derived from V-I characteristics), Q_g = 120 nC total gate charge, and switching durations t_r = 0.45 μs and t_f = 0.60 μs [11].

Under these conditions, the H-bridges function with a DC link voltage 12 V, peak load current 10 A, power factor 0.95, load resistance 10 Ω, switching frequency 2000 Hz, average current of 3.025 A and root-mean-square (RMS) current 7.071 A. The total power loss of cascaded MLI can be written as (2).

$$P_{total} = P_{sw} + P_{con} + P_{harm} + P_{ctrl} \quad (2)$$

3.1. Switching loss calculation

Switching losses are due to the overlap of voltage and current during the turn-on and turn-off transition of the IGBTs [12], [13]. The energy dissipated in each switching is calculated as (3) and (4).

$$E_{on} = (1/6) \times V_{dc} \times I_{load} \times (t_{ri} + t_{fv}) \quad (3)$$

$$E_{off} = (1/6) \times V_{dc} \times I_{load} \times (t_{rv} + t_{fi}) \quad (4)$$

The integral of the voltage and current waveforms over the switching transition gives a factor of 1/6. The total switching power loss is (5).

$$P_{sw} = f_{sw} \times (E_{on} + E_{off}) \times N_{sw} \quad (5)$$

N_{sw} is the number of switches in total. The loss part scales linearly with the number of devices and the switching frequency.

3.2. Conduction loss calculation

The forward voltage drop of IGBTs consists of a constant threshold voltage and a resistive part [14], [15]. The model for the conduction loss is given by (6).

$$P_{con} = V_{ce}(sat) \times I_{avg} \times N_{sw} + r_{on} \times I^2_{rms} \times N_{sw} \quad (6)$$

The first term reflects the losses due to the steady voltage drop and relies on the average current. The second term denotes resistive losses and is proportional to the square of the RMS current.

3.3. Harmonic loss calculation

Harmonic currents elevate thermal energy in the load without providing beneficial output [16], [17]. In accordance with Parseval's theorem and IEEE Standard 519:

$$I_{fund} = I_{rms} / (1 + (THD/100)^2)^{1/2} \quad (7)$$

$$I_{harm} = (I^2_{rms} - I^2_{fund})^{1/2} \quad (8)$$

$$P_{harm} = I^2_{harm} \times R_{load} \quad (9)$$

The THD values included in these equations were derived using PSIM simulations, utilizing sinusoidal switching techniques, both with and without LC filtering.

3.4. Control circuit loss calculation

Control circuit power losses is the electrical energy that is wasted as heat. It arises from the gate drive and other auxiliary components. Gate drive power scales with the number of switches.

$$P_{gate} = Q_g \times V_{gate} \times f_{sw} \times N_{sw} \quad (10)$$

$$P_{elec} = Vcc \times I_{cc} \quad (11)$$

$$P_{ctrl} = P_{gate} + P_{elec} \quad (12)$$

For microcontrollers, sensors and communication circuits, V_{cc} is set to 12 V and I_{cc} to 0.5 A [18].

4. RESULTS AND DISCUSSION

4.1. Simulation by PSIM

PSIM software was employed to model all five asymmetric multilevel inverter setups. Figures 1 to 5 illustrate the schematic diagrams of the 3 to 11-level inverters. Table 2 delineates the length of each voltage level in electrical degrees for the seven voltage ranges produced at the output during a single cycle of 50 Hz power output, utilizing the 7-level arrangement with the sinusoidal switching-angle technique. The voltage waveforms produced by the sinusoidal switching-angle technique are depicted in Figures 6 through 10. Upon implementing the LC filter, the THD values are presented in Table 3.

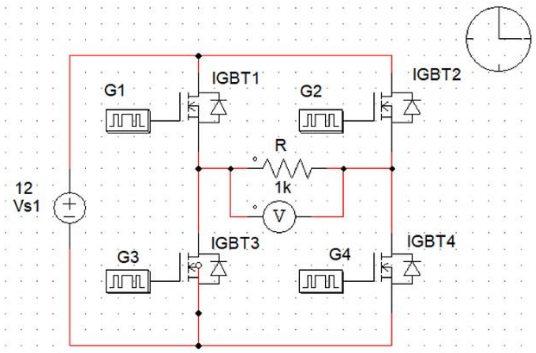

Figure 1. PSIM schematic, 3-level MLI

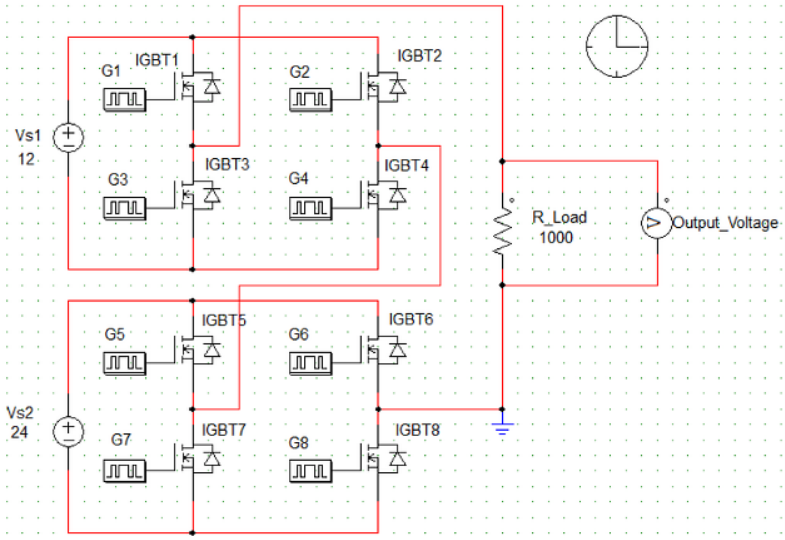

Figure 2. PSIM schematic, 5-level MLI

Table 2. Angle duration of the voltage step to create output voltages consisting of 7 levels in one cycle

Case No.	Angle	Bridge 1		Bridge 2		V_{out}
Case-1	0–30	1	2	5	6	0
Case-2	30–60	3	2	5	6	+12
Case-3	60–90	1	2	7	6	+24
Case-4	90–120	3	2	7	6	+36
Case-5	120–150	1	2	7	6	+24
Case-6	150–180	3	2	5	6	+12
Case-7	180–210	1	2	5	6	0
Case-8	210–240	4	1	5	6	-12
Case-9	240–270	1	2	8	5	-24
Case-10	270–300	4	1	8	5	-36
Case-11	300–330	1	2	8	5	-24
Case-12	330–360	4	1	5	6	-12

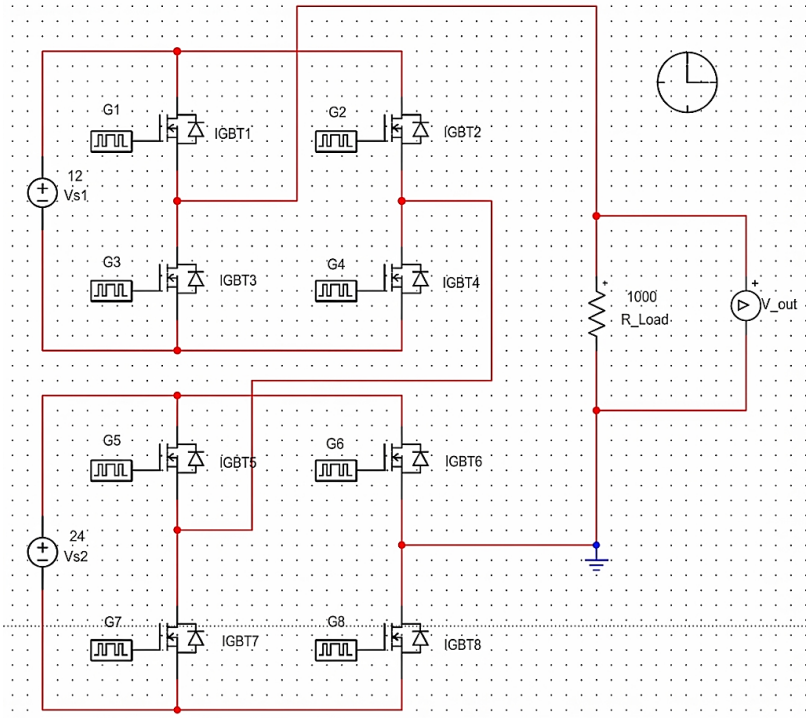

Figure 3. PSIM schematic, 7-level MLI

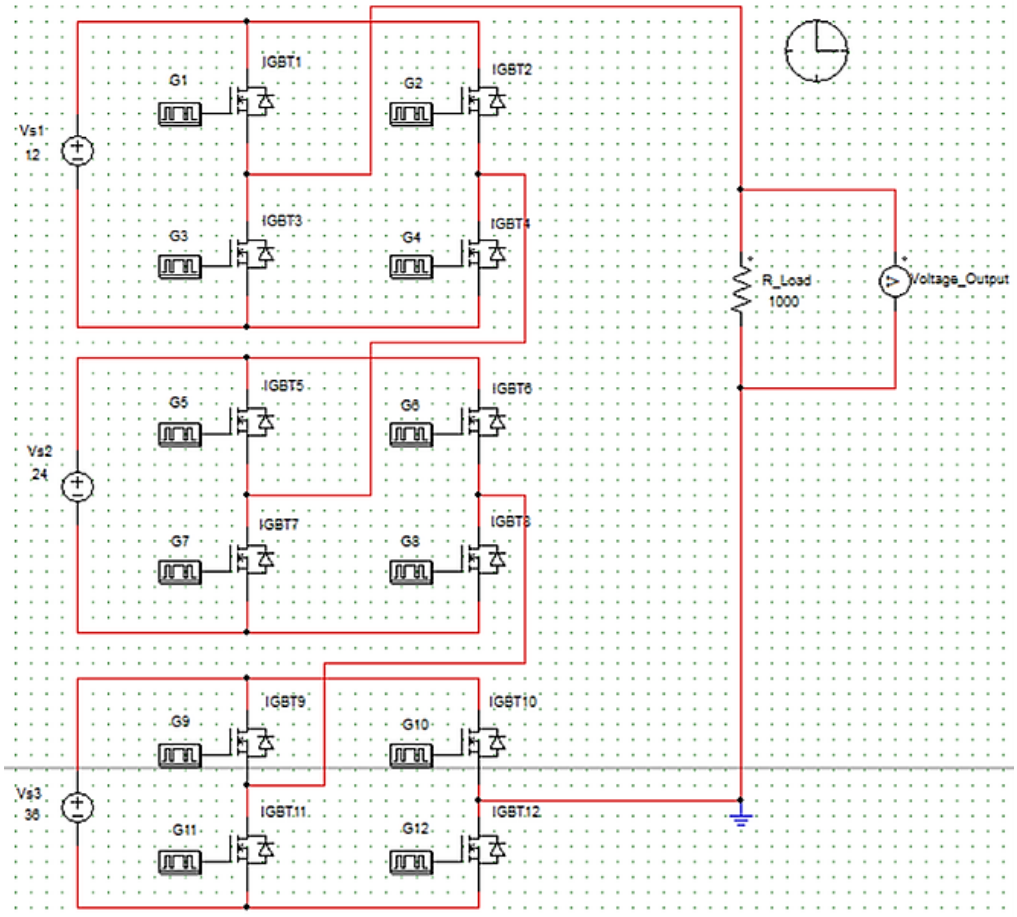

Figure 4. PSIM schematic, 9-level MLI

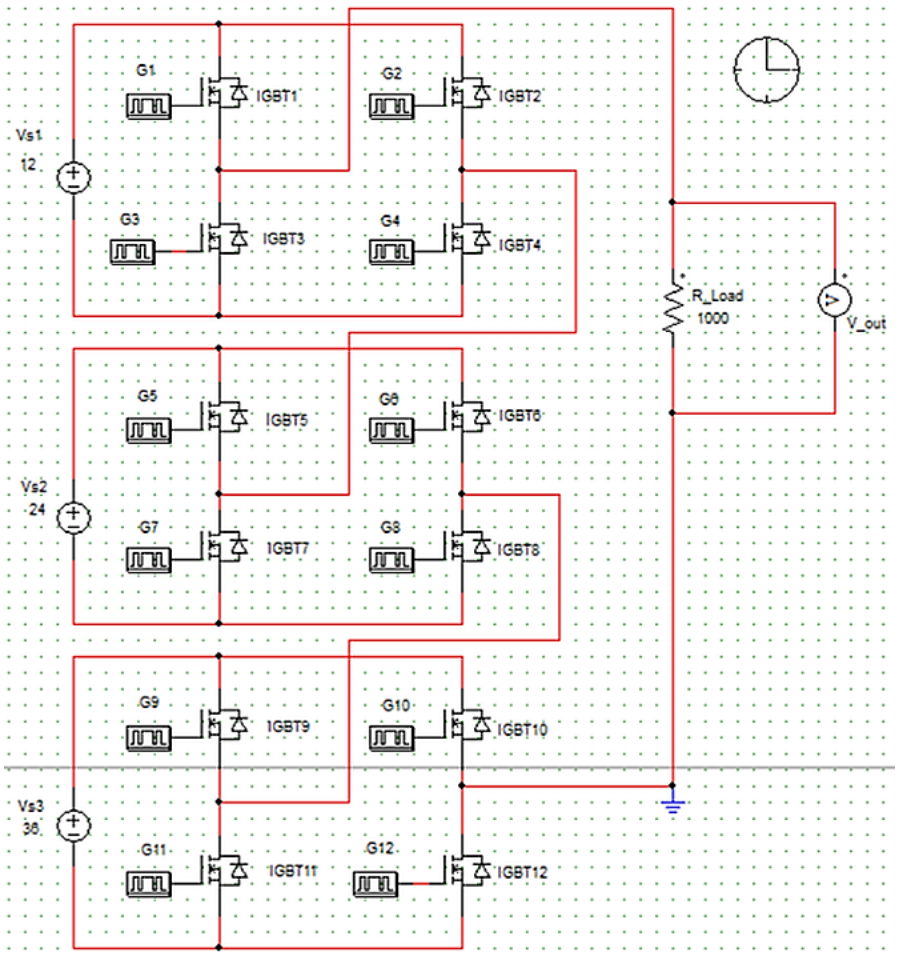

Figure 5. PSIM schematic, 11-level MLI

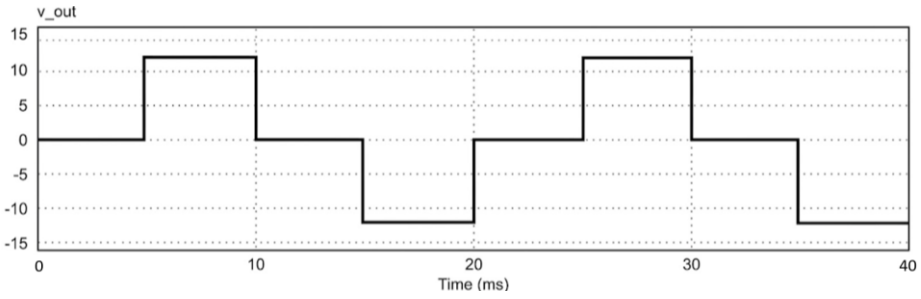

Figure 6. Output waveform, 3-level MLI

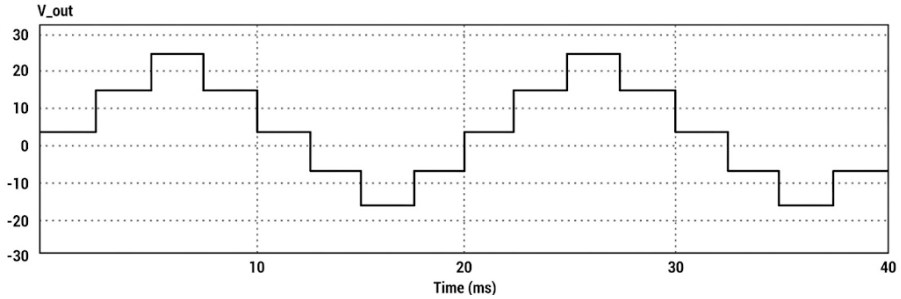

Figure 7. Output waveform, 5-level MLI

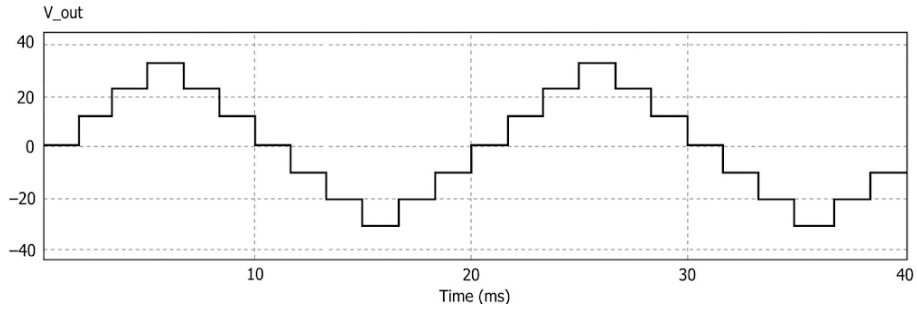

Figure 8. Output waveform, 7-level MLI

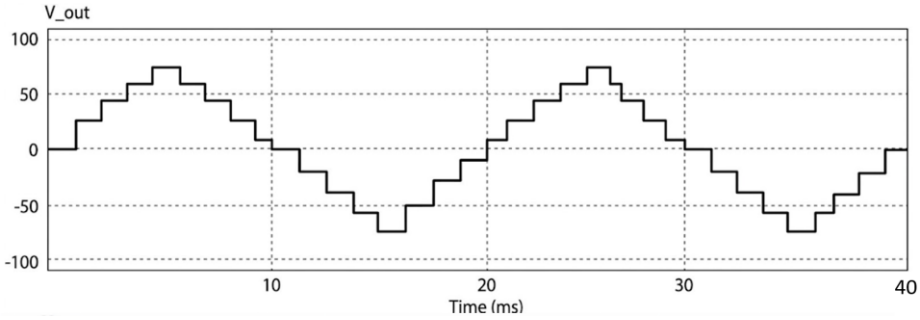

Figure 9. Output waveform, 9-level MLI

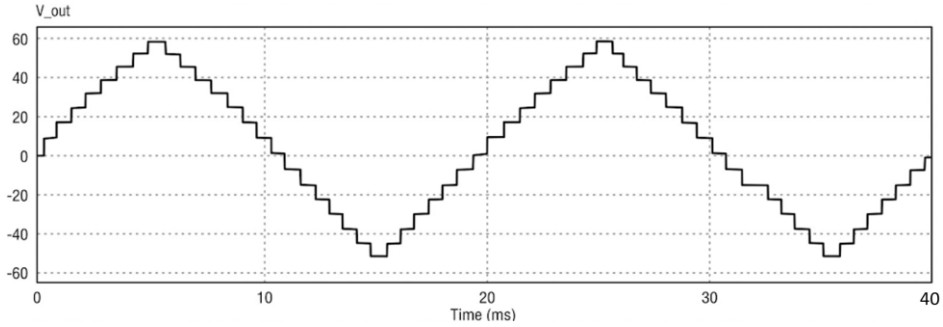

Figure 10. Output waveform, 11-level MLI

Table 3. THD comparison: without vs. with LC filter

Level	Without filter (%)	With LC filter (%)
3	37.28	36.18
5	19.88	18.68
7	15.49	14.98
9	14.15	13.88
11	13.98	10.77

4.2. Efficiency and power loss

Table 4 provides a detailed analysis of power loss for five asymmetric multilevel inverter topologies. These data show the performance of each configuration, based on requirements. With a power factor of 0.95 and LC filtering applied, Figure 11 shows how efficiency varies with the number of voltage levels. Efficiency rises sharply, from 37.83% for the 3-level configuration to 74.79% for the 7-level configuration, reflecting the substantial reduction in harmonic loss obtained by adding levels. The 7-level design also outperforms the 5-level design, achieving higher efficiency without an increase in switch count [19]. The 9-level configuration exhibits reduced harmonic loss but higher conduction loss, so its

net efficiency (68.43%) falls below that of the 7-level design. The 11-level configuration attains the highest efficiency (74.96%), owing to its larger output power and lower harmonic loss relative to the 9-level case [20]. Taken together, these results indicate that efficiency improves with increasing level count primarily through harmonic-loss reduction up to the 7-level design; beyond this point, conduction losses associated with the additional switches become the dominant factor limiting further efficiency gains.

Table 4. Complete power loss analysis (PF = 0.95, with Lc filter)

Level	N_{sw}	P_{sw} (W)	P_{con} (W)	P_{harm} (W)	P_{ctrl} (W)	P_{total} (W)	P_{out} (W)	η (%)
3	4	0.34	29.6	57.7	6.01	93.7	57	37.83
5	8	0.67	59.1	16.8	6.03	82.6	171	67.42
7	8	0.67	59.1	11.0	6.03	76.8	228	74.79
9	12	1.01	88.7	9.4	6.04	105.2	228	68.43
11	12	1.01	88.7	5.8	6.04	101.6	304	74.96

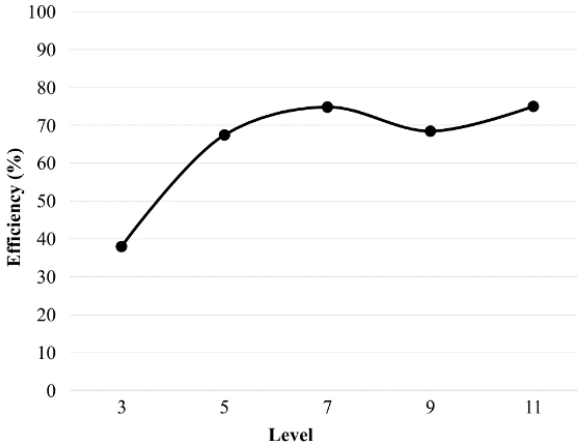

Figure 11. Level vs. efficiency

4.3. THD performance: without vs. with LC filter

Table 3 summarizes the effect of the sinusoidal switching-angle technique on total harmonic distortion (THD) across the five voltage levels, both without and with LC filtering. The results confirm that LC filtering reduces harmonic distortion at every level, although the magnitude of the reduction depends on the filter design and the number of voltage levels [21]. Table 3 and Figure 11 together indicate that harmonic-loss reduction is the primary driver of the efficiency improvement up to the 7-level design, after which conduction loss becomes the dominant limiting factor, consistent with the trend discussed in Section 4.2. With LC filtering, the 11-level configuration achieves the lowest THD (10.77%), a 22.96% reduction from its unfiltered value of 13.98% [22]; the 3-level configuration benefits least from filtering, with THD decreasing by only 2.95% (from 37.28% to 36.18%) [23]. Even without filtering, THD falls substantially as level count increases, from 37.28% at 3 levels to 13.98% at 11 levels, indicating that the staircase output waveform approaches a sinusoid as more levels are added. All configurations with seven or more levels achieve a filtered THD below 15% [24]. The 11-level design also reduces harmonic loss by 49% relative to the 9-level configuration, underscoring the combined benefit of a higher-level count and LC filtering for asymmetric multilevel inverter applications. These results support the conclusion that, at higher level counts, conduction loss rather than harmonic loss is the principal factor constraining efficiency [25].

5. CONCLUSION

In this work, an analytical power-loss framework combined with PSIM simulation was developed for 3, 5, 7, 9, and 11-level single-phase asymmetric cascaded H-bridge multilevel inverters. The sinusoidal switching-angle technique was implemented at all five levels. Efficiency and THD were evaluated both with and without LC filtering, directly addressing the gap between switching-angle studies and device-level loss analysis. Efficiency improves from 37.83% (3-level) to a peak of 74.96% (11-level), a gain of 37.13 percentage points, while the 7-level design (74.79% efficiency, 8 switches) offers a favorable balance between efficiency and switch count. THD with LC filtering falls from 36.18% (3-level) to 10.77% (11-

level). Harmonic-loss reduction is the dominant contributor to efficiency gains up to the 7-level design; beyond this point, conduction loss becomes the limiting factor, indicating that all four loss components. The present findings are based entirely on PSIM simulation and analytical loss modeling under a single operating condition (power factor 0.95, one switching frequency) and a single modulation strategy (sinusoidal switching-angle); no hardware prototype or experimental validation was performed, and comparison with published benchmark results was not included. These constraints limit the generalizability of the reported efficiency and THD values to other loading conditions, modulation schemes or component tolerances. Future work should include experimental validation on a hardware prototype under resistive, inductive, and nonlinear loads; comparison against symmetric multilevel inverters and alternative modulation strategies such as selective harmonic elimination and space-vector modulation; sensitivity analysis of component tolerances and DC-source imbalance; thermal and reliability assessment of the semiconductor devices. Extending the analysis to grid-connected, photovoltaic, and battery-energy-storage applications would further clarify the practical value of the proposed asymmetric MLI design approach.

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AUTHOR CONTRIBUTIONS STATEMENT

This journal uses Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

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C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author, [KMK], upon reasonable request.

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