DPC backstepping control applied to an active rectifier: analysis and comparison with a PIL implementation

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ABSTRACT

This paper presents a simulation and comparison of direct power control (DPC) and the new backstepping (BS) control for a three-phase PWM rectifier. The objective is to evaluate these techniques in achieving high-performance grid integration, targeting the absorption of sinusoidal current, maintaining a unity power factor, and minimizing grid current harmonics. While DPC is recognized for its fast dynamic response, it often suffers from high power ripples and variable switching frequency due to the switching table. Conversely, the proposed BS control provides superior tracking performance and improved stability margin, even under parameter uncertainties. Through detailed modeling and simulation in MATLAB/ Simulink environment, this paper analyzes key performance indicators, including current total harmonic distortion (THD), response time, and robustness, under multiple grid conditions, and validates the proposed control law using a processor-in-the-loop (PIL) implementation. The comparative study demonstrates the trade-offs between the two control methods, highlighting the advantage of backstepping control.

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1. INTRODUCTION

Power electronic converters, such as rectifiers, play a pivotal role across modern industrial applications, smart grids, renewable energy, and electric vehicles. However, conventional diode rectifiers act as a non-linear load that introduces several drawbacks, including distorted currents, harmonic content, and reactive power consumption. These power quality issues yield a low power factor (PF) and high current total harmonic distortion (THD). Such phenomena can damage grid equipment, introduce thermal stress in electrical machines, and destroy filtering capacitors [1]. To mitigate these drawbacks, we turn to the PWM rectifier with robust control strategies. PWM or Active rectifiers can be found in most modern applications, either as power supplies or power factor correction units [2].

The active AC-DC converters exhibit several advanced features, including low grid current distortion, bi-directional power flow, near-unity power factor, and stable DC-bus voltage using compact passive filters [1]-[4]. Various control strategies have been established in recent papers, notably hysteresis control (HC) and voltage-oriented control (VOC) [1], although these control methods can achieve the same main goals, their approach differ [5]. Over recent years, direct power control (DPC) has attracted substantial research interest

[6]-[7]. Modeled after direct torque control (DTC) techniques, employed in motor drive [5], DPC explicitly manages instantaneous active and reactive power components through decoupled control loops.

Unlike cascade architectures, conventional DPC eliminates inner current loops and the PWM modulator block, as the converter switching states are selected via a switching table. Switching states are selected based on the instantaneous power errors alongside the angular position of the grid voltage [6], [8] or virtual-flux vectors [8],[1]. Despite its simplicity, classical DPC exhibits some drawbacks, such as ripples in current and power, along with variable switching frequency, which may directly affect system performance and compromise stability [9].

Various control strategies have been proposed to improve DPC techniques and overcome its limitations; among these, the backstepping control (BS) technique, which we will combine with DPC to develop a robust and stable control technique against perturbations or parameter variation. The systematic, step-by-step synthesis offered by Backstepping control (BS) has made it a widely adopted approach for non-linear control applications [10], [11]. In this approach, virtual control laws are defined for lower-order subsystems, while the overall system stability is ensured by constructing a candidate Lyapunov function that aggregates the functions derived at each design step [12]. The backstepping control for DPC of a three-phase PWM rectifier was proposed by Rong et al in 2018 [12]; it was used to regulate the reactive power and DC-bus voltage of the rectifier. However, this method breaks down under varying load conditions [13] and relies on the sign function (13) and (15), which introduces the well-known chattering and high-frequency ripple. In contrast, the control law developed in this paper avoids the sign function, leading to smooth control action without chattering, while maintaining high performance under normal, unbalanced, and distorted grid conditions, as well as under parameter variations. In this paper, we take a step further by proposing a BS controller for DC voltage, active power, and reactive power to overcome the previous limitation. The control law is validated by a processor-in-the-loop (PIL) implementation.

This paper presents an improved DPC-backstepping strategy for a three-phase PWM rectifier. The main objectives are to maintain good performance under various disturbances, ensure unity power factor, and achieve low current THD (under 5%). The proposed control method aims to eliminate the classical switching table of DPC control [14]-[17] and the limitations of the previous DPC-BS approach. This study will compare DPC and DPC-BS, demonstrate the trade-offs between the two controls, and highlight the advantages of the proposed DPC-backstepping control.

2. THE PWM RECTIFIER

The active rectifier studied in this paper is based on three legs, each one consisting of two switches that contain an IGBT transistor with an antiparallel diode [18]-[21]. Figure 1 illustrates an active rectifier scheme, where e_a, e_b, e_c are AC grid voltages; R, L are the equivalent resistance and inductance of the grid; C is the DC bus capacitor; R_L is the load resistance; i_a, i_b, i_c are AC grid currents; I_{dc} is DC load current; and Vdc is DC load voltage. The coupling grid resistances (R) and grid reactance (L) are equal. Switching loss and on-state voltage are negligible, and the switching frequency is assumed to be high enough. Assuming a unity power factor, grid voltage and current are (1).

$$\begin{cases} e_a(t) = E_m.sin\,(\omega t) \\ e_b(t) = E_m.si\,n\left(\omega t - \frac{2\pi}{3}\right) \\ e_c(t) = E_m.\sin\,(\omega t - \frac{4\pi}{3}) \end{cases} \qquad \begin{cases} i_a(t) = I_m.sin\,(\omega t) \\ i_b(t) = I_m.si\,n\left(\omega t - \frac{2\pi}{3}\right) \\ i_c(t) = I_m.\sin\,(\omega t - \frac{4\pi}{3}) \end{cases} \tag{1}$$

Where E_m, I_m, ω, respectively, are the maximum simple voltage (V), the maximum grid current (A), and the angular frequency (rad/s).

From Figure 1, we can find:

$$[e]_{abc} = R.[i]_{abc} + L.\frac{d}{dt}[i]_{abc} + [v]_{abc} \tag{2}$$

By transforming (2) to the αβ reference frame, we obtain:

$$e_\alpha = Ri_\alpha + L.\frac{di_\alpha}{dt} + v_\alpha \tag{3}$$

$$e_\beta = Ri_\beta + L.\frac{di_\beta}{dt} + v_\beta \tag{4}$$

In this reference, active and reactive power (P and Q) can be expressed as (5) and (6).

$$P = e_\alpha . i_\alpha + e_\beta . i_\beta \quad (5)$$

$$Q = e_\beta . i_\alpha - e_\alpha . i_\beta \quad (6)$$

These equations are very important and form the foundation of the control theory being studied.

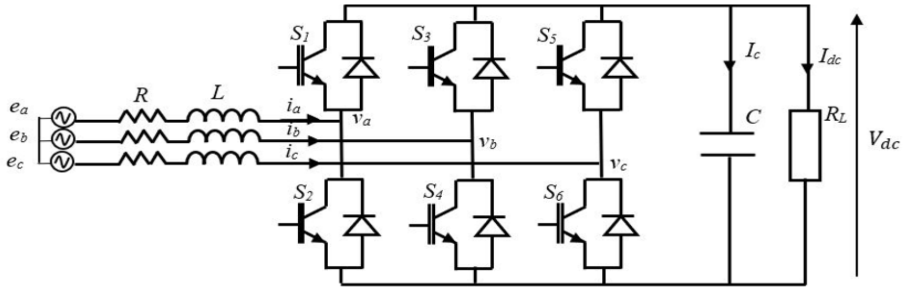


Figure 1. Active rectifier scheme

3. DESIGN OF BACKSTEPPING CONTROL

The backstepping technique provides a systematic and recursive method for designing nonlinear control laws, relying on Lyapunov functions to ensure the step-by-step stability of each synthesis step. At each stage of the process, virtual control inputs are generated to drive the system states towards their equilibrium state. This technique allows the synthesis of control laws while potentially considering disturbances or unfamiliarity with the system's parameters.

3.1. Backstepping control for the DC Bus

Our objective is to define the active power expression from the voltage reference. Based on Figure 1, using Kirchhoff's laws, we can find:

$$I = I_C + I_{dc} \quad (7)$$

With:

$$\begin{cases} I_C = C.\frac{dVdc}{dt} \\ I = \frac{P}{V} \end{cases} \quad (8)$$

Then, from (7) and (8), we can write:

$$\frac{dV_{dc}}{dt} = \frac{1}{C}.(\frac{P}{V_{dc}} - I_{dc}) \quad (9)$$

The steady-state error of the DC voltage is defined as (10).

$$\theta_1 = V_{ref} - V_{dc} \quad (10)$$

Now, a positive Lyapunov function with a negative derivative must be selected. This function, under these criteria, will ensure the system's stability without divergence; The Lyapunov theory is actually quite logical. If you have some function that is always decreasing, then it will reach zero eventually. So, there is no way that the system diverges: it must be stable.

The chosen candidate for the Lyapunov function is:

$$V_1 = \frac{1}{2}.\theta_1^2 \quad (11)$$

$$\frac{dV_1}{dt} = \theta_1.\frac{d\theta_1}{dt} \quad (12)$$

To ensure system stability, the Lyapunov function derivative must be negative; choosing $\frac{d\theta 1}{dt} = -K_1 \cdot \theta_1$ (where $K_1 > 0$) guarantees this system's convergence and stability. From (9) and (10), we have:

$$\dot{\theta}_1 = \dot{V}_{ref} - \dot{V}_{dc} \quad (13)$$

$$\dot{\theta}_1 = \dot{V_{ref}} - \frac{1}{C}.\left(\frac{P}{V_{dc}} - I_{dc}\right) = -K_1.\theta_1 \quad (14)$$

With $\dot{V}_{ref} = 0$ we can easily find the active power expression. This block will generate our power reference; the reactive power reference is null.

$$P_{ref} = V_{dc}.(K_1\theta_1.C + I_{dc}) \quad (15)$$

3.2. Backstepping for active and reactive power

The active and reactive power steady-state errors are:

$$\theta_2 = P_{ref} - P \quad (16)$$

$$\theta_3 = Q_{ref} - Q \quad (17)$$

In BS theory, the second Lyapunov function must be written as (18)-(20).

$$V_2 = V_1 + \frac{1}{2}.(\theta_2^2 + \theta_3^2) \quad (18)$$

$$\dot{V}_2 = \dot{V}_1 + \theta_2.\frac{d\theta_2}{dt} + \theta_3.\frac{d\theta_3}{dt} \quad (19)$$

$$\dot{V}_2 = -K_1\theta_1^2 - K_2\theta_2^2 - K_3\theta_3^2 < 0 \, ; \forall\theta \neq 0 \; and \; \forall Ki > 0 \quad (20)$$

The derivatives of the steady-state errors are (21) and (22).

$$\dot{\theta}_2 = \dot{P}_{ref} - \dot{P} \quad (21)$$

$$\dot{\theta}_3 = \dot{Q}_{ref} - \dot{Q} \quad (22)$$

According to (3)-(6), and by neglecting the grid resistance, the derivatives of the active and reactive powers are (23) and (24).

$$\dot{P} = \dot{e_\alpha}.i_\alpha + e_\alpha.\dot{i_\alpha} + \dot{e_\beta}.i_\beta + e_\beta.\dot{i_\beta} = -\omega \cdot e_\beta \cdot i_\alpha + \left(\frac{e_\alpha - v_\alpha}{L}\right) \cdot e_\alpha + \omega \cdot e_\alpha \cdot i_\beta + \left(\frac{e_\beta - v_\beta}{L}\right) \cdot e_\beta \quad (23)$$

$$\dot{Q} = \dot{e}_\beta.i_\alpha + e_\beta.\dot{i_\alpha} - \dot{e}_\alpha.i_\beta - e_\alpha.\dot{i_\beta} = \omega \cdot e_\alpha \cdot i_\alpha + \left(\frac{e_\alpha - v_\alpha}{L}\right) \cdot e_\beta + \omega \cdot e_\beta \cdot i_\beta - \left(\frac{e_\beta - v_\beta}{L}\right) \cdot e_\alpha \quad (24)$$

By rearranging these two equations, we will find:

$$\dot{P} = \omega \cdot (e_\alpha \cdot i_\beta - e_\beta \cdot i_\alpha) + \left(\frac{e_\alpha - v_\alpha}{L}\right) \cdot e_\alpha + \left(\frac{e_\beta - v_\beta}{L}\right) \cdot e_\beta = -\omega \cdot Q + \left(\frac{e_\alpha^2 + e_\beta^2 - e_\alpha \cdot v_\alpha - e_\beta \cdot v_\beta}{L}\right) \quad (25)$$

$$\dot{Q} = \omega \cdot (e_\alpha \cdot i_\alpha + e_\beta \cdot i_\beta) + \left(\frac{e_\alpha - v_\alpha}{L}\right) \cdot e_\beta - \left(\frac{e_\beta - v_\beta}{L}\right) \cdot e_\alpha = \omega \cdot P + \left(\frac{e_\alpha \cdot v_\beta - e_\beta \cdot v_\alpha}{L}\right) \quad (26)$$

Substituting (25) and (26) into (21) and (22), we will have:

$$\dot{\theta}_2 = \dot{P}_{ref} + \omega \cdot Q - \left(\frac{U^2 - (e_\alpha \cdot v_\alpha + e_\beta \cdot v_\beta)}{L}\right) = -K_2 \cdot \theta_2 \quad (27)$$

$$\dot{\theta}_3 = 0 - \omega \cdot P - \left(\frac{e_\alpha \cdot v_\beta - e_\beta \cdot v_\alpha}{L}\right) = -K_3 \cdot \theta_3 \quad (28)$$

With $U^2 = e_\alpha^2 + e_\beta^2$. Finally, from the previous equations, we can find that our control signals are:

$$v_\alpha = \frac{L}{U^2}.\left[-K_2 \cdot \theta_2 \cdot e_\alpha - K_3 \cdot \theta_3 \cdot e_\beta + \omega \cdot P \cdot e_\beta - e_\alpha \cdot \left(\dot{P}_{ref} - \frac{U^2}{L} + \omega \cdot Q\right)\right] \quad (29)$$

$$v_\beta = \frac{L}{U^2} \cdot \left[-K_2 \cdot \theta_2 \cdot e_\beta + K_3 \cdot \theta_3 \cdot e_\alpha - \omega \cdot P \cdot e_\alpha - e_\beta \cdot \left(\dot{P}_{ref} - \frac{U^2}{L} + \omega \cdot Q\right)\right] \quad (30)$$

The (20) ensures system stability if K_1, K_2, and K_3 are all positive gains.

3.3. DPC-Backstepping control scheme

To understand the implementation of the controller, Figure 2 illustrates the block diagram of the backstepping control. This diagram highlights the integration of the backstepping law within the active rectifier system. The PWM generator produces the six pulses required to control the six electronic switches of the active rectifier.

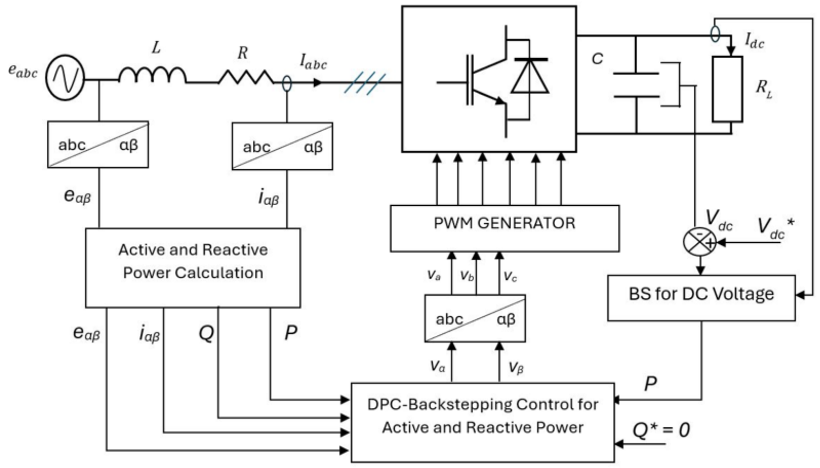


Figure 2. DPC-backstepping block diagram

4. SIMULATION RESULTS

To demonstrate the effectiveness of our DPC-backstepping control strategy, we use the MATLAB/Simulink environment. This robust and reliable simulation tool will demonstrate, through simulation, the performance of the proposed control. The simulation scenario begins with a reference DC voltage of 700 V; after one second, the reference is stepped up to 800 V; finally, it is stepped down to 600 V with a switching frequency of 50 kHz. The main objective of these transitions is to analyze the system's behavior during transient change and examine the evolution of the grid current and its corresponding THD, the power factor, and the active and reactive power. To compare, through simulation, the conventional DPC control with the DPC-backstepping control and identify the advantages that the proposed controller offers, and determine any potential limitations it may have compared to conventional DPC, we will impose different scenarios in which we want to evaluate the optimal performance of each control strategy.

4.1. The system's parameters

The system is simulated using the parameters listed in Table 1. The chosen parameters are widely adopted in the literature [22]-[25] to reflect realistic operating conditions. These parameters define the electrical and control conditions of the active rectifier.

Table 1. System's parameters

Parameter	Symbol	Value	Parameter	Symbol	Value
DC voltage	V_{dc}	600 to 800 V	Grid resistance	R	0.1 Ω
Grid voltage (RMS)	e_q	230 V	DC bus capacity	C	2 mF
Grid frequency	f	50 Hz	Load resistance	R_L	50 Ω
Grid inductance	L	5 and 10 mH	Sampling frequency	fs	50 kHz

4.2. Simulation results of DPC and DPC-BS under balanced Grid with L = 5 mH

In this simulation, we will analyze the behavior of the control strategies under optimal and normal grid conditions. The system performs optimally with a grid inductance (L) of 5mH, which represents the optimal operating condition considered in this study. The simulation results of our system under the MATLAB/Simulink environment are presented in Figures 3–6.

Based on the presented simulation results, both control strategies demonstrate good performance as shown in Figure 3; the DC-Bus voltage tracks its reference accurately with a negligible steady-state error. Overall, DPC-BS control exhibits a faster dynamic response, lower overshoot, less noisy current (1.76% vs 3.37%), and near-zero reactive power absorption. Conversely, DPC control provides a smoother current response, while DPC-BS generates spikes during transient changes (Figure 4) due to the power derivative term in the control law. However, these spikes are rapidly damped by the proposed controller. Both strategies meet our key objective; however, DPC-BS control provides superior THD performance because DPC absorbs a small amount of reactive power (Figure 5). Furthermore, under normal conditions, the grid currents exhibit excellent sinusoidal behavior and are in phase with their corresponding grid voltage (Figure 6).

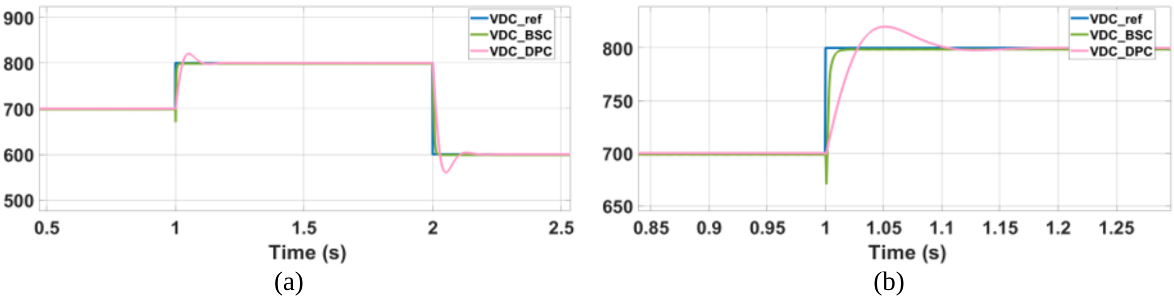


Figure 3. DC-Bus voltage response: (a) overall response and (b) transient step of Vdc voltage

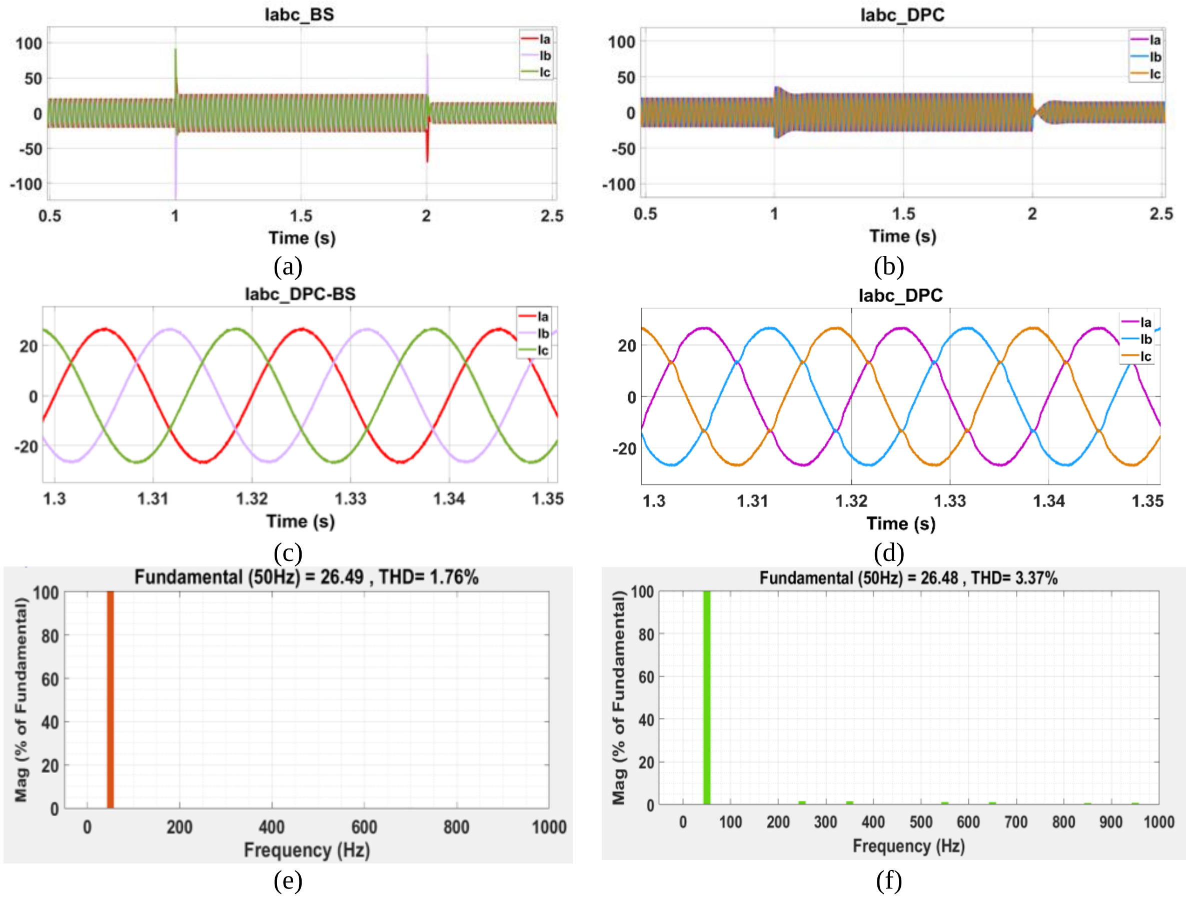


Figure 4. Grid current and THD comparison of DPC-BS and DPC controls: (a) DPC-BS grid current, (b) DPC grid current, (c) zoomed-in DPC-BS grid current at 800 V Vdc, (d) zoomed-in DPC grid current at 800 V Vdc, (e) DPC-BS current THD (1.76%), and (f) DPC current THD (3.37%)

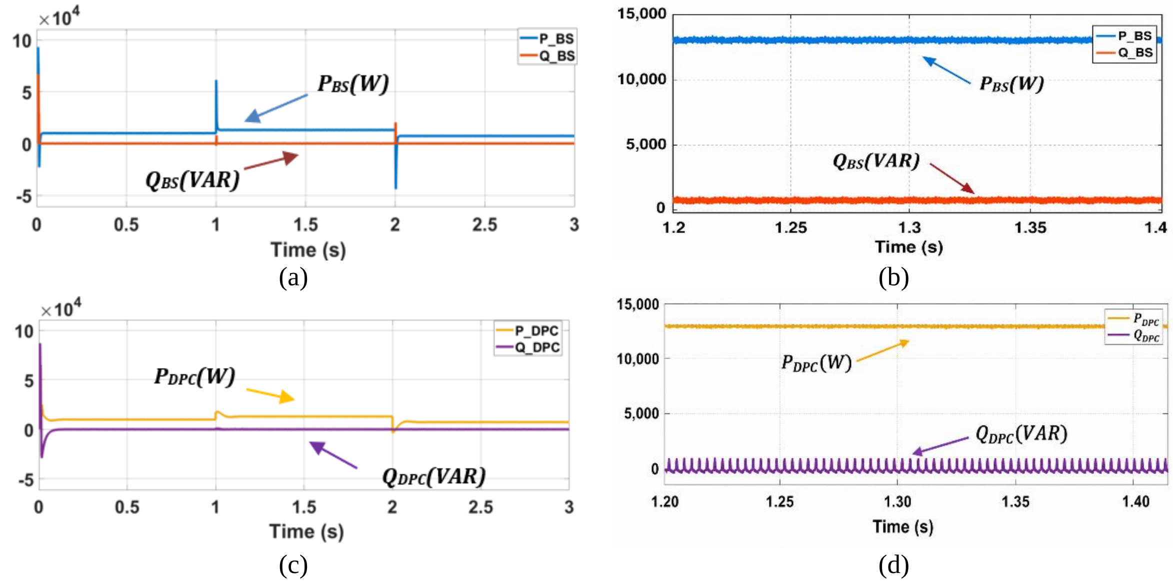


Figure 5. Active and reactive power response: (a) overall response (DPC-BS), (b) zoom of the active and reactive power (DPC-BS), (c) overall response (DPC), and (d) zoom of the active and reactive power (DPC)

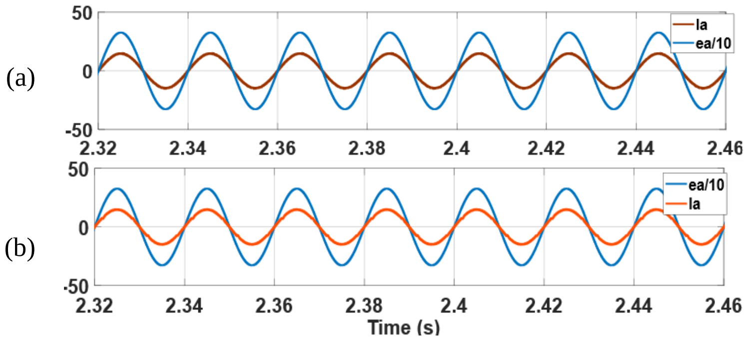


Figure 6. Grid current and voltage: (a) DPC-BS grid current and voltage and (b) DPC grid current and voltage

4.3. Simulation results of DPC and DPC-BS under unbalanced Grid with L = 5 mH

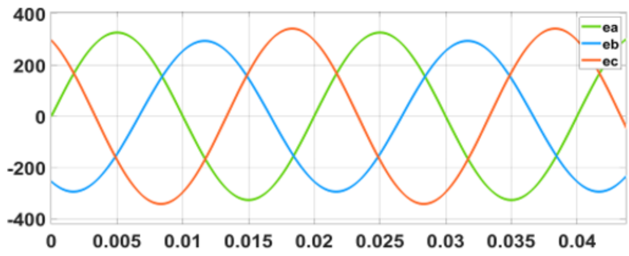
To evaluate the performance of the proposed controller under unbalanced grid conditions, the second phase voltage (eb) is decreased by 10%, and the third phase voltage (ec) is increased by 5%. Consequently, as illustrated in Figure 6, the three-phase RMS voltages are set to [ea,eb,ec] = [230, 207, 241] V. The simulation results are presented below.

Under unbalanced grid conditions, both control strategies' performance degrades; however, compared to DPC, the proposed DPC-BS controller demonstrates superior performance, with a maximum current THD of 4.91% as shown in Figures 7 and 8, satisfying our objective (THD <5%). While DPC exhibits better Vdc voltage tracking by maintaining a small steady-state error, as Figure 9 shows (0.3V vs. 1.5V for the DPC-BS), it underperforms in every other aspect. In fact, DPC fails to maintain a current THD under 5% or a unity power factor, as depicted in Figure 10; the DPC control strategy consumes a small amount of reactive power, while the DPC-BS reactive power remains zero. Overall, even with a slightly higher steady-state error, the DPC-BS strategy outperforms conventional DPC by meeting our key objectives.

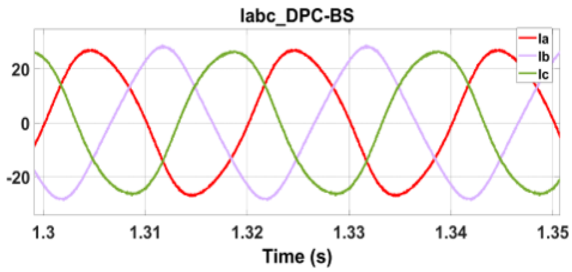
4.4. Performance of DPC vs. DPC-BS under distorted grid conditions and unfavorable inductance L = 10 mH

To evaluate the robustness of the proposed DPC-BS controller, two unfavorable conditions are imposed. First, the grid inductance is increased to L = 10 mH, which is twice the nominal design value of 5 mH. Second, a 5th harmonic component with an amplitude of 5% of the fundamental voltage is injected into all three phases. These extreme, yet unfavorable conditions stress-test our controller's adaptation to parameter variations and disturbance rejection capabilities. Figure 11 below shows the distorted grid voltage used in this simulation. The simulation results are presented in the next figures.

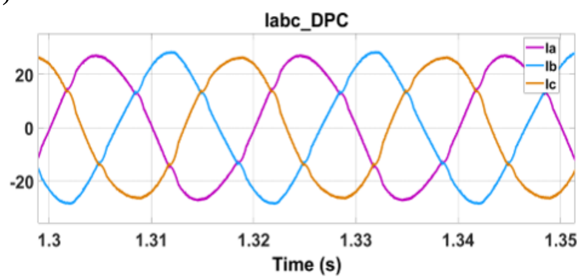
In this simulation, the introduction of the 5th harmonic (Figure 11) combined with increased grid inductance L imposes unfavorable and challenging conditions. Both strategies maintain stability at the price of performance; the grid current (Figure 12) suffers from intense distortion as its THD increases while the dynamic response decreases. In addition, we reach our THD limit of 5.82% vs. 9.63 % as Figure 13 shows, in favor of the DPC-BS, which confirms the efficacy and robustness of the proposed control.



(a)

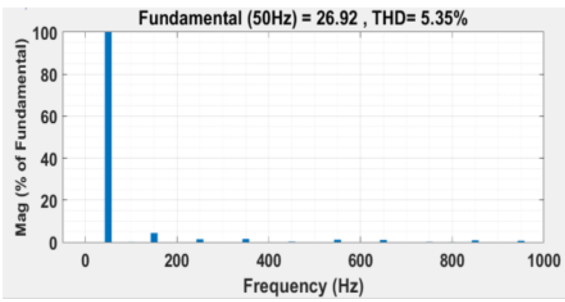


(b)

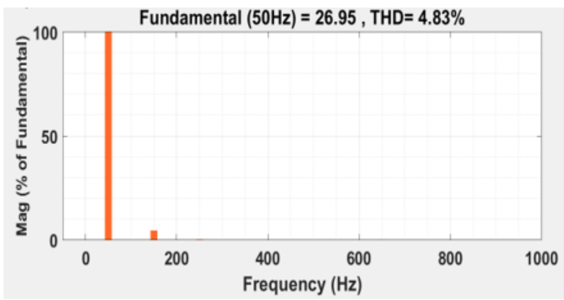


(c)

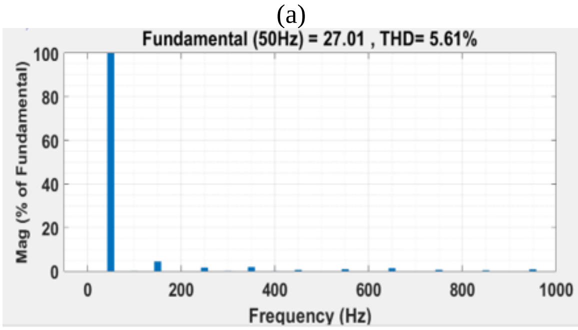
Figure 7. Response under unbalanced grid voltage: (a) unbalanced grid voltage, (b) DPC-BS current response under unbalanced grid, and (c) DPC current response under unbalanced grid



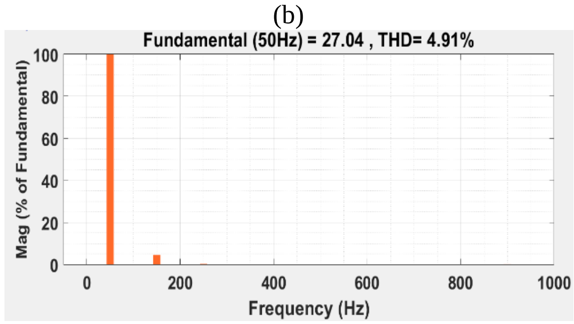
(a)



(b)

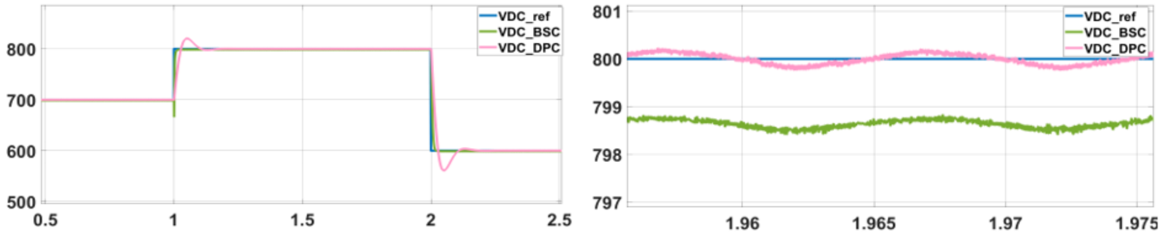


(c)



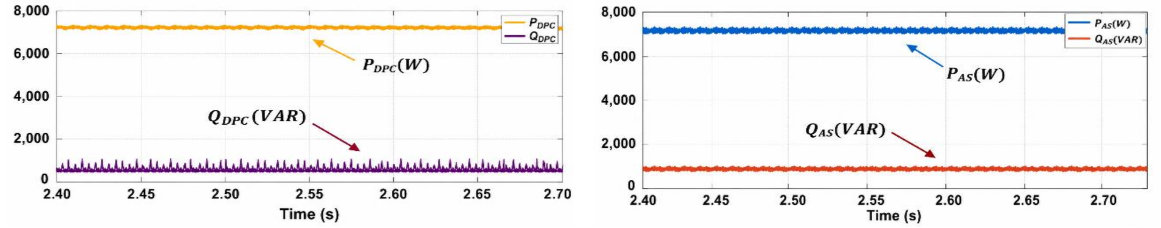
(d)

Figure 8. Current THD characteristics of the DPC and DPC-BS controls: (a) minimum current THD of DPC, (b) maximum current THD of DPC, (c) minimum current THD of DPC-BS, and (d) maximum current THD of DPC-BS



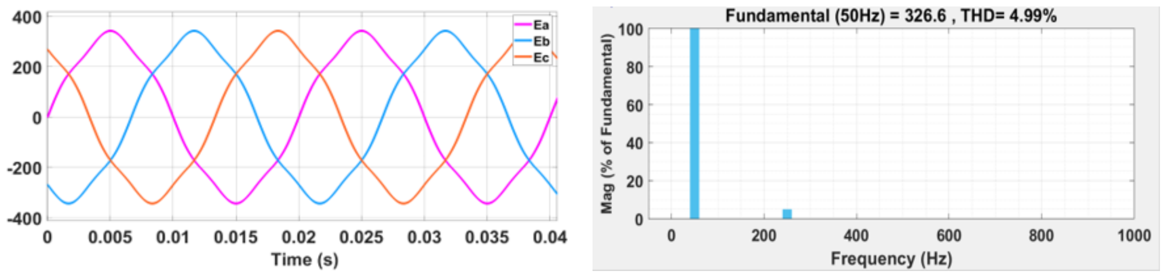
(a) (b)

Figure 9. BC-Bus voltage response: (a) overall response and (b) zoom of VDC voltage under 800 V



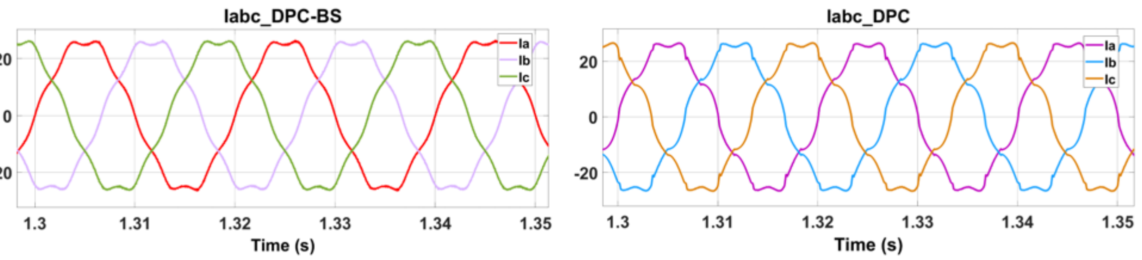
(a) (b)

Figure 10. Active and reactive power response: (a) active and reactive power of DPC control and (b) active and reactive power of DPC-BS control



(a) (b)

Figure 11. Distorted grid voltage: (a) distorted grid voltage evolution and (b) THD of the grid voltage



(a) (b)

Figure 12. Distorted grid current of: (a) DPC-BS control and (b) DPC control

As DPC exhibits unsatisfactory results in current THD, it also fails to maintain an acceptable Vdc response (Figure 14). Despite the negligible steady-state error (which was always an advantage of the conventional DPC), the first overshoot increased dramatically, leading to a longer response time. Voltage spikes appear for the first time in steady state at 800 V Vdc, indicating the limitation of DPC in adapting to perturbation or parameter variation. In conclusion, the DPC-BS demonstrates significantly better performance than DPC control under unfavorable conditions; however, the current THD slightly exceeds the 5% threshold.

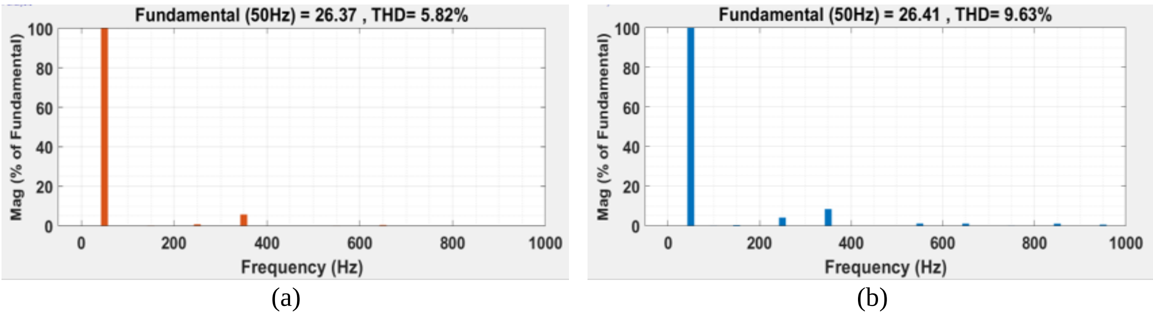


Figure 13. THD of distorted grid current: (a) DPC-BS (5.82%) and (b) DPC (9.63%)

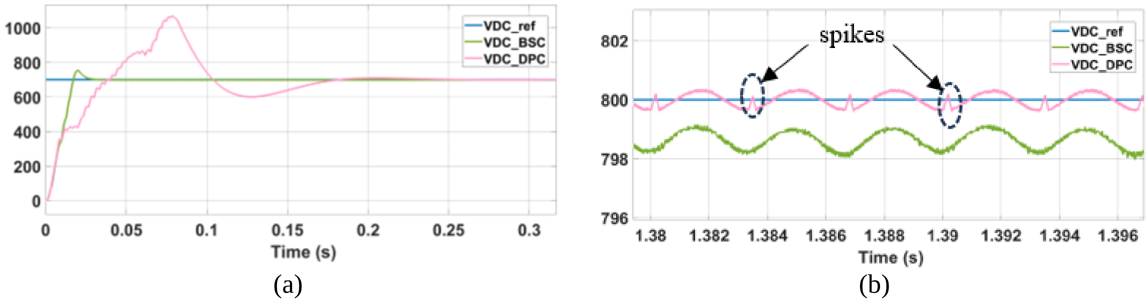


Figure 14. DC-bus voltage: (a) first overshoot of Vdc voltage and (b) zoom of Vdc response at 800 V

5. RESULTS AND DISCUSSION

To summarize the comparative analysis of the DPC and DPC-BS control strategies, Table 2 provides the key differences under balanced, unbalanced, and distorted grid conditions. The metrics evaluated include the maximum and minimum current THD, steady-state error of the DC-BUS voltage, the settling time at 95%, and the first overshoot. The proposed controller based on the DPC-BS strategy demonstrates superior dynamic response, robustness against parameter variation, and disturbance rejection across all tested scenarios.

The conventional DPC achieved a lower steady-state error, but it underperforms in critical metrics such as current THD and response time. The faster transient performance of the backstepping approach is mainly attributed to the presence of the derivative term in the control law, which enhances the system's ability to track rapid variations. However, the same derivative action is also responsible for larger overshoot. Overall, the results of this comparative study confirm the efficiency of the backstepping approach in maintaining system stability even under unfavorable grid conditions.

Table 2. Summary of comparative performance of DPC and DPC-BS

Operating condition	Metric	DPC	DPC-BS	Comparison winner
Balanced grid	Max current THD	2.51 %	1.98 %	DPC-BS
	Min current THD	3.34 %	1.76 %	DPC-BS
	Vdc steady-state error	< 0.1 V	1.2V to 1.3V	DPC
	Response time (95%)	54.34 mS	16.3 mS	DPC-BS
	First overshoot	5.97 %	13.31 %	DPC
	Power factor	≈ 1	≈ 1	Both
Unbalanced grid	Max current THD	5.61 %	4.86 %	DPC-BS
	Min current THD	5.21 %	4.81 %	DPC-BS
	Vdc steady-state error	0.1 V	1.2V to 1.5 V	DPC
	Response time (95%)	63.84 mS	16.47 mS	DPC-BS
	First overshoot	7 %	13.37 %	DPC
	Power factor	≈ 1	≈ 1	both
Distorted grid with doubled grid inductance	Max current THD	9.63%	5.82 %	DPC-BS
	Min current THD	6.44 %	5.32 %	DPC-BS
	Vdc steady-state error	0.1V to 0.4V	1.5 V	DPC
	Response time (95%)	160 mS	21.96 mS	DPC-BS
	First overshoot	52.5 %	7.6 %	DPC-BS
	Power factor	≈ 1	≈ 0.9998	DPC-BS

6. PROCESSOR-IN-THE-LOOP VALIDATION

To further validate our control algorithm, a processor-in-the-loop (PIL) test was conducted. The controller was implemented in a DSP TMS320F28379D dual-core processor at 200 MHz, which is widely used in power electronics control. The backstepping (BS) controller operated with a sampling frequency of 50 kHz. The plant model used the same parameters listed in Table1 with a grid inductance (L) of 10 mH. The overall PIL scheme is illustrated in Figure 15.

The experimental implementation employed the same control law presented in this paper. However, the derivative term cannot be implemented directly; therefore, it was replaced with a transfer function providing an equivalent approximation to the derivative action. The experimental results obtained from the PIL implementation are illustrated in the next figures.

Figure 16 demonstrates the main performance of the proposed controller, showing an accurate Vdc response, a unity power factor, fast transient response, and low grid current THD complying with our objective. However, despite these good performances, certain limitations must be highlighted, as the serial communication link (USB) between the host and DSP induces latency and limits the baud rate, which affects the sampling frequency. Even with all these limits, the PIL profiling results indicate that the maximum average execution time step is 5.17 µs with a sampling time of 20 µs, which demonstrates excellent real-time execution capability. Figure 17 presents the PIL setup, using a TMS320F28379D DSP connected to a host PC via a USB cable.

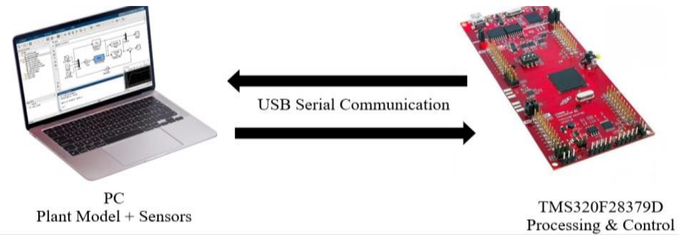


Figure 15. Processing-in-the-loop experimental setup using the TMS320F28379D DSP

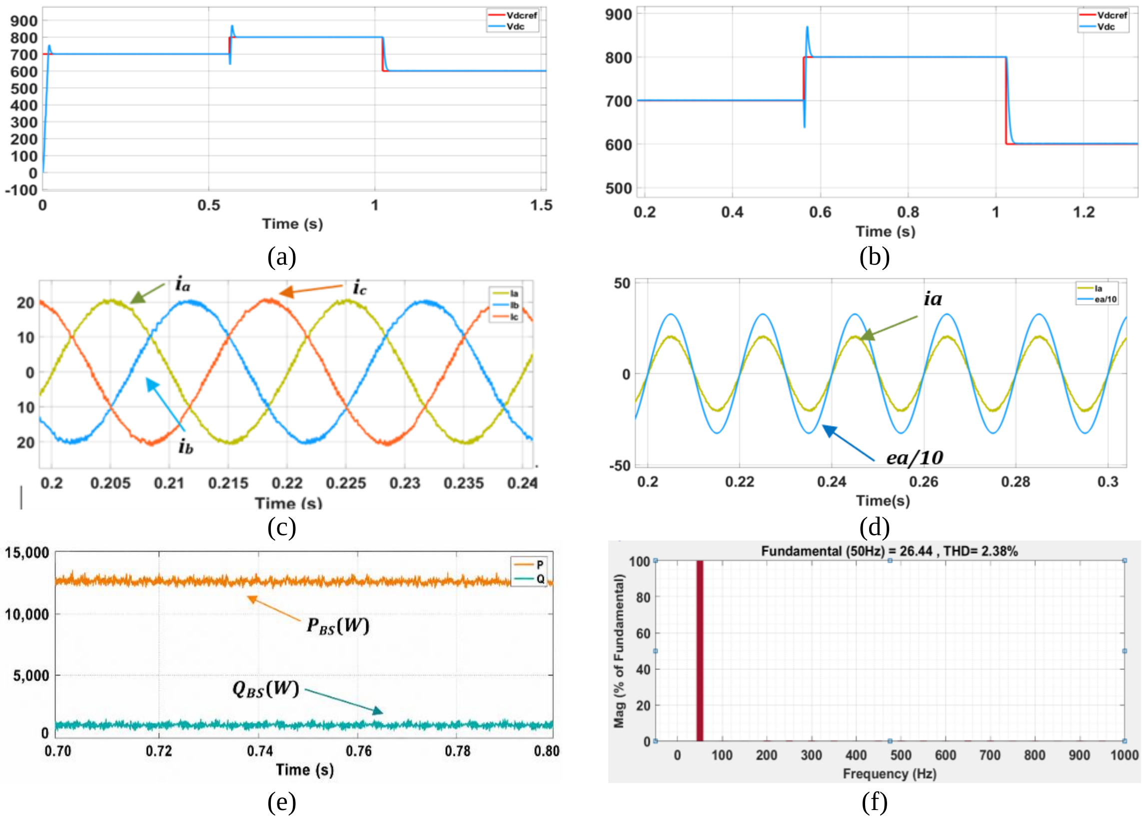


Figure 16. Main PIL performances: (a) Vdc response, (b) zoom of Vdc response, (c) grid currents, (d) grid voltage and current (in phase), (e) active and reactive power, and (f) current THD under 800 V Vdc

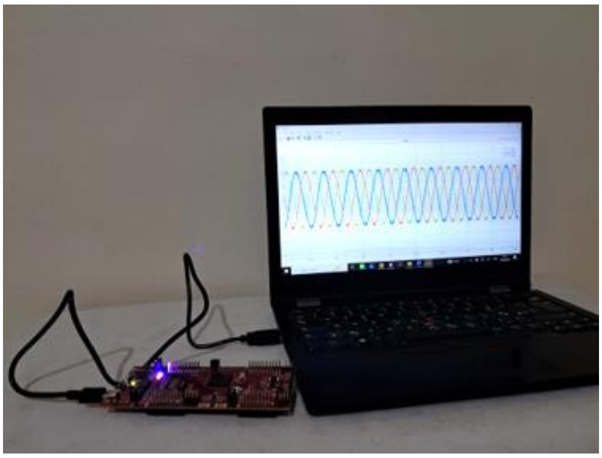


Figure 17. PIL setup

7. CONCLUSION

In this paper, we compared the performance of direct power control (DPC) and the proposed DPC-backstepping (DPC-BS) for a three-phase grid connected PWM rectifier and validate our control algorithm with PIL implementation. The objective was to address the limitation of the conventional DPC by maintaining near sinusoidal current (THD < 5%), unity power factor (Q = 0), achieving grid power quality, under all circumstances, disturbance or parameter variation. The proposed control law eliminates the sign function found in conventional backstepping law, to reduce chattering and discontinuity, while assuring a Backstepping design for active and reactive power. The simulation results in MATLAB/Simulink environment conducted under balanced, unbalanced, and distorted grid conditions with parameter variation, confirm the robustness and efficacy of the DPC-BS strategy, achieving faster response, less distorted current and stable performance in all scenarios. However, even with its superiority and robustness, DPC-BS slightly exceeds the 5% current THD under severe grid harmonic pollution (5.32-5.82%), therefore future efforts will be directed toward harmonic compensation technique or adaptive filtering methods to ensure compliance with our objective. A processor-in-the-loop (PIL) implementation was carried out to confirm our control algorithm feasibility and validate further DPC-BS robustness.

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AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

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C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

All authors state that there is no conflict of interest.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author, [SC], upon reasonable request.

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