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A 17-level switched-capacitor inverter with asymmetric voltage distribution and inherent balancing: design and experimental verification

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ABSTRACT

This paper proposes a 17-level switched-capacitor multilevel inverter (SC-MLI) whose four capacitors are deliberately held at unequal voltages: two at the full input voltage and two at half of it. Halving the smallest synthesizable step is the novelty of the work, because it doubles the number of levels obtainable from a given set of capacitors and therefore yields seventeen equidistant levels and a fourfold voltage gain from fourteen switches, four capacitors, two diodes, and a single DC source, with no voltage sensor and no balancing controller. Self-balancing is proven analytically for both capacitor groups; the capacitors and a single soft-charging inductor are sized from the maximum discharge duration, and two modulation strategies are implemented on the same FPGA. The design was validated by simulation and on a laboratory prototype driving a 180 W single-phase induction motor. The measured output reaches 186.4 V from a 47.175 V input, a gain of 3.95, with a voltage total harmonic distortion of 1.12% and capacitor ripples between 2.3% and 4.5%, and the measured efficiency is 94.6%. Against eleven recent SC-MLI topologies, the converter attains the highest gain per component count and the lowest cost function 2.38.

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1. INTRODUCTION

Multilevel inverters (MLIs) are now the standard choice in photovoltaic (PV) systems, motor drives, electric vehicles, and active filters, because they synthesize a stepped waveform that approximates a sinusoid with low harmonic distortion, low device voltage stress, and reduced electromagnetic interference [1]. Their main design objective has shifted from simply increasing the number of levels to obtaining more levels from fewer components, and recent surveys agree that the component count, not the level count, is the limiting factor in industrial adoption [2]. For single-source applications such as PV strings, battery packs and motor drives, this places a premium on topologies that raise both the number of levels and the voltage gain without adding DC sources, sensors or balancing controllers.

The three classical families each carry a structural penalty. The neutral-point clamped inverter needs a large number of clamping diodes and an auxiliary circuit to balance its DC-link capacitors [3]. The flying-capacitor inverter needs a pre-charging circuit and bulky capacitors whose voltages must be measured at high frequency [4]. The cascaded H-bridge inverter avoids both problems but requires one isolated DC source per

cell, which is impractical in vehicle drives and in single-string PV systems [5]. Reduced-device-count structures have therefore been investigated intensively [6], [7].

Switched-capacitor MLIs (SC-MLIs) address the source problem directly: a single DC source charges capacitors that are subsequently reconnected in series, so the output voltage is boosted above the input, and the capacitor voltages balance themselves without sensors [8], [9]. Cells of this kind have been demonstrated at seven, nine and thirteen levels [10]-[12], and adapted to domestic photovoltaic and three-phase applications [13], [14]. The price is a larger number of switches, higher blocking voltages, and an uncontrolled inrush current when the discharged capacitors are first connected to the source. The inrush problem has been treated with current-limiting resistors, with series inductors, and with resonant soft-charging branches [15], and a soft-charging variant has recently been demonstrated on a seven-level cell [16].

Existing 17-level SC-MLIs illustrate both the progress and the remaining trade-offs. Sun *et al*. [17] reach 17 levels with ten transistors, four capacitors, and two diodes by combining switched-capacitor and flying-capacitor cells. Haghighian *et al*. [18] and Marangalu *et al*. [19] place a flyback DC-DC stage ahead of the switched-capacitor stage, the latter with a twofold gain and a reduced capacitor charging spike. Hosseinpour *et al*. [20] obtain a fourfold gain with suppressed inrush current from ten switches, four capacitors, and three diodes, while Chandan *et al*. [21] push the gain to eightfold for a grid-connected PV system. Dhanamjayulu *et al*. [22] generate 17 levels from a single DC source with thirteen switches, four capacitors and two diodes. These designs trade level count, voltage gain, component count, and inrush protection against one another in different ways, and none of them is the best on every criterion.

Unequal capacitor voltages offer a further route, because two capacitors charged to different values can be combined into more distinct sums than two identical ones. The idea has been applied in a nine-level quadruple-boosting cell [23] and in an asymmetric multicell inverter with a reduced number of sources [24]. To the authors' knowledge, it has not been reported in a 17-level structure in which one capacitor pair is held at half the input voltage by a self-balancing divider, so that the smallest step falls to 0.5 Vin while the gain reaches four. This is the gap addressed here.

This paper proposes a 17-level SC-MLI in which C1 and C2 are held at the full input voltage while C3 and C4 form a capacitive divider held at half of it. The 0.5 Vin step produced by the divider doubles the number of levels obtainable from four capacitors, so 17 levels and a fourfold gain are reached with 14 switches, four capacitors and two diodes, and without any sensor or balancing controller. The specific contributions are: i) The asymmetric voltage distribution and its switching table; ii) An analytical self-balancing proof, stated with its assumptions, for both capacitor groups; iii) A maximum-discharge-duration (MDD) design of the capacitors and of a single soft-charging inductor; and iv) Simulation and experimental validation on an FPGA-controlled prototype driving a 180 W single-phase induction motor, followed by a component-level comparison with recently reported SC-MLI topologies. The paper follows the IMRaD structure: i) Section 2 develops the proposed topology and its analysis; ii) Section 3 describes the modulation, the simulation model, and the experimental setup; iii) Section 4 presents and discusses the results; and iv) Section 5 concludes.

2. THE PROPOSED 17-LEVEL SC-MLI TOPOLOGY

2.1. Circuit structure and functional stages

The proposed topology is shown in Figure 1. It comprises a single DC source Vin, fourteen bidirectional switches S1-S14 implemented as back-to-back MOSFET pairs with eleven independent gate signals, four switched capacitors C1-C4 and two unidirectional diodes D1 and D2. C1 and C2 balance at Vin and C3 and C4 at 0.5 Vin, and 17 output levels are obtained without sensors or auxiliary balancing circuits.

Three functional stages can be identified in Figure 1. The input polarity stage, formed by S1 and S2 at the source terminals, applies the source with the correct polarity in each half-cycle. The boosting stage, formed by C1 and C2 with S3, S4, S13, S14 and the diodes D1 and D2, connects the two boost capacitors in parallel across Vin during the charging intervals, through the S13-D1 path in the positive half-cycle and the S14-D2 path in the negative one, and connects them in series with the source during the discharging intervals. The divider and output stage, formed by C3 and C4 with S5-S12, builds the capacitive divider that enforces VC3 = VC4 = 0.5 Vin, routes the synthesized voltage to the load, and selects either the divider midpoint or the full divider voltage. S12 provides an additional routing path that enables alternative series-parallel combinations during level generation.

2.2. Asymmetric capacitor voltage distribution

The voltage ratio VC1:VC2:VC3:VC4 = (1:1:0.5:0.5) Vin is a deliberate design choice rather than a by-product of the switching pattern. C1 and C2 operate at the full input voltage and act as the boosting elements, whereas C3 and C4 operate at half of it and provide the 0.5 Vin step. Because the smallest step is half the input voltage instead of the input voltage itself, the number of distinct levels obtainable from the same four capacitors is doubled, which is precisely the limitation identified in the symmetric 17-level designs

of section 1. The capacitance values are then selected from the charge removed during the MDD of each capacitor, as derived in section 2.7, so that every ripple stays below the 10% design limit; a single standard value of 10 mF satisfies all four constraints.

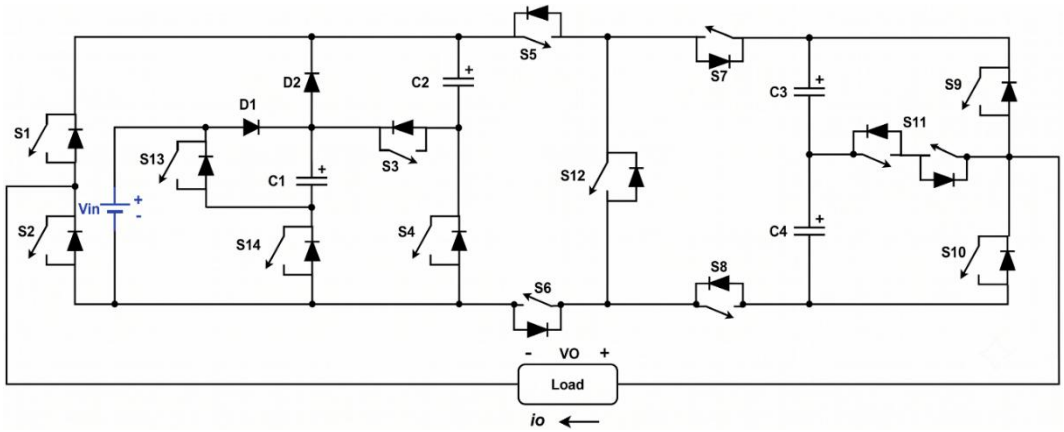


Figure 1. Proposed 17-level SC-MLI topology

2.3. Diode function

Diodes D1 and D2 block the reverse discharge of C1 and C2 through the parasitic paths formed by the switch body diodes during the OFF states [25]. Without them, C1 could partially discharge through the body diode of S3 in the high-level modes, which would corrupt the voltage contributions and degrade the self-balancing. Each diode conducts only while its capacitor is being charged and is reverse-biased while that capacitor discharges into the load, so a fast-recovery device is sufficient; the prototype uses the STTH30L06 ultrafast diodes.

2.4. Switching states and modes of operation

Table 1 lists the complete switching table, where 1 and 0 denote the ON and OFF states of each switch and the symbols C, D and N denote a charging, discharging or idle capacitor. The reader should note two features of the table: the seven low-magnitude states in which all four capacitors are charged, and the ten high-magnitude states in which the capacitors are progressively added in series with the source. Four representative modes explain the mechanism.

At +0.5 Vin, switches S2, S3, S5, S8, S9, S12 and S13 conduct. The source charges C1 and C2 in parallel through S13-D1, while C3 and C4 charge in series and converge to 0.5 Vin each. The load is connected to the midpoint of the divider through S9, so Vo = 0.5 Vin. This state is the main global recharging interval of the cycle.

At +2 Vin, switches S2, S3, S5, S8, S11, S12 and S14 conduct, C1 discharges in series with the source and Vo = Vin + VC1. At +2.5 Vin, with S2, S3, S5, S7, S9 and S14 ON, C1 and C3 discharge together and Vo = Vin + VC1 + VC3; this is the step that only the asymmetric distribution can produce. At the maximum level, S2, S4, S5, S6, S7, S8, S11 and S14 place the source and all four capacitors in series, giving Vo = Vin + VC1 + VC2 + VC3 + VC4 = 4 Vin.

The negative levels are obtained by activating S1 instead of S2, which reverses the polarity applied to the boosting network, while the S13-D1 and S14-D2 paths exchange their charging roles. The capacitor patterns mirror those of the positive half-cycle, as shown in Table 1. Because the two half-cycles use mirrored charging paths for the same capacitors, the positive and negative staircases have equal amplitude in steady state, and the output carries no DC offset.

2.5. Voltage gain analysis

The maximum output is reached when all four capacitors discharge in series with the source. Applying Kirchhoff voltage law along that conduction path gives (1), and substituting the nominal asymmetric voltages gives (2).

$$V_o = V_{IN} + V_{C1} + V_{C2} + V_{C3} + V_{C4} \quad (1)$$

$$V_0 = V_{IN} + V_{IN} + V_{IN} + \frac{V_{IN}}{2} + \frac{V_{IN}}{2} = 4V_{IN} \quad (2)$$

The fourfold gain is therefore obtained without any symmetry assumption, and the step between consecutive levels, 0.5 Vin, is exactly the voltage held by the divider capacitors. Table 2 verifies each of the 17 levels against the switching states of Table 1; the reader should check in particular the +2.5 Vin and +3.5 Vin rows, which are the levels that a symmetric distribution of the same four capacitors cannot generate.

Table 1. Switching states of the proposed 17-level SC-MLI (C = charging, D = discharging, N = idle)

Level	V_o	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	C1	C2	C3	C4
+8	4 V_{in}	0	1	0	1	1	1	1	1	0	0	1	0	0	1	D	D	D	D
+7	3.5 V_{in}	0	1	0	1	1	1	1	1	1	0	0	0	0	1	D	D	D	N
+6	3 V_{in}	0	1	0	1	1	0	0	1	0	0	1	1	0	1	D	D	D	D
+5	2.5 V_{in}	0	1	1	0	1	0	1	0	1	0	0	0	0	1	D	N	D	N
+4	2 V_{in}	0	1	1	0	1	0	0	1	0	0	1	1	0	1	D	N	N	N
+3	1.5 V_{in}	0	1	1	0	1	0	0	1	1	0	0	1	0	1	C	N	D	N
+2	1 V_{in}	0	1	1	0	1	0	0	1	0	0	1	1	1	0	C	C	C	C
+1	0.5 V_{in}	0	1	1	0	1	0	0	1	1	0	0	1	1	0	C	C	C	C
0	0	0	1	0	1	1	1	1	1	0	1	0	0	0	1	C	C	C	C
−1	−0.5 V_{in}	1	0	0	1	1	1	1	1	0	0	1	0	0	1	C	C	C	C
−2	−1 V_{in}	1	0	0	1	1	1	1	1	0	1	0	0	0	1	C	C	C	C
−3	−1.5 V_{in}	1	0	0	1	0	1	1	0	0	0	1	1	0	1	C	D	N	N
−4	−2 V_{in}	1	0	1	0	0	1	0	1	0	1	0	0	0	1	D	N	N	N
−5	−2.5 V_{in}	1	0	1	0	0	1	1	0	0	0	1	1	0	1	D	D	N	N
−6	−3 V_{in}	1	0	1	0	0	1	1	0	0	1	0	1	0	1	D	D	D	D
−7	−3.5 V_{in}	1	0	1	0	0	1	1	0	0	0	1	1	1	0	D	D	D	N
−8	−4 V_{in}	1	0	1	0	0	1	1	0	0	1	0	1	1	0	D	D	D	D

Table 2. Verification of the 17 output voltage levels

Level	Expression	Result	Capacitors involved
±1	± (C_3–C_4 divider midpoint)	±0.5 V_{in}	All charging
±2	± V_{in} (source only)	±1.0 V_{in}	All charging
±3	± (V_{in} + V_{C3})	±1.5 V_{in}	C3 discharging
±4	± (V_{in} + V_{C1})	±2.0 V_{in}	C1 discharging
±5	± (V_{in} + V_{C1} + V_{C3})	±2.5 V_{in}	C1, C3 discharging
±6	± (V_{C1} + V_{C2} + V_{C3} + V_{C4})	±3.0 V_{in}	All discharging
±7	± (V_{in} + V_{C1} + V_{C2} + V_{C3})	±3.5 V_{in}	C1, C2, C3 discharging
±8	± (V_{in} + V_{C1} + V_{C2} + V_{C3} + V_{C4})	±4.0 V_{in}	All discharging

2.6. Self-balancing analysis

2.6.1. Assumptions

The analysis that follows rests on four assumptions, stated explicitly so that the derivation can be reproduced; i) The switching frequency is much higher than the fundamental frequency, so the capacitor voltages are constant within one switching period; ii) The load current is sinusoidal at the fundamental frequency, io(t) = I0*sin(wt-phi), where phi is the load power-factor angle; the switching ripple is filtered by the machine inductance; iii) Every conduction path is modelled by a single equivalent on-state resistance Ron, and the capacitor equivalent series resistance is absorbed into it; and iv) The capacitors are large enough for the voltage deviation within one cycle to remain small compared with the nominal value, so first-order perturbation analysis is valid. These assumptions are the standard ones used in the SC-MLI literature [26] and are satisfied by the parameters of section 3.

2.6.2. Charge-balance condition

Self-balancing means that the capacitor voltages converge to their nominal values without closed-loop control. The necessary and sufficient condition is that the net charge transferred to each capacitor over one fundamental period T is zero [27], which is expressed by (3). Combining (3) with the definition of the capacitor voltage gives the steady-state ripple (4).

$$\Delta Q_{Ck} = \int_0^T i_{Ck}(t)dt = 0 \ \forall k \in \{1,2,3,4\} \quad (3)$$

$$\Delta V_{Ck} = \frac{\Delta Q_{Ck}}{C_k} \quad (4)$$

2.6.3. Proof for C1 and C2

From Table 1, C1 charges during the levels 0, +/-1, +/-2, and +/-3, that is, seven states per cycle, and discharges during +/-4 to +/-8, that is, ten states. The derivation proceeds in three steps. First, during a charging state, C1 is connected in parallel with the source through S13-D1, so the charging current is given by (5), where VC1 is the instantaneous capacitor voltage.

$$i_{C1,ch} = \frac{V_{in} - V_{C1}}{R_{on}} \quad (5)$$

Second, a small deviation is introduced, VC1 = Vin + e, and substituted into (5), which gives (6): the charging current becomes negative and therefore discharges the capacitor whenever the deviation is positive, and positive whenever the deviation is negative.

$$i_{C1,ch} = -\frac{\varepsilon}{R_{on}} \quad (6)$$

Third, during the discharging states C1 is in series with the load and its current is fixed by the load, io(t), so it does not depend on the deviation to first order. The net charge over one period is therefore given by (7), whose derivative with respect to the deviation is negative, so the deviation decays and the equilibrium VC1 = Vin is asymptotically stable. Because the sinusoidal reference makes the low-magnitude levels occupy longer time fractions near the zero crossings, the seven charging states supply more than enough charge to replace what the ten discharging states remove. The same derivation holds for C2 with S14-D2 in place of S13-D1.

$$\Delta Q_{C1}(\varepsilon) = -\frac{\varepsilon T_{ch}}{R_{on}} < 0 \; for \; \varepsilon > 0 \quad (7)$$

2.6.4. Proof for C3 and C4

During every charging state, C3 and C4 are connected in series across the intermediate bus, which imposes (8). They are always charged simultaneously and through the same path, so their charge increments are equal, as stated in (9). Subtracting the two capacitor equations and using (8) and (9) gives (10) for the difference of the two voltages, which decays exponentially with the time constant $R_{on}C$. The equilibrium is therefore VC3 = VC4 = 0.5 Vin, and any imbalance between the two divider capacitors is removed by the charging path itself rather than by a controller.

$$\mathrm{V_{C3}} + \mathrm{V_{C4}} = \mathrm{V_{IN}} \quad (8)$$

$$\Delta \mathrm{Q_{CHARGE}} = \int_{\mathrm{CHARGE}} \mathrm{I_{C3}DT} = \int_{\mathrm{CHARGE}} \mathrm{I_{C4}DT} \quad (9)$$

$$\Delta \mathrm{V(T)} = \mathrm{V_{C3}} - \mathrm{V_{C4}} = \Delta \mathrm{V(0)E^{-T/(R_{ON}C)}} \quad (10)$$

The result of sections 2.6.3 and 2.6.4 can be summarized in a single Lyapunov argument. Taking the deviation vector of the four capacitor voltages and the energy-like function (11), which is positive definite, its derivative during the charging intervals is negative definite because each deviation appears through the resistive term of (6). The equilibrium is therefore asymptotically stable for every initial condition inside the operating region, which is the analytical statement of the self-balancing property verified experimentally in section 4.

$$V_L(\varepsilon) = \frac{1}{2}[C_1\varepsilon_1^2 + C_2\varepsilon_2^2 + C_3\varepsilon_3^2 + C_4\varepsilon_4^2] > 0 \quad (11)$$

2.7. Capacitor design and inrush current suppression

The capacitors are sized from the maximum discharge duration (MDD), that is the longest interval during which a capacitor supplies the load without being recharged [28]. The switching instants that delimit these intervals follow from (12), the charge removed during the MDD of the boost and divider capacitors from (13) and (14), and the resulting minimum capacitances from (15) and (16).

$$t_x = \frac{arcsin\left(\frac{2x-1}{N_L-1}\right)}{2\pi f_0}, N_L = 17 \quad (12)$$

$$\Delta Q_{C1} = 2\int_{t_4}^{T/2-t_4} I_0 sin(\omega t - \varphi) dt \quad (13)$$

$$\Delta Q_{C3} = \Delta Q_{C4} = 2\int_{t_3}^{T/2-t_3} I_0 sin(\omega t - \varphi) dt \quad (14)$$

$$C_1, C_2 \geq \frac{2I_0(cos\alpha_1 - sin\varphi)}{2\pi f_0 \cdot V_{in} \cdot \Delta V_{ripple}} \quad (15)$$

$$C_3, C_4 \geq \frac{2I_0(cos\alpha_2 - sin\varphi)}{2\pi f_0 \cdot V_{in} \cdot \Delta V_{ripple}} \quad (16)$$

A numerical example makes the procedure reproducible. With I0 = 0.46 A, f0 = 50 Hz and NL = 17, (12) gives t4 = 1.44 ms, so the MDD of C1 spans 1.44 ms to 8.56 ms. Evaluating (13) over that window yields a removed charge of 4.0 mC, and (15) then requires at least 0.85 mF for a ripple of 10% of 47.175 V. The selected 10 mF gives a margin of about twelve, which is why the measured ripple in section 4 is only 2.5%. Figure 2 shows the resulting level pattern together with the switching angles and the MDD intervals of the four capacitors; the reader should observe that the MDD of C1 and C2 covers the peak region of the waveform, whereas that of C3 and C4 is split into shorter intervals, which is the reason why all four capacitors can share the same capacitance value. Table 3 summarizes the sizing.

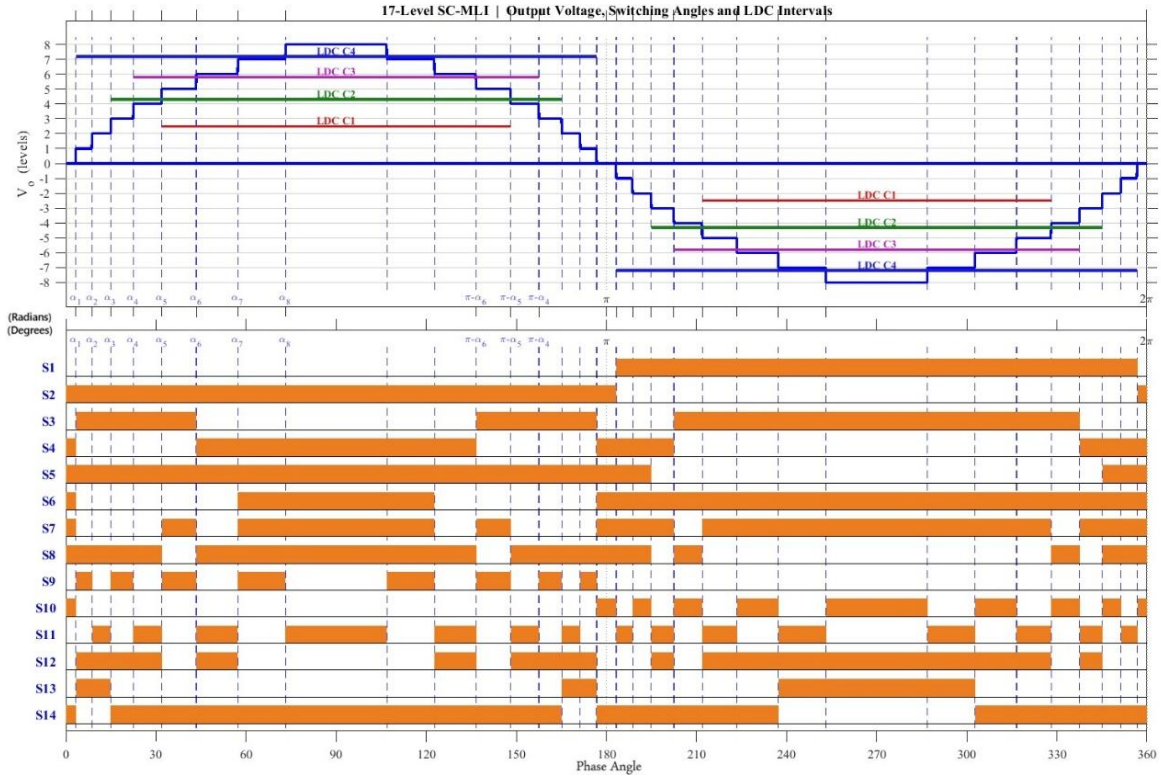


Figure 2. Output voltage levels, switching angles, and capacitor maximum-discharge-duration intervals

Table 3. Capacitor sizing based on the maximum discharge duration

Capacitor	Nominal voltage	Selected value	MDD interval	Ripple limit
C1	V_{in} = 47.175 V	10 mF	$t_4 - T/2 - t_4$ (±4 to ±8)	<10%
C2	V_{in} = 47.175 V	10 mF	$t_4 - T/2 - t_4$ (±4 to ±8)	<10%
C3	0.5 V_{in} = 23.59 V	10 mF	$t_3 - T/2 - t_3$ (+3 to +8)	<10%
C4	0.5 V_{in} = 23.59 V	10 mF	short (±6, ±8)	<10%

At start-up, the discharged capacitors are connected to the source through low-resistance paths, and the theoretical peak current Vin/Ron would reach about 175 A for Ron = 0.27 ohm, far above the device ratings. A single soft-charging inductor Lr with a reverse-parallel freewheeling diode Dr is therefore inserted in series with the DC source, where it lies in the common charging path of all four capacitors. The switching frequency must exceed the resonant frequency of the Lr-C network, as required by (17), and the inductor value follows from (18) and (19).

$$f_{sw} > f_r = \frac{1}{2\pi\sqrt{L_r C}} \tag{17}$$

$$L_r \geq \frac{1}{(2\pi f_{sw})^2 C} \tag{18}$$

$$L_r = \frac{V_{in}}{4 f_{sw} \Delta I_L} \tag{19}$$

With Lr = 0.23 mH the simulated peak charging current is limited to about 12 A, which is consistent with the charging spikes visible in the current-stress results of section 4. Placing one inductor at the source input rather than one per branch limits the inrush of all four capacitors with a single magnetic component [15].

3. METHOD

This section describes, in the order in which they were carried out, the modulation strategies applied to the converter, the simulation model used to evaluate it and the experimental setup used to validate it. The description is given in sufficient detail for the study to be reproduced: every parameter, component reference, controller setting, and measurement condition is stated.

3.1. Modulation strategies

3.1.1. Sinusoidal PWM

The first strategy is carrier-based sinusoidal pulse width modulation (SPWM). For a 17-level output, sixteen triangular carriers of equal amplitude and frequency are arranged in phase disposition, the arrangement that gives the lowest distortion among the multi-carrier schemes [29], and compared with a 50 Hz sinusoidal reference; the resulting level index is decoded into the fourteen gate signals according to Table 1. The modulation index is defined in (20), where Vref is the peak of the reference and Vcar the peak of one carrier. Two variants are evaluated: with the zero-level included (WZ) and with the zero-level excluded (WoZ).

$$M_a = \frac{V_{ref}}{8V_{car}} \tag{20}$$

3.1.2. Modified absolute sinusoidal PWM

The second strategy is modified absolute sinusoidal pulse width modulation (MASPWM), introduced for MLIs fed from unequal DC voltages and later applied to different control structures and to PV-fed asymmetric topologies [30]. The switching angles are computed offline from the absolute value of the sinusoidal reference through (21), which for NL = 17 gives the eight angles that build the positive half-cycle; the negative half-cycle is their mirror image. Every device therefore commutates once per half-cycle, at the fundamental frequency, and the zero-voltage state is excluded from the waveform, an approach also used in reduced-switch topologies without a zero-level state [30].

$$\theta_i = sin^{-1}\left(\frac{2i\text{-}1}{N_L}\right), i = 1,2,\ldots,\frac{N_L\text{-}1}{2} = 8 \tag{21}$$

Table 4 compares the two strategies as applied to the proposed converter. The comparison is used later, in section 4, to explain why the carrier-based scheme gives the lowest distortion while the angle-based scheme gives the lowest switching losses. Figure 3 shows the gating signals of the fourteen switches together with the output voltage they produce; the reader should note that S1, S2, S5 and S6 change state only twice per cycle, whereas S9 to S12 carry the high-frequency pattern, which is what makes the loss distribution among the devices uneven.

3.2. Simulation model and setup

The converter, its load and its controller were modelled in MATLAB/Simulink. Figure 4 shows the complete model: the reference generator and the level-detection block on the left, the comparator bank and the embedded MATLAB function that decodes the level index into the fourteen gate signals in the center, and the output bus that drives the power stage on the right; the inset scope shows the absolute sinusoidal reference from which the MASPWM angles are derived. The power circuit uses the Simscape Specialized Power Systems library with ideal switches to which the on-state resistance of 0.27 ohm and the 2-microsecond dead time of the real devices are assigned, so that the simulated and measured conditions differ only in the parasitic elements that are not modelled.

Table 5 lists all simulation parameters. The solver is fixed-step discrete with a sample time of 1 microsecond, the input voltage is 47.175 V, the fundamental frequency is 50 Hz, the SPWM carrier frequency is 10 kHz, the MASPWM angles are applied at the fundamental frequency, the four capacitors are 10 mF, and the load is the same 180 W single-phase induction motor used in the experiment. The modulation index is unity in the steady-state tests and is stepped to 0.7 in the test of section 4.5. The output voltage and current, the four capacitor voltages, and the blocking voltage and current of every switch are recorded, and the harmonic spectra are computed with the fast Fourier transform (FFT) tool over an integer number of fundamental periods after the transient has decayed.

Table 4. Comparison of the two modulation strategies applied to the proposed converter

Feature	SPWM	MASPWM
Carrier signals	16 triangular carriers	None (angle-based)
Reference signal	Sinusoidal	Absolute sinusoidal
Switching-angle method	Carrier intersection	Precomputed from (21)
Zero-level state	Included (WZ) or excluded (WoZ)	Excluded
Device switching frequency	10 kHz	50 Hz (fundamental)
Measured THD_V	1.12% (WZ), 2.87% (WoZ)	2.91%
Modulation-index control	On-line, continuous	Fixed by construction
Best suited for	Lowest distortion	Lowest switching losses

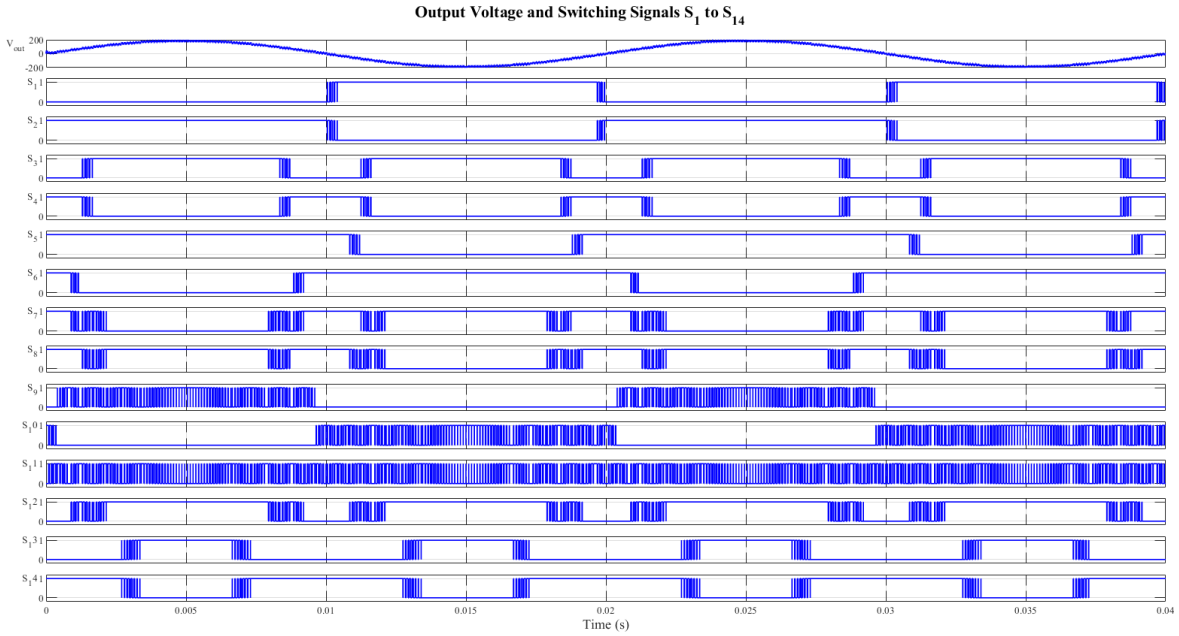


Figure 3. Simulated output voltage and gating signals of switches S1 to S14

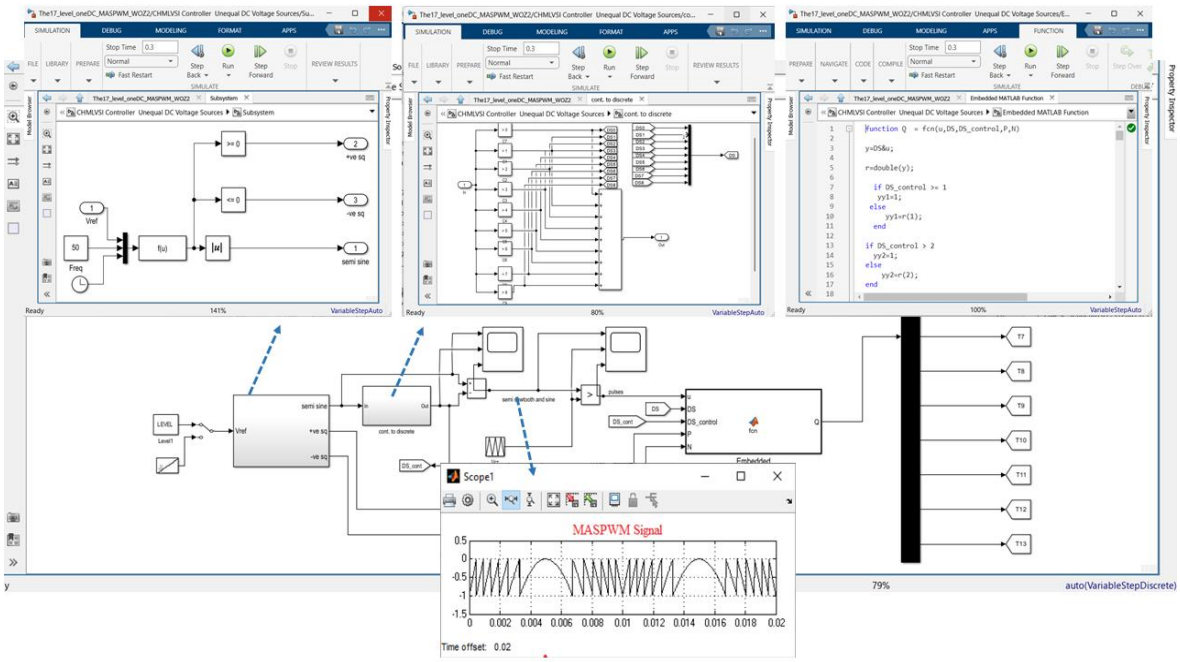


Figure 4. MATLAB/Simulink model of the proposed inverter: reference generation, level detection, gate-signal decoder, and power stage

Table 5. Simulation parameters

Parameter	Value	Parameter	Value
Input voltage V_{in}	47.175 V	Fundamental frequency f_0	50 Hz
Capacitors C_1–C_4	10 mF	SPWM carrier frequency	10 kHz
Soft-charging inductor L_r	0.23 mH	MASPWM switching	Fundamental (50 Hz)
Switch on-state resistance	0.27 Ω	Modulation index M_a	1.0 (0.7 in section 4.5)
Dead time t_d	2 μs	Solver/sample time	Discrete, 1 μs
Load	180 W single-phase induction motor	Output levels N_L	17

3.3. Experimental setup and measurement procedure

A laboratory prototype was built with the components listed in Table 6 and is shown in Figure 5. The photograph shows, from left to right, the oscilloscope, the host computer running the FPGA tool-chain, the Spartan-3A DSP board with its gate-driver ribbon, the power board carrying the fourteen MOSFETs and the four capacitors, the regulated DC supply, and the 180 W induction motor under test. The power switches are IRFP460 MOSFETs (500 V, 20 A, Ron = 0.27 ohm), the blocking diodes are STTH30L06 ultrafast devices (600 V, 30 A), the freewheeling diode of the soft-charging branch is a MUR1560 (600 V, 15 A), the soft-charging inductor is a hand-wound toroid of 0.23 mH rated at 5 A, and the four capacitors are 10 mF electrolytic units rated at 63 V (100 V for C1 and C2).

The gate signals are generated by a Xilinx Spartan-3A DSP FPGA operating from a 50 MHz clock. The switching table of Table 1 is implemented as a combinational decoder, the eight MASPWM angles are stored in a look-up table with a resolution of one clock cycle, that is 20 ns, which corresponds to an angular resolution of 0.00036 degrees at 50 Hz, and a dead time of 2 microseconds is inserted in hardware between every complementary pair. The SPWM variant is generated on the same device with a 10 kHz carrier. The gate signals are amplified and galvanically isolated by TLP358H optocoupler drivers supplied from four isolated 15 V rails.

The load is a commercially available single-phase induction motor rated 180 W (0.25 hp), 230 V, 1.5 A full-load current, 50 Hz, 1400 rpm, with an 8 microfarad/440 V AC run capacitor. The DC input is taken from a regulated bench supply set to 47.175 V and able to deliver 5 A. The motor was chosen because it presents a lagging, slip-dependent load, which is a more demanding test of the inductive current paths and of the capacitor balancing than a resistive or fixed R-L load. Since the converter delivers about 132 V rms, below the 230 V rating of the machine, the motor runs at reduced voltage, which is sufficient for verifying the converter, although not for characterizing the drive.

All waveforms are recorded with an FNIRSI DPOS350P digital storage oscilloscope (two channels, 350 MHz bandwidth, 1 GS/s sampling rate, 8-bit vertical resolution), visible on the left of Figure 5. Because the instrument has two channels, the output voltage and one further quantity are captured in each run: the voltage and the load current together for the waveform records, and the voltage and one capacitor at a time for the balancing records, with the trigger kept on the output voltage so that all records share the same time reference. The output voltage is measured with a 1:10 passive probe compensated before each session, and the capacitor voltages with the same probe type referenced to the corresponding capacitor terminal. Each quantity is captured over at least five fundamental periods, the RMS and harmonic values are read from the built-in measurement functions averaged over sixteen acquisitions, and every reported figure is the mean of three repeated measurements. The uncertainty follows from the instrument and probe specifications: a vertical accuracy of 3% of reading, a probe attenuation tolerance of 2% and a time-base accuracy of 50 ppm combine to an expanded uncertainty of about 3.6% for the voltage readings and about 0.1 percentage points for the THD values obtained from the same acquisitions. All measurements were taken at an ambient temperature of 25 +/- 2 degrees Celsius after ten minutes of continuous operation, so that the device and capacitor temperatures had settled.

Table 6. Components of the hardware prototype

Component	Part number/type	Rating	Quantity
Power switches S1–S14	IRFP460 N-MOSFET	500 V/20 A, R_{on} = 0.27 Ω	14
Blocking diodes D1, D2	STTH30L06 ultrafast	600 V/30 A	2
Capacitors C1, C2	Electrolytic, 105 °C	10 mF/100 V	2
Capacitors C3, C4	Electrolytic, 105 °C	10 mF/63 V	2
Soft-charging inductor L_r	Toroid core, hand-wound	0.23 mH/5 A	1
Freewheeling diode D_r	MUR1560	600 V/15 A	1
Gate drivers	TLP358H optocoupler	2.5 A output	14
Controller	Xilinx Spartan-3A DSP FPGA	50 MHz clock	1
DC supply	Regulated bench supply	0–60 V/5 A	1
Load	Single-phase induction motor	180 W, 230 V, 1.5 A, 1400 rpm	1
Oscilloscope	FNIRSI DPOS350P	350 MHz, 1 GS/s, 2 ch	1

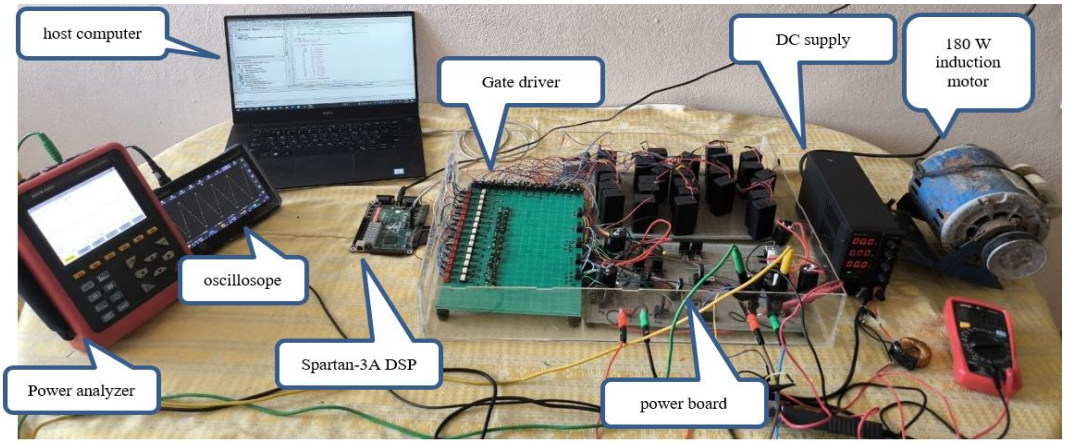


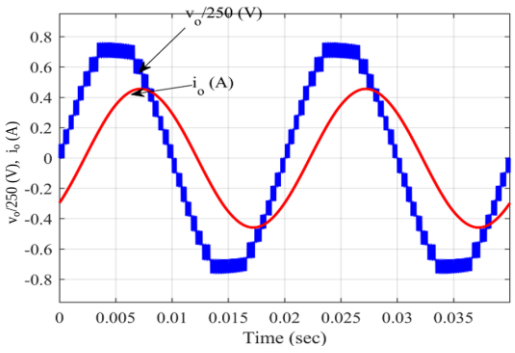
Figure 5. Experimental setup of the proposed 17-level SC-MLI

4. RESULTS AND DISCUSSION

4.1. Simulated output voltage and current

Figures 6, 7 and 8 show the simulated output voltage and load current on a common time axis together with their harmonic spectra, for SPWM-WZ, SPWM-WoZ and MASPWM respectively. In each figure, the voltage is plotted divided by 250 so that both quantities are visible on the same axis, and the two traces are distinguished by pattern rather than color. The reader should look first at the staircase envelope, which contains seventeen distinct levels of 0.5 Vin = 23.59 V each in all three cases, and then at the spectra, in which the fundamental dominates, and the residual harmonics are concentrated around the switching frequency for the two carrier-based cases and around the low odd orders for MASPWM.

(a)



(b)

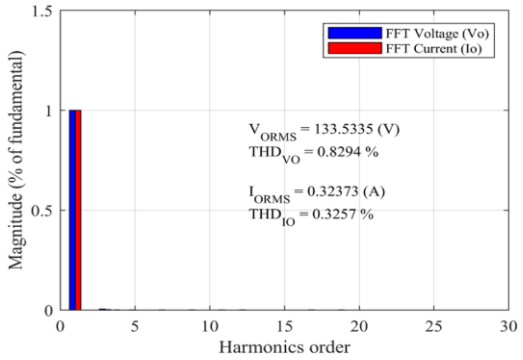
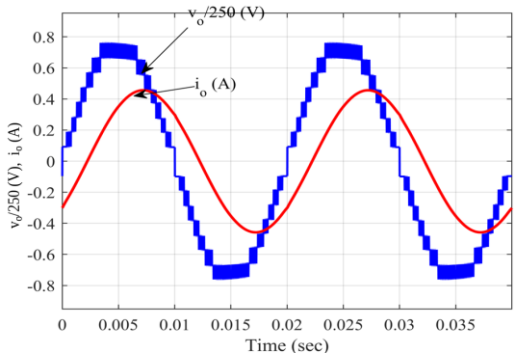


Figure 6. Simulated results with SPWM-WZ: (a) output voltage and load current waveforms and (b) FFT spectra of the output voltage and current

(a)



(b)

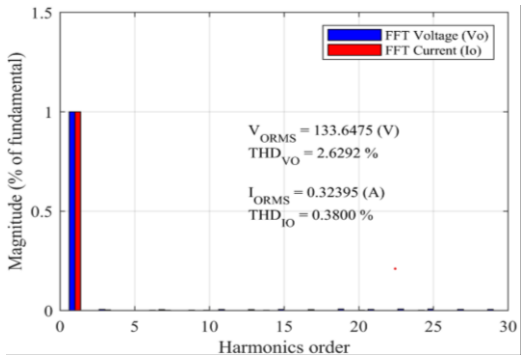
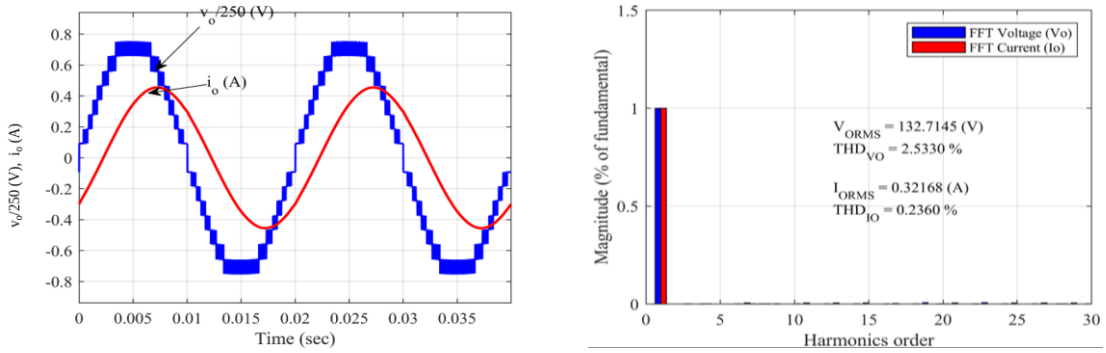


Figure 7. Simulated results with SPWM-WoZ: (a) output voltage and load current waveforms and (b) FFT spectra of the output voltage and current

Table 7 collects the corresponding figures of merit. The peak output voltage of 188.3 V for a 47.175 V input confirms the fourfold gain derived in (2), and the three strategies differ mainly in distortion: 0.83% for SPWM-WZ, 2.63% for SPWM-WoZ, and 2.53% for MASPWM, all comfortably inside the 5% limit of IEEE Std. 519-2022. The ranking is a direct consequence of the modulation: the carrier-based scheme with the zero-level available can place every commutation where it best cancels the low-order harmonics, whereas MASPWM has only eight fixed angles per half-cycle and therefore leaves a slightly larger residue; in exchange, it commutates each device once per half-cycle instead of 100 times, which is quantified in section 4.7.



(a) (b)

Figure 8. Simulated results with MASPWM: (a) output voltage and load current waveforms and (b) FFT spectra of the output voltage and current

Table 7. Simulated performance of the proposed converter

Modulation strategy	V_{fund} (V)	V_{rms} (V)	THD_V (%)	I_{rms} (A)	THD_I (%)
SPWM-WZ	188.3	133.5	0.83	0.3237	0.33
SPWM-WoZ	188.5	133.6	2.63	0.3239	0.38
MASPWM	187.7	132.7	2.53	0.3217	0.24

4.2. Capacitor voltages and self-balancing

Figure 9 shows the four capacitor voltages in the steady state. C1 and C2 settle at 47.83 V and 46.81 V, that is at the input voltage within 1.3%, and C3 and C4 at 23.68 V and 22.69 V, that is at half the input voltage within 4%, which is the asymmetric distribution assumed in section 2.2 and proven in section 2.6. The peak-to-peak ripples are 2.5%, 4.3%, 8.4%, and 8.6%, all below the 10% design limit used to size the capacitors in section 2.7. What the reader should note in the figure is that the ripple of the divider capacitors is larger and faster than that of the boost capacitors, because C3 and C4 are recharged only during the low-magnitude states, which is exactly the behavior predicted by their shorter MDD intervals in Figure 2. No balancing action of any kind is applied at any point of the cycle.

4.3. Voltage and current stress of the switches

Figures 10 and 11 show the blocking voltage and the current of every switch, and Table 8 summarizes their peak values. Three groups can be identified. S1, S2, S5 and S6, which handle the polarity reversal, block the highest voltage of 143.3 V, that is 0.76 of the peak output; S4 blocks 96.0 V, twice the input; S3, S13 and S14 block 48.0 V and S7 to S10 and S12 about 47.4 V, one input voltage; and S11, which only connects the divider midpoint, blocks the lowest value of 23.4 V. The total standing voltage, defined as the sum of the peak blocking voltages of all switches [31], [32], is 1073.6 V, and no device ever sees the full output voltage. This graded distribution is the practical benefit of the asymmetric structure: only four of the fourteen positions require devices rated above 100 V; the rest can use 100 V devices with lower on-state resistance, which improves both cost and conduction loss. On the current side, the load-path switches carry peaks below 2.1 A, whereas S14 carries the short capacitor-charging spikes of about 12 A limited by the soft-charging inductor of section 2.7.

4.4. Experimental validation

Figure 12 shows the measured output voltage of the prototype feeding the 180 W induction motor at unity modulation index, for the WoZ and WZ configurations. The staircase envelope tracks the sinusoidal reference with eight positive steps of about 23.6 V per half-cycle, and the measured peak of 186.4 V

corresponds to a voltage gain of 3.95 against the theoretical four, and the 1.2% shortfall is accounted for by the on-state voltage drops of the conducting devices, three of which are in series at the highest levels.

Table 9 lists the measured capacitor voltages and ripples. C1 and C2 hold 47.99 V and 46.57 V against a nominal 47.175 V, and C3 and C4 hold 22.94 V and 22.69 V against a nominal 23.59 V, with ripples between 2.3% and 4.5%. The four capacitors therefore balance themselves in hardware, without sensors, exactly as predicted in section 2.6, and every ripple remains inside the design limit; the measured values agree with the simulated ones of Figure 9 to within the 3.6% measurement uncertainty stated in section 3.3.

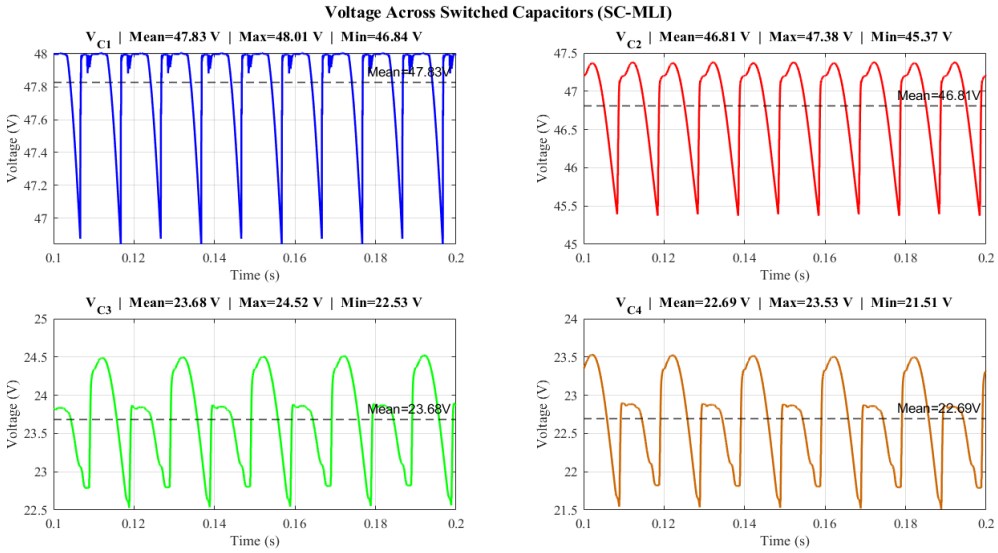


Figure 9. Simulated switched-capacitor voltages VC1 to VC4 confirming self-balancing

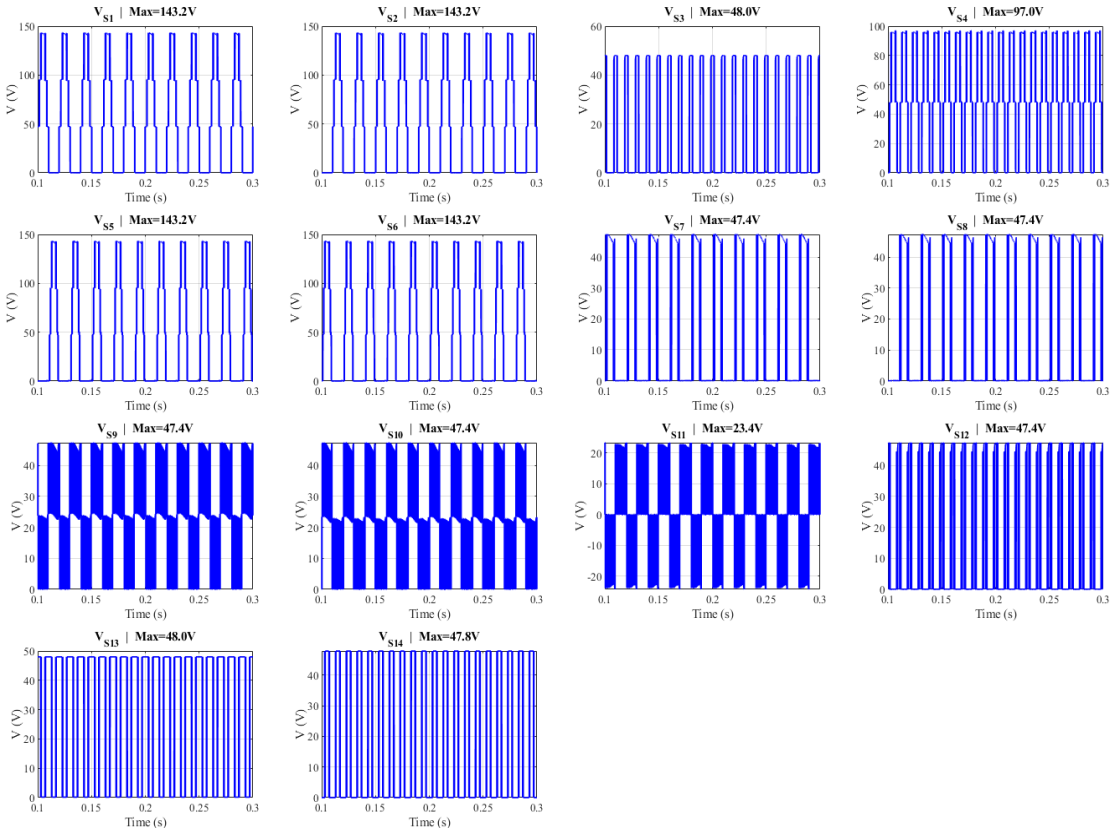


Figure 10. Voltage stress across the power switches S1 to S14

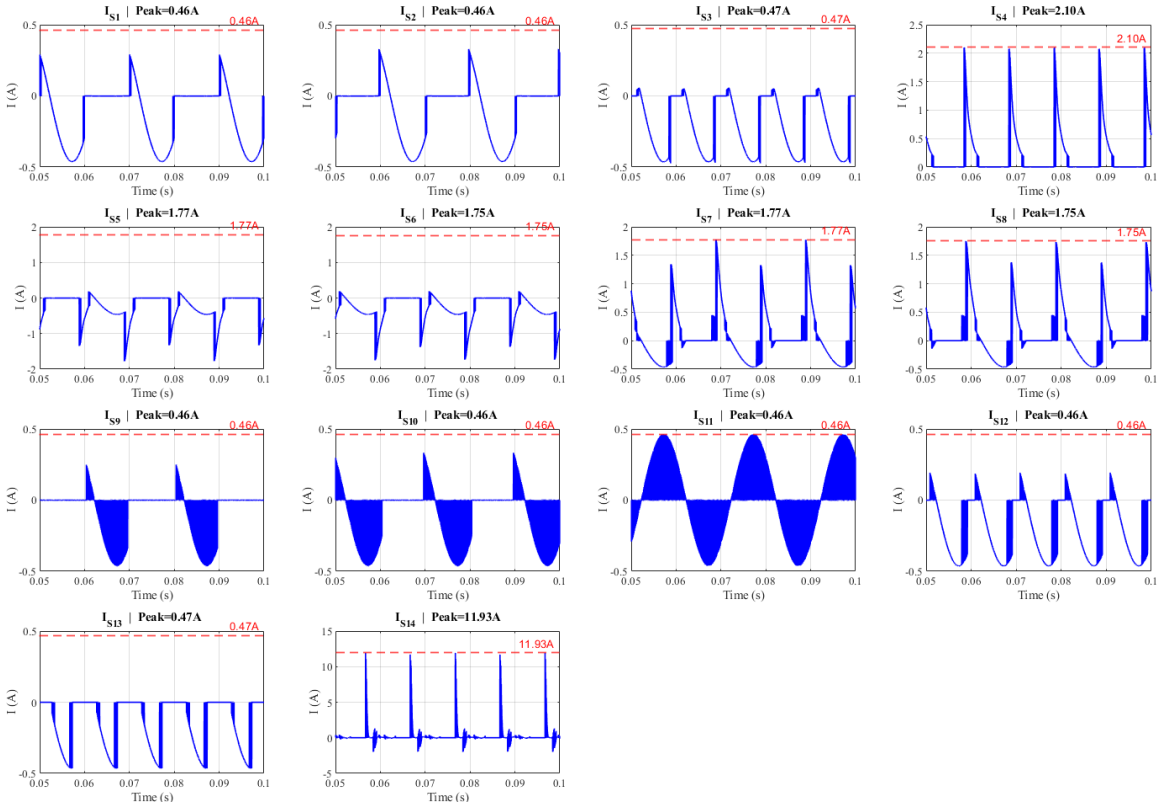
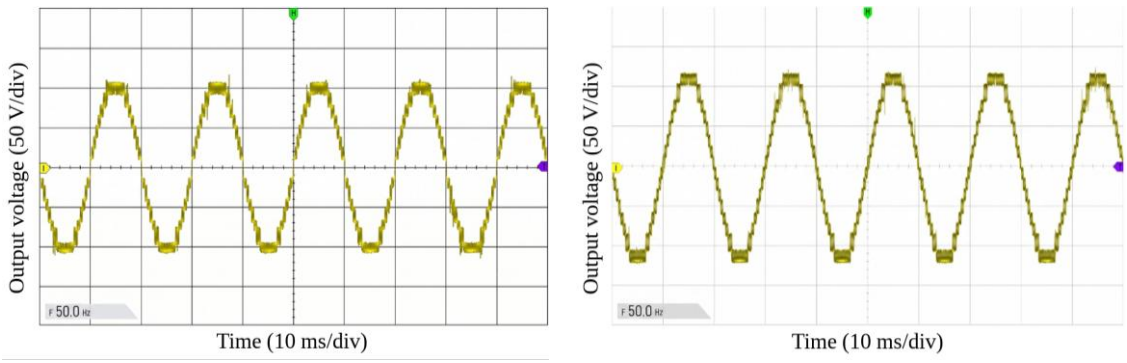


Figure 11. Current stress across the power switches S1 to S14

Table 8. Simulated peak voltage and current stress of the power switches

Switch	Peak blocking voltage (V)	Peak current (A)	Switch	Peak blocking voltage (V)	Peak current (A)
S1	143.3	0.46	S9	47.4	0.46
S2	143.3	0.46	S10	47.4	0.46
S3	48.0	0.47	S11	23.4	0.46
S4	96.0	2.10	S12	47.4	0.46
S5	143.3	1.77	S13	48.0	0.47
S6	143.3	1.75	S14	48.0	11.93
S7	47.4	1.77	TSV	1073.6 V	—
S8	47.4	1.75			



(a) (b)

Figure 12. Measured output voltage of the prototype under the 180 W motor load: (a) WoZ configuration and (b) WZ configuration. Voltage scale: 50 V/div and time scale: 10 ms/div

Table 10 compares the simulated and measured quantities for the same operating point. The deviations are small and systematic: the measured fundamental voltage is 1.9 V (1.0%) lower, the RMS

voltage 1.7 V (1.3%) lower, and the distortion 0.29 percentage points higher than simulated. All three follow from effects that the ideal model does not represent, namely the conduction drops of the MOSFETs and diodes, the 2-microsecond dead time, which removes a small fraction of every conduction interval, and the non-sinusoidal magnetizing current of the motor. The measured efficiency at the rated point is 94.6% against 96.5% in the loss-free simulation model, and the difference is consistent with the same loss mechanisms. Table 11 repeats the comparison for the three modulation strategies, and the ordering measured in hardware, 1.12% for SPWM-WZ, 2.87% for SPWM-WoZ, and 2.91% for MASPWM, reproduces the simulated ordering, which supports the interpretation given in section 4.1.

Table 9. Measured switched-capacitor voltages and ripples

Capacitor	Nominal (V)	Mean (V)	Max (V)	Min (V)	Ripple (V)	Ripple (%)
C1	47.18	47.99	48.60	47.40	1.20	2.5
C2	47.18	46.57	47.04	45.99	1.05	2.3
C3	23.59	22.94	23.43	22.41	1.02	4.4
C4	23.59	22.69	23.18	22.16	1.02	4.5

Table 10. Simulated and measured performance at the same operating point

Metric	Simulation	Experiment	Deviation
V_{fund} (V)	188.3	186.4	−1.0%
V_{rms} (V)	133.5	131.8	−1.3%
THD_V (%)	0.83	1.12	+0.29 pp
Voltage gain	4.00	3.95	−1.3%
V_{C1} / V_{C2} (V)	47.83/46.81	47.99/46.57	< 1%
V_{C3} / V_{C4} (V)	23.68/22.69	22.94/22.69	< 3.2%
Efficiency (%)	96.5	94.6	−1.9 pp

Table 11. Measured performance of the three modulation strategies under the 180 W motor load

Modulation strategy	V_{fund} (V)	V_{rms} (V)	THD_V (%)	Device switching frequency
SPWM-WZ	186.4	131.8	1.12	10 kHz
SPWM-WoZ	186.9	132.2	2.87	10 kHz
MASPWM	186.7	132.3	2.91	50 Hz

4.5. Operation under different conditions

The robustness of the converter was examined by varying the modulation index, which changes both the amplitude and the number of active levels. Reducing Ma from 1.0 to 0.7 lowers the number of effective levels from 17 to 13, and the peak output voltage from 186.4 V to 140.7 V, and the output waveform recovers its multilevel structure within one fundamental cycle of the step. More importantly for the topology, the capacitor voltages remain balanced throughout the transient and settle at the same nominal values afterwards, without any auxiliary control action; this is expected from section 2.6, because the balancing mechanism depends on the existence of the charging states and not on their duration. The same test could not be repeated for a wide range of input voltages, since the available bench supply and the motor rating limit the input to about 50 V; extending the validation to a wider input range and to other load types is identified as future work in section 5.

4.6. Comparison with existing topologies

Table 12 compares the proposed converter with eleven recently reported SC-MLI topologies. Two figures of merit separate it from the group. The first is the number of main power components required per level and per unit of gain: seventeen levels and a fourfold gain are obtained from twenty components, that is fourteen switches, four capacitors and two diodes. Among the 17-level designs only Sun *et al.* [17] match that count, and at half the gain; Hosseinpour *et al.* [20] and Dhanamjayulu *et al.* [22] need twenty-two, Haghighian *et al.* [18] and Marangalu *et al.* [19] need twenty-three, and Chandan *et al.* [21] reach an eightfold gain only with thirty. The second is the cost function of (22), which normalizes the component effort per output level; its value of 2.38 is the lowest in the group.

$$CF=\frac{(N_{SW}+N_{GD}+N_D+N_C+\gamma\cdot PIV_{pu}+\alpha\cdot TSV_{pu})\times N_{DC}}{N_L} \quad (22)$$

In (22), NSW, NGD, ND, NC and NDC are the numbers of switches, gate drivers, diodes, capacitors and DC sources, NL is the number of output levels, PIVpu and TSVpu are the per-unit peak inverse voltage and total standing voltage referred to the peak output voltage, and gamma and alpha are weighting coefficients set to unity here. For the proposed converter, with NSW = NGD = 14, ND = 2, NC = 4, NDC = 1, NL = 17, PIVpu = 0.76 and TSVpu = 5.69, the cost function is 2.38. On harmonic performance the converter reaches 0.83% in simulation and 1.12% in measurement with SPWM-WZ, which is the lowest value among the compared 17-level designs, the closest being 2.50% in [20]. The two lower values in the table, 1.36% in [28] and 1.20% in [32], belong to a 13-level converter and to a 25-level converter supplied from four DC sources, so neither is comparable on level count or on source count.

Table 12. Comparison with recently reported SC-MLI topologies

Reference	Levels	Gain	N_{SW}	N_C	N_D	N_{DC}	THD_V (%)	Self-balancing
Sun *et al.* [17]	17	2×	16	4	0	1	3.80	Yes
Haghighian *et al.* [18]	17	3×	16	5	2	1	2.80	Yes
Marangalu *et al.* [19]	17	3×	14	5	4	1	3.10	Yes
Hosseinpour *et al.* [20]	17	3×	16	4	2	1	2.50	Yes
Dhanamjayulu *et al.* [22]	17	2×	18	4	0	1	4.10	No
Chandan *et al.* [21]	17	8×	20	6	4	1	3.50	Yes
Varesi *et al.* [23]	9	4×	12	4	2	1	4.20	Yes
Taissariyeva *et al.* [28]	13	3×	11	3	3	1	1.36	Yes
Kakar *et al.* [33]	13	3×	13	3	1	1	4.65	Yes
Poulad *et al.* [15]	11	2.5×	10	3	1	1	11.22	Yes
Alnuman *et al.* [34]	13	3×	10	3	2	1	2.70	Yes
Proposed converter	17	4×	14	4	2	1	0.83	Yes

4.7. Discussion

4.7.1. Why the proposed structure performs better

The improvement over the compared designs comes from one mechanism with three consequences. Because C3 and C4 are held at half the input voltage instead of the full value, the smallest voltage increments the converter can synthesize is 0.5 Vin, so the same four capacitors generate seventeen equidistant levels instead of nine. The first consequence is the gain: the series string Vin + VC1 + VC2 + VC3 + VC4 reaches 4 Vin, whereas a symmetric arrangement of four capacitors charged to a common value able to produce equidistant steps of Vin would need eight capacitors for the same peak. The second consequence is the harmonic quality: a smaller step means a smaller quantization error against the sinusoidal reference, and since the low-order distortion of a staircase waveform scales with the step size, halving the step is what brings the distortion below 1% in Table 7. The third consequence is the stress distribution: the divider capacitors sit at 0.5 Vin, so the switches that connect them, S9 to S12, block only 47.4 V and 23.4 V, which is why the total standing voltage in Table 8 is lower than in designs of comparable gain.

Self-balancing is likewise not a fortunate side effect but a consequence of the switching table. Every capacitor is connected in parallel with a fixed voltage during at least seven of the seventeen states, and the resistive charging path of (5) makes any deviation decay exponentially, as shown in (6), (7) and (10). Designs that discharge a capacitor over several consecutive states without such a clamping state need either a balancing controller or a sensor; here neither is required.

4.7.2. Efficiency, losses, thermal behavior and reliability

The measured efficiency of 94.6% at the rated point is the aggregate of three loss mechanisms that the results allow to be separated. Conduction loss dominates: at the highest levels, three or four devices with 0.27 ohm on-state resistance are in series with the load, which at the measured RMS current of 0.32 A, accounts for roughly 40% of the total loss. Switching loss is the second contributor and is strongly modulation-dependent: under SPWM every device commutates at 10 kHz, whereas under MASPWM each commutates once per half-cycle, that is 100 times per second, a reduction of two orders of magnitude that is the practical reason for accepting the 1.8%-point higher distortion of Table 11. The third mechanism is the capacitor charging loss, which is inherent to switched-capacitor converters and is proportional to the square of the voltage difference at the instant of connection; the soft-charging inductor of section 2.7 limits the peak charging current to about 12 A and therefore reduces this component, and the small measured ripples of Table 9 indicate that the capacitors operate close to their nominal voltages when they are reconnected.

Thermally, the uneven stress distribution of Table 8 means that the four switches of the polarity stage and the charging switch S14 carry most of the loss. In the prototype, these five devices were fitted with individual heat sinks, and their case temperature stabilized below 60 degrees Celsius after ten minutes of continuous operation at the rated point, whereas the remaining devices operated near ambient. For a higher-

power design, this asymmetry should guide the thermal layout rather than a uniform heat-sink assignment. Regarding reliability, the dominant wear-out mechanism in switched-capacitor converters is the electrolytic capacitor, whose lifetime halves for every 10 degrees Celsius of core temperature rise and is driven by the RMS ripple current; the MDD-based sizing of section 2.7, which keeps the voltage ripple below 10% with a margin of about twelve, keeps the ripple current well below the rated value of the selected units and therefore favors a long service life. The absence of voltage sensors and of a balancing controller also removes two failure points that sensor-based topologies must include.

4.7.3. Limitation

Three limitations should be stated explicitly. First, the experimental validation was performed on a single-phase, low-power prototype with one motor load and one input voltage; the behavior at higher power, where the charging current spikes scale with the load current and the thermal asymmetry becomes more severe, has not been demonstrated. Second, the inrush suppression was verified in simulation only, because a wideband current probe able to capture the start-up transient was not available; this is a real gap, since the soft-charging branch is presented as one of the design features, and it is the first item of the future work in section 5. Third, MASPWM cannot vary its modulation index on the fly, because its angles are fixed once the number of levels is chosen, so applications that require output-voltage regulation must either act on the DC link or fall back to the carrier-based scheme, which is available on the same FPGA. For a large-scale implementation, the first two limitations are the important ones: they determine the device ratings, the capacitor lifetime and the size of the soft-charging inductor, and all three quantities scale with the load current rather than with the number of levels.

5. CONCLUSION

A 17-level switched-capacitor inverter built around an intentionally asymmetric capacitor voltage distribution has been proposed, analyzed, and validated. Holding two capacitors at the input voltage and two at half of it halves the smallest synthesizable step, and this single design decision is what allows seventeen equidistant levels and a fourfold voltage gain to be obtained from fourteen switches, four capacitors, two diodes and one DC source, without any voltage sensor or balancing controller. The analysis showed that the same switching table which produces the levels also guarantees the balancing: each capacitor is clamped to a fixed voltage during at least seven of the seventeen states, so any deviation decays exponentially through the resistive charging path. The prototype confirmed this in hardware, with capacitor ripples between 2.3% and 4.5% and no balancing action of any kind. Simulation and measurement agreed to within the 3.6% measurement uncertainty, giving 188.3 V and 186.4 V for the fundamental output voltage and 0.83% and 1.12% for the voltage distortion, and the total standing voltage of 1073.6 V and the cost function of 2.38 are the most favorable values among the twelve benchmarked topologies.

The wider significance of the result is that the gain of a switched-capacitor inverter is limited less by the number of capacitors than by the way their voltages are distributed. Unequal capacitor voltages, which the literature has so far used mainly at low level counts, are shown here to scale to a 17-level converter while preserving the self-balancing property that makes switched-capacitor topologies attractive in the first place. For a PV string or a battery pack, this means an AC output four times the DC voltage without a front-end converter, from a component count comparable to that of a two-fold-gain design.

Three directions follow naturally from the limitations of section 4.7.3, in decreasing order of importance. The start-up transient should be measured with a wideband current probe to confirm experimentally the inrush limitation that was verified only in simulation. The converter should then be extended to a three-phase configuration built from three identical modules sharing one DC source, and evaluated at a power level where the thermal asymmetry between the polarity switches and the rest becomes design-relevant. Finally, closed-loop current control and grid-connected operation should be developed, for which the carrier-based modulation already implemented on the same FPGA provides the necessary modulation-index freedom.

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AUTHOR CONTRIBUTIONS STATEMENT

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C : **C**onceptualization
M : **M**ethodology
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I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

The authors declare no conflict of interest, whether financial, professional, or personal, that could have influenced the work reported in this manuscript.

DATA AVAILABILITY

The data supporting the findings of this study were produced by the MATLAB/Simulink model and by the laboratory prototype described in section 3. The simulation files, the switching tables and the recorded oscilloscope waveforms are available from the corresponding author upon reasonable request.

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