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High-gain multi-stage interleaved DC–DC converter with fuzzy logic control for electric vehicle applications

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ABSTRACT

High-gain DC–DC converters are essential for interfacing low-voltage batteries with high-voltage DC buses in electric vehicles (EVs). This study proposes a three-stage cascaded interleaved high-gain DC–DC converter with a dual-floating-output configuration for battery-powered EV applications. The converter increases a 24 V battery input to approximately 600 V, achieving an overall voltage gain of 25. A Mamdani-type fuzzy logic controller regulates the duty cycle based on output-voltage error and its rate of change. MATLAB/Simulink simulations evaluate voltage conversion, transient response, current behavior, and voltage stability. The results demonstrate stable 24 V-to-600 V conversion with coordinated operation of the three cascaded stages. The proposed configuration provides a modular approach to high-gain DC–DC conversion for EV applications and a basis for future studies on bidirectional operation and hybrid energy sources.

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1. INTRODUCTION

Electric vehicles (EVs) require efficient power conversion systems to interface low-voltage, high-current batteries with high-voltage DC buses. High-gain DC–DC converters are therefore essential for achieving large voltage conversion ratios while maintaining acceptable current ripple, semiconductor stress, and dynamic performance [1], [2]. Conventional single-stage boost converters require high duty ratios to obtain large voltage gains, which can increase conduction losses and semiconductor stress. High step-up converter topologies have therefore been developed to increase voltage gain and improve the suitability of DC–DC conversion for low-voltage energy sources [3]. Interleaved and floating-output converter structures can further provide parallel current paths and improved current characteristics [4], [5]. Intelligent control techniques have also been investigated for EV power conversion, including fuzzy-logic-based motor control and neural-network-based regulation of interleaved converters [6].

Various non-isolated high-gain converter configurations have been proposed to address the limitations of conventional boost converters. Multi-input structures provide flexible energy-source integration and current-sharing capability [7], while coupled-inductor and switched-capacitor techniques can increase voltage gain and manage semiconductor voltage stress [8]. Fuzzy-logic control has also been applied to hybrid EV energy-management systems under varying operating conditions [9]. Floating-output

interleaved-input converters have demonstrated high voltage gain through distributed current paths [10], while other high step-up structures have focused on reducing input-current ripple [11]. Fuzzy-based energy-management approaches have further been investigated for hybrid EV applications [12]. Multi-input converters with inherent current-sharing mechanisms have been developed for renewable-energy systems [13], followed by improved multi-input structures with enhanced voltage gain and current distribution [14]. Coupled-inductor and voltage-multiplier techniques have also been studied for high step-up conversion while considering semiconductor stress and conversion losses [15].

Recent studies have further investigated intelligent control and high-gain conversion for EV applications. Fuzzy logic has been used for dynamic energy optimization in EV propulsion systems [16], while an interleaved DC–DC converter supplied by a 24 V battery has been investigated for high-voltage EV applications [17]. Transformerless high-gain converters have also been proposed to achieve high voltage conversion without a high-frequency transformer [18]. Extended switched-capacitor structures have been developed to increase voltage gain while reducing voltage stress on switches and diodes [19]. Diode–capacitor-cell-based high step-up converters have likewise been proposed to achieve high voltage gain while limiting conduction and switching losses [20]. These studies indicate that voltage gain, current distribution, ripple characteristics, semiconductor stress, and control complexity are important considerations in high-gain converter design. However, the voltage contribution of individual cascaded stages and their coordinated control remain insufficiently investigated, particularly for low-voltage battery sources.

This study investigates a three-stage cascaded interleaved high-gain DC–DC converter with a dual-floating-output configuration for battery-powered EV applications. The proposed converter converts a 24 V battery input to approximately 600 V DC, corresponding to an overall voltage gain of about 25. The cascaded structure distributes the voltage conversion across three stages, while the interleaved branches provide parallel current paths. A Mamdani-type fuzzy logic controller regulates the converter duty cycle using the output-voltage error and its rate of change. The converter is modeled in MATLAB/Simulink to evaluate duty-cycle response, intermediate voltages, terminal and inductor currents, capacitor voltages, and transient behavior. The main contribution is the simulation-based evaluation of the combined cascaded interleaved topology, dual-floating-output configuration, and fuzzy-logic voltage regulation for 24 V-to-600 V conversion. The study focuses on forward power flow and does not demonstrate bidirectional operation or experimental validation.

2. METHOD

Figure 1(a) shows the proposed three-stage cascaded interleaved high-gain DC–DC converter for battery-powered EV applications. The converter is supplied by a 24 V battery and uses a fuzzy logic controller (FLC) to regulate the output voltage. The cascaded architecture distributes the overall voltage conversion across three stages, reducing the need for a high duty ratio in a single stage and providing a structured high-gain conversion process [21], [22].

The battery supplies the first conversion stage through the input inductors, which store and release energy according to the switching states. The energy is transferred sequentially through the cascaded stages to obtain the required high-voltage output. In the considered simulation, the voltage is increased from approximately 24 V to intermediate levels of 90 V and 250 V before reaching approximately 600 V. The intermediate voltages are used to evaluate the voltage contribution of each stage [23], [24].

Figure 1(b) shows the interleaved conversion stage. Each stage consists of two parallel boost branches operating with a 180° phase shift [25], [26]. The interleaved arrangement distributes the input current between the branches and provides partial ripple cancellation [27], [28]. The total input current is expressed as (1).

$$i_{\text{in}}(t) = i_{L1}(t) + i_{L2}(t) \tag{1}$$

i_{L1} and i_{L2} are the currents through the two interleaved inductors. Under balanced operation, the average branch currents are expected to be similar, while the difference between the maximum and minimum total input current represents the input-current ripple [29]. The overall voltage gain of the proposed converter is as in (2).

$$G_{\text{total}} = \frac{V_o}{V_{\text{in}}} = \frac{600}{24} = 25 \tag{2}$$

V_{in} and V_o are the battery input and final output voltages, respectively. The gain of each cascaded stage is determined by (3):

$$G_1 = \frac{V_1}{V_{\text{in}}},\ G_2 = \frac{V_2}{V_1},\ G_3 = \frac{V_o}{V_2} \tag{3}$$

and therefore:

$$G_{\text{total}} = G_1 G_2 G_3 \tag{4}$$

This stage-by-stage formulation allows the voltage contribution of each conversion stage to be evaluated independently.

Figure 2 presents the closed-loop FLC used to regulate the converter output voltage. The measured output voltage is compared with the reference to obtain the voltage error:

$$e(k) = V_{\text{ref}}(k) - V_o(k) \tag{5}$$

and its change:

$$\Delta e(k) = e(k) - e(k-1) \tag{6}$$

These two variables are supplied to a Mamdani-type fuzzy inference system to determine the required duty-cycle control action [25], [26], [30].

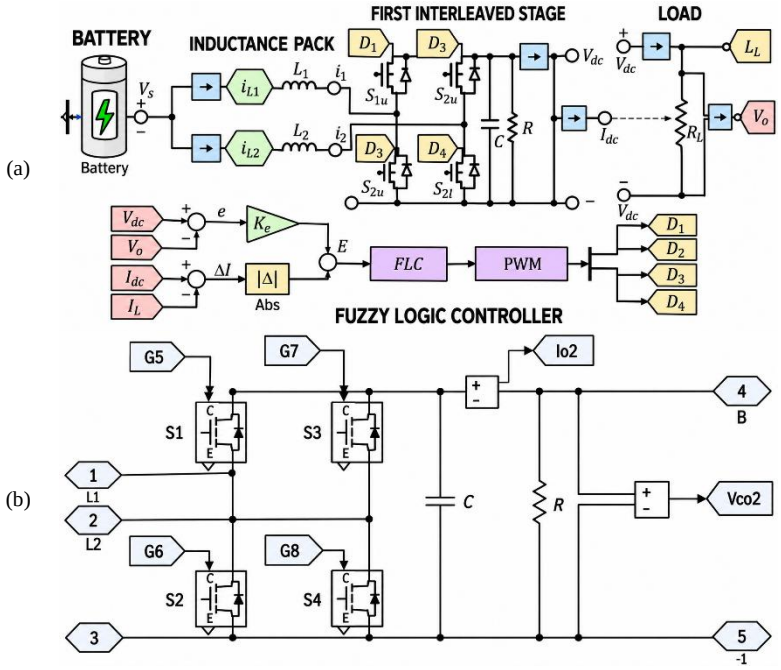

Figure 1. Topologies of the proposed 24 V/600 V DC/DC converter: (a) three-stage converter and (b) first interleaved-stage converter

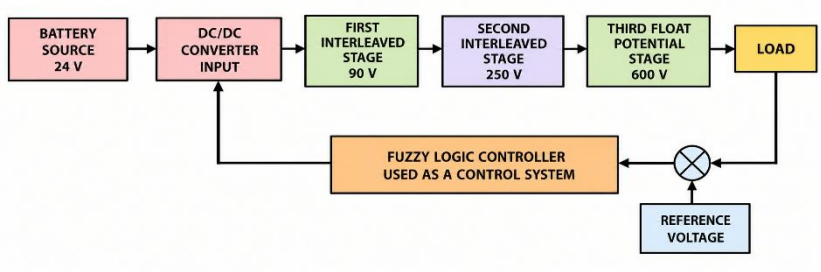

Figure 2. Closed loop DC/DC converter using FLC

Five linguistic variables are used for each input: negative big (NB), negative small (NS), zero (ZE), positive small (PS), and positive big (PB). Triangular membership functions are used for the intermediate

regions and trapezoidal functions at the boundaries. The fuzzy output is converted to a crisp control signal using centroid defuzzification and subsequently applied to the pulse width modulation (PWM) generator. The normalized controller inputs are defined as (7).

$$e_n = K_e e \text{ and } \Delta e_n = K_{\Delta e} \Delta e \quad (7)$$

K_e and $K_{\Delta e}$ are the corresponding scaling factors. The controller parameters and membership-function ranges should be specified in the simulation parameter table to ensure reproducibility. For each boost stage, the ideal voltage conversion relationship is as in (8):

$$V_o = \frac{V_{\text{in}}}{1-D} \quad (8)$$

or equivalently as (9).

$$D = 1 - \frac{V_{\text{in}}}{V_o} \quad (9)$$

D is the duty ratio of the corresponding stage. Thus, the duty ratio is determined separately for each cascaded stage rather than from the overall 24 V-to-600 V conversion ratio. For continuous-conduction operation, the required inductance can be estimated from (10).

$$L = \frac{V_{\text{in}} D}{\Delta I_L f_s} \quad (10)$$

L is the branch inductance, ΔI_L is the allowable inductor-current ripple, and f_s is the switching frequency. The output capacitance can be estimated from:

$$C = \frac{I_o D}{\Delta V_o f_s} \quad (11)$$

C, I_o, and ΔV_o represent the output capacitance, load current, and allowable output-voltage ripple, respectively. The proposed converter is evaluated using MATLAB/Simulink under the specified input voltage, intermediate voltage levels, output voltage, switching parameters, passive components, and load conditions. The evaluation considers duty-cycle response, intermediate and output voltages, inductor and terminal currents, capacitor voltages, and transient behavior. Where applicable, semiconductor voltage and current stresses can be obtained from the simulated switching waveforms. Overall, the methodology evaluates the combined effects of the cascaded architecture, interleaved current paths, and fuzzy-logic voltage regulation in achieving high-gain conversion from a 24 V battery to approximately 600 V. The analysis is limited to forward power flow and the simulation conditions considered in this study.

3. RESULTS AND DISCUSSION

3.1. Results

Figure 3 shows the complete MATLAB/Simulink model developed to evaluate the proposed three-stage cascaded interleaved high-gain DC–DC converter. The simulation model consists of a 24 V lithium-ion battery source, three cascaded conversion stages, interleaved switching branches, intermediate energy-storage elements, a FLC, voltage and current measurement blocks, and the output load. The converter is evaluated under a forward power-flow condition in which electrical energy is transferred from the low-voltage battery source toward the high-voltage DC output. The simulation is used to examine the voltage conversion process, duty-cycle response, terminal currents, inductor currents, and capacitor voltages of the proposed converter. Figure 4 presents the battery terminal voltage during the 0.5 s simulation interval. The battery voltage increases rapidly from the initial condition and reaches approximately 24 V within the first 40–50 ms. After reaching the steady-state value, the voltage remains approximately constant at 24 V throughout the remaining simulation interval. No significant oscillation is observed in the displayed waveform. The result indicates that the battery-side voltage remains stable while supplying the cascaded converter stages.

The observed startup behavior is important because the converter contains several energy-storage elements that must be charged during initialization. The gradual convergence of the battery terminal voltage indicates that the startup process does not produce a sustained disturbance at the battery voltage. However, the battery-voltage waveform alone is not sufficient to quantify the battery current stress or input-current ripple. Therefore, the modulation duty cycles in Figure 5 and the cascaded output voltages in Figure 6 are examined next to explain the converter's progressive voltage buildup and its response to sequential duty-

cycle adjustments. The input-current waveforms presented in Figure 7 are subsequently analyzed to provide further insight into the current stress and ripple during startup and steady-state operation. Based on Figure 4, the steady-state battery voltage remains close to its nominal value, although the exact ripple percentage should be calculated from the simulation data rather than estimated solely from the plotted waveform.

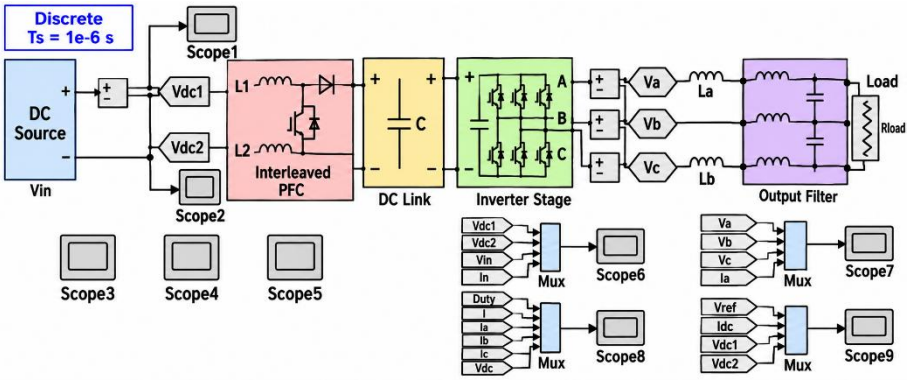

Figure 3. MATLAB simulation of 24 V/600 V proposed converter

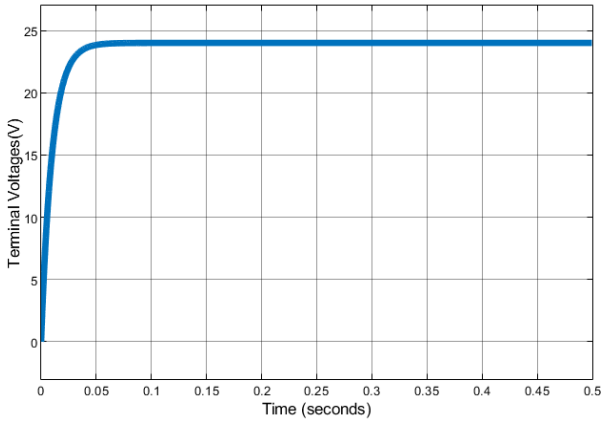

Figure 4. Input terminal voltage of battery

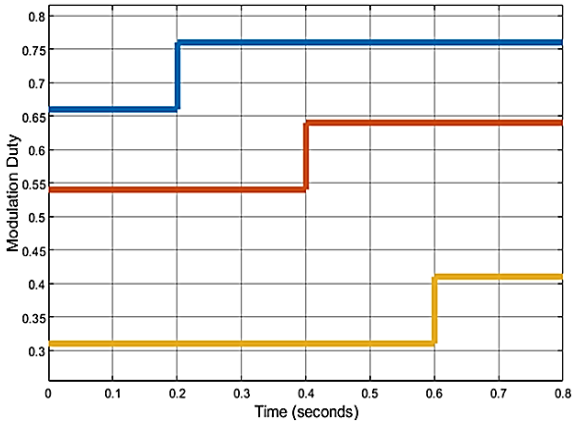

Figure 5. Modulation duty of three stages

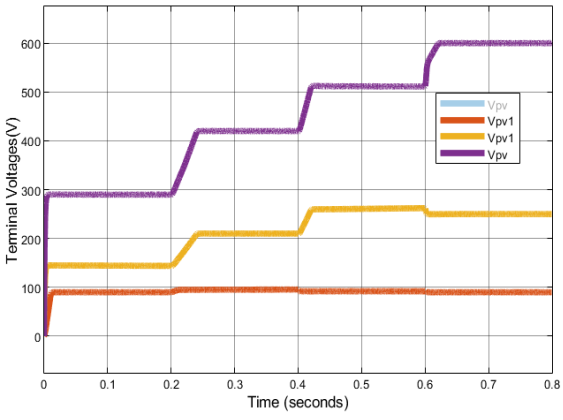

Figure 6. Terminal voltages of three stages

Figure 5 presents the modulation duty cycles of the three converter stages. The duty ratios are adjusted sequentially at approximately 0.2 s, 0.4 s, and 0.6 s. The first-stage duty ratio increases from approximately 0.66 to 0.76, the second from 0.54 to 0.64, and the third from 0.31 to 0.41. These changes correspond to the progressive voltage buildup shown in Figure 6. The different duty ratios result from the

different input voltage levels of each cascaded stage; therefore, identical duty ratios are not required to achieve the overall voltage conversion. The duty-cycle waveforms remain approximately constant between the transitions, indicating stable operating points under the considered simulation conditions [30], [31]. However, these results alone do not establish superior performance over a conventional PI controller. Such a comparison would require quantitative evaluation of settling time, overshoot, steady-state error, and voltage ripple. Figure 6 shows the terminal voltages of the cascaded converter. The voltage increases progressively from the low-voltage battery side to the final high-voltage output. The first intermediate voltage is maintained at approximately 90–95 V, while the high-voltage output increases successively from approximately 290 V to 420 V, 510 V, and finally 600 V following the duty-cycle transitions.

The voltage transitions in Figure 6 coincide with the duty-cycle changes in Figure 5, confirming the relationship between stage modulation and progressive voltage buildup. At approximately 0.2 s, 0.4 s, and 0.6 s, the increased duty ratios of the first, second, and third stages, respectively, produce successive increases in the converter voltage. Under the final operating condition, the converter achieves approximately 600 V from a 24 V input, corresponding to an overall voltage gain of approximately 25. No pronounced overshoot or sustained oscillation is observed following the major voltage transitions, indicating stable operation under the tested conditions. Nevertheless, quantitative transient metrics should be extracted for a rigorous assessment. The final output remains close to 600 V after approximately 0.6 s, demonstrating the high-gain conversion capability of the proposed cascaded configuration. Further comparison with conventional topologies should consider voltage gain, ripple, semiconductor stress, efficiency, and transient response.

Figure 7 presents the terminal currents measured at different points of the proposed converter during startup and subsequent operating transitions. A high transient current occurs at startup, particularly at the input, as the inductive and capacitive elements are initially energized. After this transient, the current decreases toward the operating level and changes in response to the duty-cycle transitions at approximately 0.2 s, 0.4 s, and 0.6 s.

At each transition, the current exhibits a temporary increase followed by a reduction toward a new operating level. These responses correspond to the duty-cycle changes in Figure 5 and the voltage transitions in Figure 6, indicating temporary energy redistribution within the cascaded stages. However, Figure 7 does not provide sufficient evidence to quantitatively evaluate current sharing or ripple cancellation because the individual interleaved branch currents are not separately shown. Figure 8 shows the inductor currents of the three converter stages. A pronounced startup transient is followed by a rapid reduction as the converter approaches its initial operating condition. Further current transitions occur at approximately 0.2 s, 0.4 s, and 0.6 s, consistent with the duty-cycle changes in Figure 5. The peak currents decrease after startup, while the average current levels change as the converter moves toward higher-voltage operating conditions. These responses reflect the redistribution of stored magnetic energy during changes in the converter operating point.

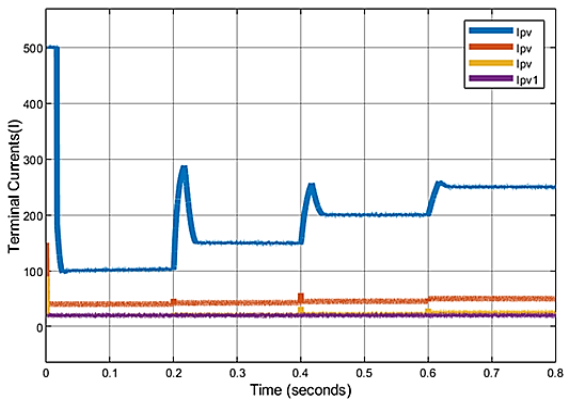

Figure 7. Terminal currents of three stages

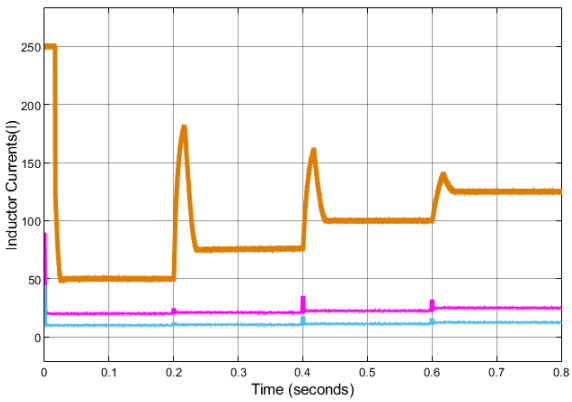

Figure 8. Inductor currents of three stages

The inductor-current waveforms can also be used to assess the interleaved operation. For a two-branch interleaved stage, effective current sharing is indicated by similar average branch currents with a 180° phase displacement, while ripple cancellation is reflected by reduced ripple in the combined current. Therefore, individual branch currents should be presented separately if available from the Simulink model. In the absence of such waveforms, the interleaving feature should be described as a topological characteristic rather than a quantitatively demonstrated improvement in current sharing or ripple reduction.

Figure 9 presents the capacitor-voltage waveforms during steady-state switching operation over the interval from approximately 0.4993 s to 0.5000 s. The capacitor voltages are approximately 90 V, 250 V, and 427 V for the corresponding intermediate nodes. Periodic switching ripple is observed around these average voltage levels, while the voltage variation remains relatively small compared with the corresponding DC levels. The capacitor voltages establish the intermediate DC levels required by the subsequent cascaded stages. Their relatively stable waveforms indicate that the energy-storage elements reach steady operating conditions under the simulated forward-power-flow condition. The observed ripple is associated with the switching operation and should be evaluated together with the inductor-current ripple to assess the overall filtering performance. Exact capacitor-ripple values should be obtained directly from the simulation data rather than estimated from the plotted waveform.

The results in Figures 4–9 demonstrate the sequential voltage conversion and regulation of the proposed converter from a 24 V battery source to approximately 600 V, corresponding to an overall voltage gain of 25. The duty-cycle, terminal-current, inductor-current, and capacitor-voltage responses are consistent with the sequential operation of the three cascaded stages. However, these results demonstrate only the simulated forward-power-flow operation and do not by themselves establish advantages in efficiency, EMI, fault tolerance, lifetime, or bidirectional power transfer. The relatively large capacitor values provide energy storage and help maintain stable intermediate voltage levels. However, larger capacitance also increases stored energy and may increase the startup inrush current. Therefore, the effects of capacitor sizing and startup control should be evaluated quantitatively in future work.

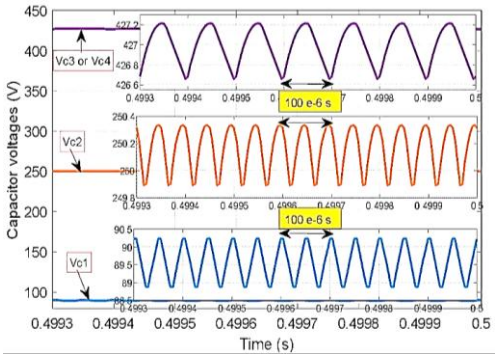

Figure 9. Capacitor voltages at state (simulation results)

3.2. Discussion

The simulation results confirm that the proposed three-stage cascaded interleaved converter can convert a 24 V battery input to approximately 600 V, achieving an overall voltage gain of 25. The sequential duty-cycle adjustments produce intermediate voltage levels of approximately 90–95 V, 250 V, and 427 V before reaching the final output. The relatively stable voltage and duty-cycle waveforms indicate proper operation of the proposed converter under the investigated conditions [3], [10], [15], [17]. The current and capacitor responses further demonstrate stable operation after startup and during operating-point transitions. The capacitor voltages remain around 90 V, 250 V, and 427 V with periodic switching ripple. Although the interleaved structure is intended to improve current distribution and reduce ripple [3], [13], [17], these benefits are not quantitatively verified because the individual branch currents are not separately presented. Therefore, the present study demonstrates forward 24 V-to-600 V conversion, while efficiency, semiconductor stress, bidirectional operation, and comparative performance require further investigation.

4. CONCLUSION

This study presented a three-stage cascaded interleaved high-gain DC–DC converter with fuzzy logic control for battery-powered EV applications. MATLAB/Simulink results demonstrated stable 24 V-to-600 V conversion with an overall voltage gain of 25 and sequential intermediate voltage buildup. The results confirm the feasibility of the proposed topology for high-gain DC conversion; however, further work is required to quantitatively evaluate efficiency, ripple, current sharing, semiconductor stress, PI-controller comparison, bidirectional operation, and experimental validation.

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AUTHOR CONTRIBUTIONS STATEMENT

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Sridevi Veerappan		✓				✓		✓	✓	✓	✓	✓		
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C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author, [TH], upon reasonable request.

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