International Journal of Power Electronics and Drive System (IJPEDS)
Vol. 7, No. 1, March 2016, pp. 124~133
ISSN: 2088-8694

Design of Three-Phase Three-Switch Buck-Type Rectifier for Pre-Charging Application

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Article Info

Article history:

Received Jul 11, 2015
Revised Dec 20, 2015
Accepted Jan 9, 2016

Keyword:

Peak current detection
Variable frequency drives
Zero crossing detection

ABSTRACT

The main objective of a pre-charging circuit in variable frequency drives is to pre-charge the DC-bus capacitor without any voltage and current overshoot within the specified time. In exisiting variable frequency drives seperte pre-charging circuits (or) thyristor bridges were used due to this drives power density, cost becomes high and control technique becomes complex. This paper presents about the design of three-phase three-switch buck-type rectifier for pre-charging application used in variable frequency drives which elimates the disadvantages of existing techniques. In this paper we will discuss about design procedure of pre-charging circuit of an 800KW converter with dc-link output voltage of 775V at an input ac voltage of 550V, 60Hz, selection of power and passive components, voltage and current stress of power transistors. In the final this paper discusses about loss distribution of the components and comparison of new converter technique with existing pre-charging techniques.

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1. INTRODUCTION

In all high power variable frequency drives (VFD's); dc-link capacitors were used to maintain a stiff DC-link voltage across the rectifier output, fed via an uncontrolled rectifier from three-phase ac voltage. The main usages of dc-link-capacitor were;

- Load-balancing energy storage element
- To compensate the difference between the power requirement of the inverter and the output power of input-uncontrolled bridge rectifier;
- To take in the demagnetization energy of the drive in case of an emergency shutdown of all converter transistors;
- To supply transient-power peaks;
- To protect the inverter from transient peaks of the mains voltage.

The size of this dc-link or filter capacitor depends on the amount of ac energy it must absorb to maintain a required amount of current ripple at the dc-line and the level of rms current it can tolerate because of ESR heating. When a capacitor bank is initially connected to a voltage source a transient charging (inrush) current will flow. Inrush current is a maximum, instantaneous input current drawn by dc-link capacitors when it's first turned on. The magnitude and frequency of this charging current depends upon the total capacitance and inductance of the circuit as well as magnitude of the applied voltage.

As an application case a pre-charging circuit for VFD application shall be dimensioned in such a way that it's input voltage $U_{l\text{-}l,rms}$=550V±10%, Output DC link voltage U_0= 775V and P_0=800KW.

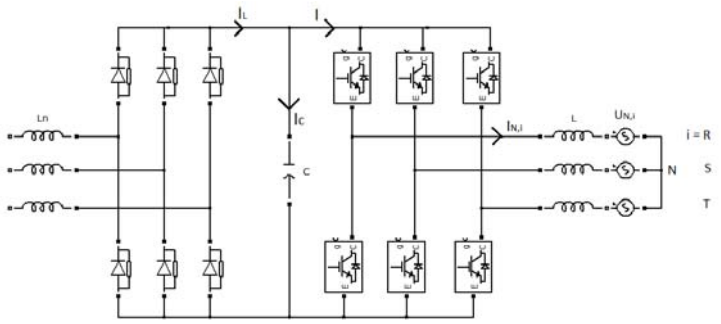

Figure 1. Basic power circuit of a Variable frequency drive

Basically there are different pre-charging topologies available to meet this specification such as; Resistor-contactor arrangement, Thyristor switch arrangement, Thyristor Bridge as rectifier, Magnetic resistive-element and proposed new topology Three-phase three-switch buck type rectifier [1]. The main advantage of the proposed new techniques is less number of active and passive components, less expensive, simple in control and controllability and able to detect all failure conditions.

In this paper we will discuss about the design of three-phase three-switch buck rectifier shown in Figure 2 used for pre-charging application.

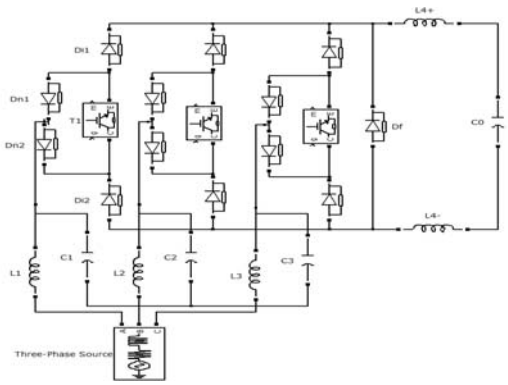

Figure 2. Three – phase Three-switch buck rectifier circuit for dc-link capacitor pre-charging

The main objectives of pre-charging circuit were;

- To charge the dc-link capacitor within the allowed time
- To limit both the peak dc link and ac input line current to any desired limit (pre-defined value).

Furthermore in this paper we will discuss about usage of rectifier for pre-charging application in Section II, selection of power semiconductor, passive components in Section III, loss distribution of the components during a pre-defined pre-charging circuit current limit in Section IV and finally the performance comparison of existing converters with the proposed converter.

2. RECTIFIER AS A PRE-CHARGING CIRCUIT

The basic operating priciple of three phase three switch buck rectifier for pre-charging application is similar to the standard three phase bridge rectifier. The main difference is based on control technique used for pre-charging the DC-link capacitor, no of power semiconductors used. The switching sequence (110-011-101) of the proposed converter were shown in Figure 3, where *i=R, S, T* indicates a combination of three

swiches S_i, When S_i=0 means the correcponding swicth in the bridge leg is turned off and S_i=1 indiates the switch is in turned on state. For example, by considering one swiching sequence (101) the current flows in the bridge leg S_R of the rectifier, dc link inductor, dc link capacitor and bridge leg S_T of the rectifier S_R - L_4 - C_0 -S_T. The rectifier input current can be calculated for each of the switching sequences as shown in below equations; generally the three-phase rectifier input current is defined as

$$i_{rec} = \frac{2}{3}\left(i_{rec,R} + e^{j2\pi/3}.i_{rec,S} + e^{j4\pi/3}.i_{rec,T}\right) \quad (1)$$

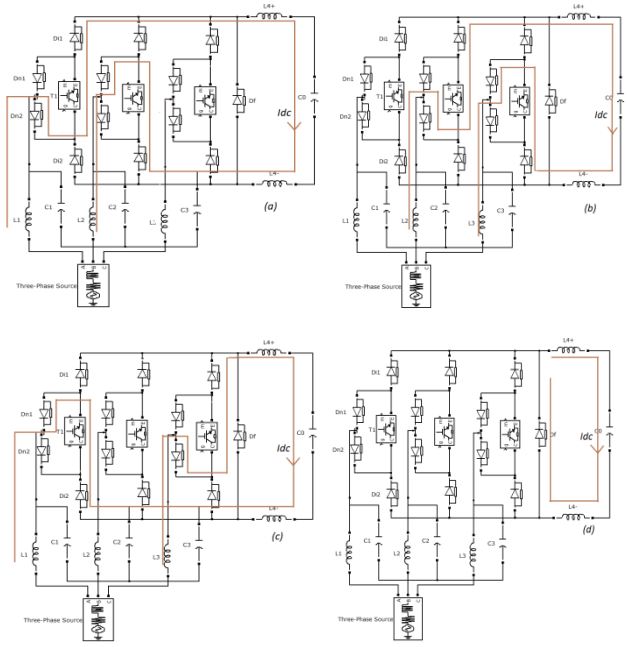

Figure 3. Conduction states of the Three-phase Three-switch buck PWM rectifier, (a) I_{dc} during switching sequnce (110), (b) I_{dc} during switcing sequence (011), (c) I_{dc} during switching sequence (101), (d) I_{dc} during freewheeling

For the switching state j=(101) the rectifier input currents are $i_{rec,R} = I$, $I_{rec,s} = 0$ and $i_{rec,T} = -I$, therefore the rectifier input current for the switching states will be;

$$i_{rec,(101)} = I.\frac{2}{\sqrt{3}}e^{j\pi/6} \quad (2)$$

$$i_{rec,(110)} = I.\frac{2}{\sqrt{3}}e^{-j\pi/6} \quad (3)$$

$$i_{rec,(011)} = I.\frac{2}{\sqrt{3}}e^{j4\pi/3} \quad (4)$$

2.1. Proposed Control Technique

The proposed control algorithm shown in Figure 4 consists of two blocks i). Zero crossing detection and ii). Peak current mode control. The zero crossing detection circuit is used for generating PWM pulses required for normal operation of the converter.

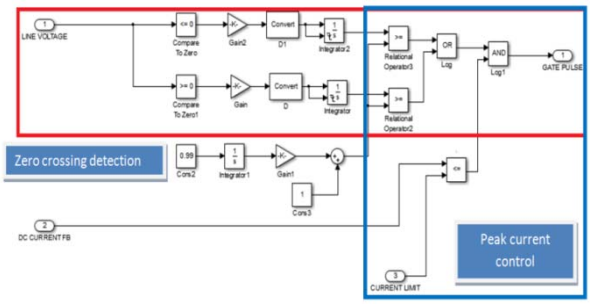

Figure 4. New proposed soft charging control technique with constant current control

The basic switching sequence of three phase three switch buck converter is similar to the standard three phase bridge rectifier. The required PWM gate pulses were generated through passing the input three phase ac voltage to a zero crossing detector (ZCD) circuit, falling edge integrator and logical gate circuits. Initially, three phase input ac voltages were applied through the ZCD circuits which generated a series of pulses based on the zero crossing of ac voltage.

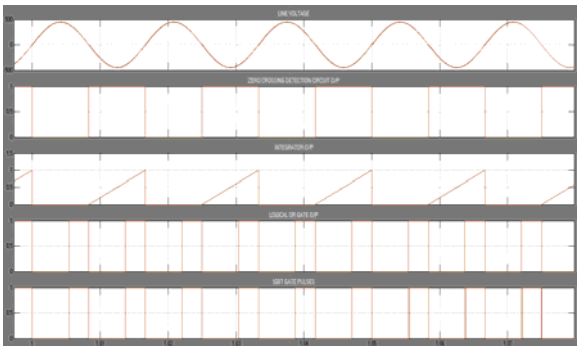

Figure 5. Waveforms at different stages of pre-charging control circuits, (a) Line voltage, (b) Zero crossing detection circuit o/p, (c) Logical OR gate o/p, (d) Logical o/p from current feedback, (e) IGBT gate pulses

The pulses from ZCD were further sampled through falling edge integrator through which synchronized ramp signals will be generated for both positive and negative ac voltages. Finally, the ramp signals were compared through comparator and logic gates through which pulses were generated for each cycle of ac input voltage. In peak current mode control the DC link inductor current was compared with the required pre-defined reference set current, when the DC link inductor current is less than the set current a pulse will be generated and vice versa. The resultant pulses from the zero crossing detection circuit and peak current control were logically compared through an AND gate and generates resultant PWM pulses for IGBT's as shown in Figure 5. Separate control circuits (zero crossing & peak current detection circuit) will be implements for individual phases through which the individual IGBT's will be controlled.

3. SYSTEM DESIGN

In this section we will discuss about selection of active and passive components which are mainly depends on the voltage and current stress of the components.

3.1 Voltage Stresses

The voltage stresses on the active and passive components mainly depends on the mains line to line voltage, however, for selecting IGBT's and power diodes and additional margin of double the line to line voltage has to be considered.

$$U_{l-l,\max} = \sqrt{2} * (550V + 10\%) = 855V \quad (5)$$

The output voltage is controlled to a constant value of U_0=775V, therefore the induction L_4 and capacitor C_0 were selected for this value plus 10% margin for overshoot margin of control loop.

3.2 Current Stresses

In order to select the active and passive components it is necessary to calculate the device average and rms currents. For exact calculation of average current it is necessary to know the currents during different intervals of the pre-charging phase [2] are shown in Figure 6. The inductor dc current during pre-charging phase have three intervals; 1.Inductor current before reaching the pre-set current limit, 2. Inductor current reaches the pre-set value, 3. Inductor current reaches after the pre-set value.

The average and rms current flows through the power semiconductor during this interval I for a pulse period are shown in Figure 7;

$$i_{T,avg} = \frac{1}{T_p} \int_0^{\delta_R T_p} I \, dt_\mu = I.\delta_R \tag{6}$$

$$i^2_{T,rms} = \frac{1}{T_p} \int_0^{\delta_R T_p} I^2 \, dt_\mu = I^2.\delta_R \tag{7}$$

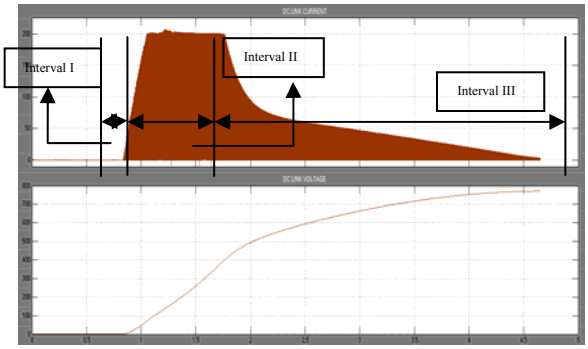

Figure 6. (a). DC link current limited to 200A, (b). DC link voltage of 770V across the capacitor

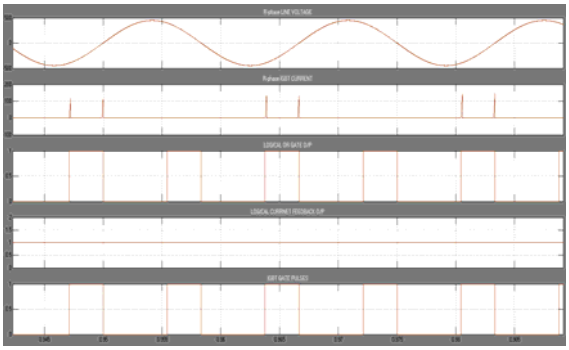

Figure 7. Waveform during pre-charging Interval I, (a) R-phase Line voltage $U_{R,N}$ = 550V, (b)R-phase IGBT current, (c)Zero crossing detection circuit logical OR gate o/p, (d) Peak current detection logical current feedback o/p, (e) IGBT gate pulses

During interval I the DC link inductor current is less than the pre-set current limit, so the DC link inductor current will be in discontinuous conduction mode. In interval II, once the DC link inductor current reaches the pre-set current value the pre-charging converter will operate in swich mode of operation as shown in Figure 8, 9. The DC link inductor current during the interval II is further divided into two sub intervals, the first sub interval is the current rise from zero to pre-set current limit and the second sub interval is the

switched operation of the pre-charging converter where the DC link inductor current is switching between zero and the pre-set current limit. The DC link inductor current during the first sub interval can be defined as;

$$i(d\,T_S) = i(0) + (d\,T_S) * \left(\frac{U_{l-l}(t)}{L} \right) \tag{8}$$

During the second sub interval, the DC link inductor current changes with the essentially constant values provide by eq. 8. Hence the value at the end of second interval is;

$$i(T_S) = i(dT_S) + (d'\,T_S) * \left(\frac{U_{L4}(t)}{L} \right) \tag{9}$$

Finally the DC link inductor current during interval II is the sum of sub intervals I & II;

$$i(T_S) = i(0) + \frac{T_S}{L} \left(d(t) \langle U_{l-l}(t) \rangle + d'(t) \langle U_{L4}(t) \rangle \right) \tag{10}$$

In practical the average DC link inductor current is equal to the pre-set current limit which will be used for selecting the active and passive components.

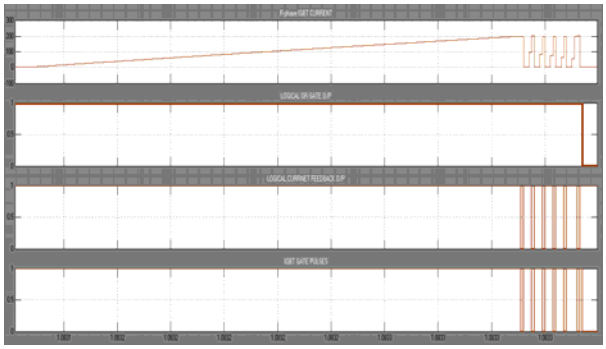

Figure 8. Waveform during pre-charging Interval II, (a) R-phase IGBT current, (b) Zero crossing detection circuit logical OR gate o/p, (c) Peak current detection logical current feedback o/p, (d) IGBT gate pulses

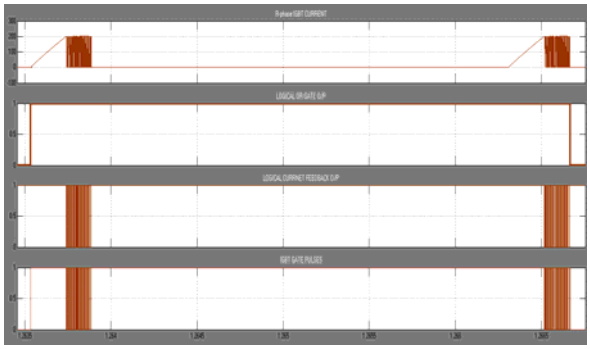

Figure 9. Waveform during pre-charging Interval II (Zoom-out version), (a) R-phase IGBT current, (b) Zero crossing detection circuit logical OR gate o/p, (c) Peak current detection logical current feedback o/p, (d) IGBT gate pulses

3.3 Selection of Capacitor C_0

The dc-link bus capacitor is used in converters and inverters to decouple the effect of inductance from the DC voltage source to the power bridge. The bus link capacitor provides a low impedance path for

the ripple current associated with inverter hard switching, plays a major role in reduction of leakage inductance of the inverter power bridge which in turn reduces the switching loses of the power devices. Having a low impedance DC bus is the basis for designing an efficient converter [3].

The DC link bus capacitor is selected on the basis of allowed ripple current, ripple voltage and the DC bus capacitor voltage;

$$C = \frac{U_0}{\left(32 * L * \Delta V_{0.5t} * f^2\right)} \tag{11}$$

Where $\Delta V_{0.5t}$ is the maximum peak-peak ripple voltage across the dc-bus link capacitor at 50% PWM duty cycle, V_{bus} is the bus voltage, L is the inductance and f is the PWM frequency.

3.4 Selection of Inductor L_4

A DC choke between the input rectifier and the DC link bus capacitor affects the DC bus voltage waveform and the AC input current waveform. It reduces the amount of AC ripple on the DC bus voltage and the AC input line harmonics. Additionally it offers protection against nuisance tripping due to voltage spikes, such as those caused by phase advancing capacitor switching. DC link chokes can be used individually, typically on the positive DC bus, or in pairs with one in the positive and one in the negative DC bus branch. When two DC reactors are used on the bus, the inductance is additive [4].

$$L = \Delta V\%_0 * \left(\frac{U_0}{\sqrt{3} * 2 * \pi * f * I_{con}}\right) \tag{12}$$

Where $\Delta V_{\%}$ is the percentage amount of ac-ripple voltage across the inductor, U_0 is the dc-bus link voltage, f is the switching frequency of the converter, and I_{con} is the dc inductor current.

For selection of components the worst case operating conditions has to be considered. For the current stresses of power semiconductor the worst case is given by the maximum pre-set current limit set during the pre-charging condition. According to equation.5, considering a margin for power semiconductor turn-off and for an overshoot of the rectifier input voltage, the IGBTs and diodes with double the line-to-line voltage blocking capability have been chosen. The selected power semiconductors and passive devices were listed in Table I.

Table 1. Active and Passive Components selection and specifications

Components	Specification
IGBT S_i	IGBT Module FD400R33KF2C, 3300V, 400A
Diodes D_N	Diode Module DD400S33KL2C, DD400S33K2C, 3300V, 400A
Diode D_F	Diode Module DD400S33K2C, 3300V, 400A
Output Inductor L_4	Magnetics, Ferrite-0T49928EC, 4x1.2mH, N=37 turns, 14AWG
Output Capacitor C_0	Epcos B25620B, 80x1000µF, 1320VDC

4. PERFORMANCE EVALUATION

The performance of three-phase three-switch buck rectifier which has designed in the previous section is evaluated based on the power losses, conduction and switching losses can be derived accurately based on the analytical derivations and calculations.

4.1 Conduction Losses

The conduction loss of IGBT and diode has been calculated based the forward characteristics of the semiconductor (forward voltage drop and forward resistance of the devices) [5]. The average conduction losses of the IGBTs and diodes are;

$$P_{cT} = U_{ceo} * I_{av} + r_{ce} * I_{rms}^2 \tag{13}$$

$$P_{cD} = U_{do} * I_{av} + r_d * I_{rms}^2 \tag{14}$$

Where U_{ceo}, U_{do} is the forward voltage drop of IGBT and diode, r_{ce}, r_d is the IGBT, diode forward resistance and I_{ac}, I_{rms} is the average, rms currents.

During different intervals of pre-charging condition, conduction losses will be high during interval II as rectifier will be operating in switched mode of operation. In interval I and III the conduction losses will be less, as the power semiconductors will ON for a short duration as the dc link inductor current is less than the pre-set current limit.

4.2 Switching Losses

The switching losses of power semiconductors are the product of switching energy and switching frequency of the rectifier [6].

$$P_{swT} = \left(E_{onT} + E_{offT}\right) * f_{sw} \tag{15}$$

$$P_{swD} = \left(E_{onD} + E_{offD}\right) * f_{sw} \tag{16}$$

Where $E_{on(T,D)}$, $E_{off(T,D)}$ is the IGBT and diode on and off state energy losses and f_{sw} is the switching frequency.

During interval II of pre-charging condition, the dc link inductor current reaches the pre-set current limit, due to this the rectifier is operating in switched mode of operation where switching losses will be more. In interval I & III the dc link inductor current is less than the pre-set current limit, due to this switching losses is less as the rectifier operates for a momentary time depends on the three phase line voltage and rectifier control sequence.

4.3 Passive Components Losses

In addition to the losses of active components, losses of passive components have to be considered. Generally the dc output inductor (L_4) and dc link capacitor (C_0) losses needs to be considered. The core and coper losses of the dc inductor were;

$$P_{fe,L4} = k * f_{sw}^{(m)} * B_{ac}^{(n)} * \left(W_{tfe}\right) * \left(10^{-3}\right) \tag{17}$$

$$P_{cu,L4} = I_{rms}^{2} * R_l \tag{18}$$

Where k, m, f were the empirical values available in core datasheet, B_{ac} is the flux density, W_{tfe} is the core weight and R_l is the resistance of the winding [7].
The losses of the output capacitor C_0 can be calculated via;

$$P_{co} = ESR_{co} * I_{co}^{2}{}_{rms} \tag{19}$$

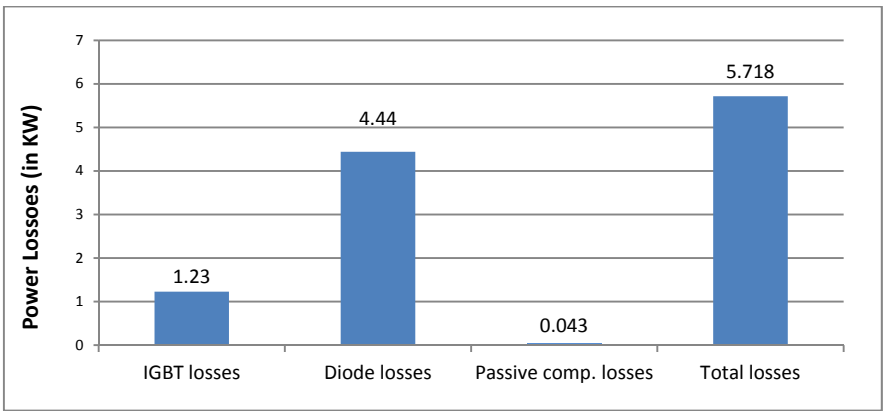

Figure 10. Breakdown of total losses at different components at $U_{R,N}$, $U_{S,N}$, $U_{T,N}$ = 550V and I_{dc}=200A

With the analytical equations mentioned from (13) – (19) provides the losses of active and passive components through which the total losses of the converter can be easily evaluated. The total losses and breakdown of the total losses are depicted in Figure 10 at a pre-set current limit of I_{dc}=200A. Additionally the losses distribution of passive and active components at different pre-set current limit can be evaluated based on the above equations.

5. DISCUSSION

In the previous sections the converter working principle, selection of active and passive components and their loss distribution at a pre-defined charging current of the three-phase buck-type rectifier has been analyzed. In this section we will compare advantages, performance of proposed converter with existing pre-charging techniques like Resistor-contactor arrangement, Thyristor switch and Thyristor bridge rectifier arrangement. While comparing the proposed and existing topologies, the proposed topology has advantage like easy in controllability as the proposed topology uses IGBT's, since IGBT's is a voltage controlled device the gate charge, gate current requirements were less and gate circuit is very simple not like thyristor based techniques which required complex gate circuits. The proposed topology requires only three controlled switches so the control circuit requirement is also less, whereas the thyristor bridge rectifier requires six numbers of thyristor which requires control circuits double the times of proposed topology. In general when comparing existing and proposed topologies with respect to cost, volume, power dissipation and robustness the proposed converter is better than the existing topologies. The proposed topology is cost effective as it requires only three IGBT's and less control circuits while other topologies like thyristor bridge requires six thyristors and double the control circuits, thyristor switch and resistor contactor arrangement requires bulky resistor banks to limit the pre-charging current during DC link capacitor pre-charging time. The power dissipation of three-phase three-switch buck rectifier and thyristor bridge rectifier is almost same, as the proposed topology uses one IGBT and four power diodes for each leg due to than the power dissipation almost similar but it's less compared with other topologies which uses resistor banks for pre-charging application. The proposed topology and thyristor bridge rectifier is less robust compared with resistor bank topologies as these uses controlled switches where resistor contactor arrangement uses electro-mechanical devices. In industrial high power drives approximately six to seven terminals were available for customer access in order to connect input AC supply, DC capacitor banks and output terminals for connecting the drives, these terminals were live terminals so before the pre-charging operation begins diagnosis is mandatory to detect the faults like DC bus short, Inverter output fault, Phase voltage imbalance, Partial dc link discharge. The proposed topology and Thyristor Bridge as rectifier can detect these faults as in both the topologies the DC link current were monitored, but in thyristor bridge arrangement and other existing topologies it's not possible to switch off the controlled switched immediately as it's using thyristor, but in proposed topology it possible since it uses IGBT's by switching off the gate pulses it is possible to switch off the IGBT's thereby the DC bus pre-charging is stopped immediately.

The proposed soft charging control algorithm uses simple logic gate functionalities unlike the existing control technique uses nonlinear discontinuous current control in thyristor bridge topologies etc, for detecting zero crossing detection of input ac line voltage and detection of dc link inductor peak current. The proposed algorithm can be easily implemented through low cost microcontroller (or) FPGA device as the detection technique is through logic gates.

6. CONCLUSION

In this paper a detailed overview of three-phase three-switch buck converter, its design procedure and performance was analyzed at a pre-set charging current and given drive rating, followed by comparison of proposed topology with existing topologies were done. The Resistor contactor, Thyristor switch and Magneto resistance element type soft charging circuits were older techniques even though they are robust, it's not possible to control the dc link inductor peak current and dc-bus capacitor voltage precisely without overshoot. During different fault conditions like; brownout condition, fault to ground, bus fault and partially charged capacitors it's difficult to detect the fault conditions as there is no possibility of controlling the input DC inductor current and capacitor charging current. The proposed three-phase three-switch buck converter type soft charging technique eliminates the above mentioned demerits and possible to control the dc bus capacitor voltage step by step and limit the DC link inductor current within a peak limit with small DC link inductor. Addition to the above mentioned merits the main advantage of proposed topology and control technique for pre-charging application is because of its simple in operation, less power density compared with existing pre-charging concepts and possibility of using same converter for both operations, i.e) for pre-

charging application and driving the VFD. From the above mentioned analysis, the three-phase three-switch buck type rectifier is suitable for high power drives pre-charging application since it's possible to pre-set the converter charging current to any pre-defined values. Further research is ongoing, on using three-phase three-switch converter for both pre-charging application and driving the VFD. When we use three-phase three-switch converter for both application, two separate control mechanism were required i) to control the peak charging current during pre-charging and ii) to control and maintain the constant dc bus voltage across the dc bus link capacitor during driving operation of the VFD.

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