

Review of Static Compensation of Autonomous Systems

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ABSTRACT

Deregulation of the electric power energy market has thrown open opportunities for tapping the large number of small pockets of renewable energy sources with the asynchronous generators. Whether the power is supplied by asynchronous generator or by the grid at the remote location, its quality has become an important aspect for consumers of electricity. Efforts have been made to improve the power quality using passive filters, active filters and the new concept of Custom Power. Use of Custom power devices ensures that a load do not pollute the power supply of the other loads. One such custom power device is the DSTATCOM (Distribution Static Compensator) which is connected in shunt at the load end. The heart of the DSTATCOM is an inverter. The focus on the autonomous generation has increased in the recent years. The paper presents a comprehensive review of the DSTATCOM used for autonomous generation. It is aimed at providing a broad perspective on the status of DSTATCOM, used with Asynchronous generators, vis-à-vis its working principle, topology, supply system configurations, solid state switching devices and technology, control methodologies and approaches, application areas of DSTATCOM to researchers and application engineers dealing with power quality aspects of Autonomous Systems. Classified manner in which the references are presented in this paper will serve them as quick and useful reference.

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1. INTRODUCTION

The last few decades has seen ever increasing demand for energy. This has caused fast depletion of the conventional energy sources i.e. the fossil fuel. This induced man to harness the renewable energy available from nonconventional energy sources such as small hydro, wind and bio-mass. Most of these resources are available at remote locations and with small capacity. This required that the generator be rugged, requiring less maintenance, low cost and small and efficient machine. One generator which met all of the requirements is the induction generator [1]. Further deregulation of power system has allowed autonomous generation of electrical energy [2]-[3]. Thus autonomous asynchronous generator (AAG) with its excitation requirement being met by a capacitor bank connected across its terminals [4]-[9], has become a compatible option. However the poor voltage and frequency regulation is a major bottleneck in its commercialization. This has led to a number of attempts to investigate the voltage and frequency controllers for constant [10]-[16], as well as variable power applications [17]-[19]. The reported controllers support either three phase 3-wire or three phase 4-wire systems. The later catering for single phase loads also.

2. STATE OF ART

The concept of compensation of the distribution system was arrived at, from the desire of the consumers of electricity to get quality power. This has been extended to autonomous power systems where the distribution system is directly connected to AAG instead of being connected to the utility supply system. The state of art, load equipments are more sensitive to power quality variations than their earlier versions. The increased competitiveness has led to desire for higher efficiency, which in turn brought in the power electronics controllers for the drives [20]. This has resulted in increased harmonic level on the power system. The present scenario has made the end users become more conscious of the power quality issues [21]-[30]. Early power quality addressing was done with passive filters connected to PCC to filter out the harmonics generated by a load. LR filters acted as series filter and RC filters were used as shunt filters [31]-[33]. Problems of fixed compensation, resonance with supply system and limited flexibility forced them to be replaced by active filters [34]-[37]. To compensate the harmonic distortions in voltage and current the active filters are used in various configurations like series, shunt and a combination of both. These active filters suffered from a serious drawback, in that its rating has to be of nearly full capacity of the load. A mid path solution was then chosen in the form of hybrid filters [38]-[40]. This reduced the cost and improved reliability.

Parallel to the above another group of engineers had been working on FACTS and STATCOM for reactive power compensation of transmission lines. Drawing from the experience of these people the concept of custom power was proposed by N. G. Hingorani [41]. Custom power device is a power electronics controller used for power quality improvement on distribution systems [42]-[47]. Its performance for power quality improvement is widely reported for both Autonomous and Grid connected distribution systems.

The compensating devices, either compensates a load, (i.e. corrects its pf), or improves the supplied voltage. These devices are either connected in shunt or in series or a combination of both. They are :

- (1) Distribution STATCOM or DSTATCOM
- (2) Dynamic Voltage Restorer (DVR)
- (3) Unified Power Quality Conditioner (UPQC)

The DSTATCOM is connected parallel to the load and in shunt to the power system [48]. The DVRs are connected in series with the power supply lines. They add a voltage to the supply voltage which is opposite to the line voltage drop. There by decreasing the effective length of the line [49][51]. The UPQC is a combination of both series and shunt compensators.

In case of autonomous power systems the no load requirement of AAG of the reactive power is met by the capacitor bank. However the additional reactive power requirement of the AAG on load and that of the load itself is supplied by the DSTATCOM to regulate the terminal voltage of the AAG. This is in contrast with the DSTATCOM used with distribution systems connected to utility supply mains. A typical autonomous power system with an AAG, an R-L load and a DSTATCOM is shown in Fig. 1.

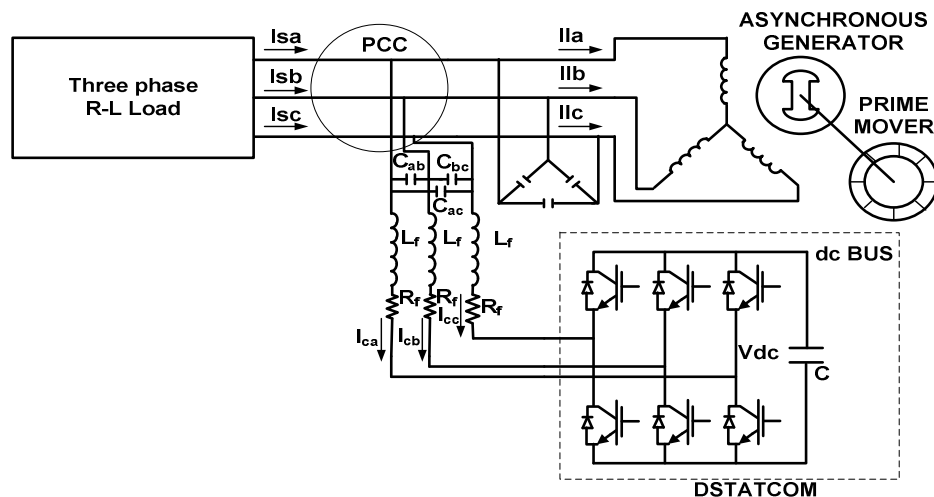


Figure 1. A typical autonomous power system.

With the deregulation of the power systems, the concept of distributed generation (DG) and microgrid (MG) are gaining popularity. The DGs and the MGs are interfaced to the distribution system through the power electronics VSIs. This solves many of the problems of distribution systems. It also

replaces by its functions many of the existing compensation devices, which in turn reduces the cost. Further the utility is not constrained to increase its installed capacity [1], [52].

A comprehensive review of the DSTATCOM technology and its development as applied to Autonomous Generation are carried out in this chapter. The present section has six subsections viz. (i) working principle (ii) DSTATCOM topology (iii) supply system configurations (iv) solid state switching devices and technology (v) control methodologies and approaches (vi) application areas of DSTATCOM.

3. WORKING PRINCIPLE

The improvement of power quality is usually achieved with a converter having a bridge structure. Converters having DC voltage as source called voltage source inverter (VSI) are generally chosen for this purpose [53]. The use of current source inverter, however, is less reported [54]. The working principle of the DSTATCOM is similar to generic predecessor namely the STATCOM. In its use as compensator of the Autonomous Generation it acts in voltage regulation mode and force the voltage at the point of common coupling (PCC) a balanced sinusoid. It generates reactive power and provides for the increased VAR requirement of AAG on load together with the VAR requirement of the load itself. In current control mode it can compensate the distortion caused by the load and prevent it from getting into the supply side of PCC [55]. Also the DSTATCOM with a battery source connected on the DC side can perform load balancing and load leveling [56]-[58].

4. DSTATCOM TOPOLOGY

Many VSI based topologies and configurations are reported in the state-of-art DSTATCOM controller for Autonomous Systems. Multi-pulse and multi-level topologies are reported in the design of the compensators [22] [59]. A basic six-pulse VSI having three legs with two valves per leg and an electrostatic capacitor on the DC bus is illustrated in Fig. 2. A self-commutating switch with a reverse diode connected in parallel make up each valve of the bridge. Using the fundamental frequency switching modulation, the square wave mode produces eight possible switching states with respect to the polarity of the DC voltage (V_{dc}). The AC terminal then produces three quasi-square waveforms, displaced successively by 120° . The Fig. 3 shows the output voltage wave shapes obtained, which have voltage levels $0, \pm V_{dc}/3$ and $\pm 2V_{dc}/3$ for phase to neutral voltage and $0, \pm V_{dc}$ for line to line voltages. This produces unacceptable level of current harmonics which interfere with the other loads connected to the system. To reduce the THD to a value below the IEEE

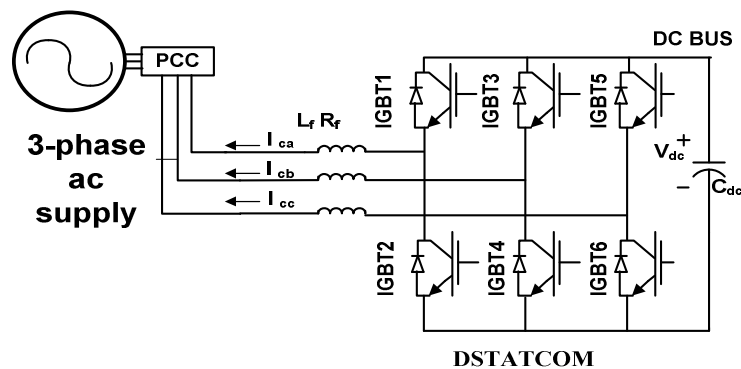


Figure 2. A basic six pulse Voltage Source Inverter.

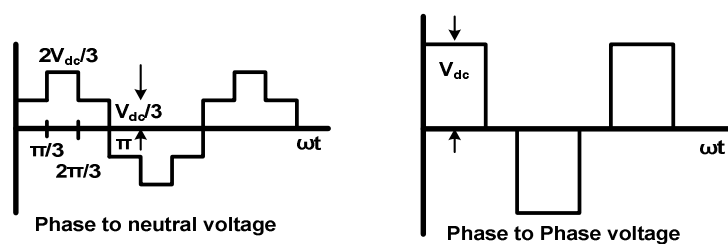


Figure 3. Wave shapes of inverter output for fundamental square wave type of switching.

519 stipulation, multiple pulse converter topologies are used which are achieved by combining a number (say N) of six-pulse converter units and triggering them at specific displacement angles. The output AC waveform from each unit is then electro-magnetically added with an appropriate phase shift by inter-phase transformers to produce a multi-pulse ($6 * N$ pulses) waveform, which brings the output AC waveform more close to the sinusoidal wave and a decrease in THD [60].

However the increase in pulse order is associated with an increase in the number of electronics devices, magnetic and associated components. This increases the cost of the converter as well as increases the switching losses. Further as multi-pulse converters involve complex series-parallel connection of transformer windings/circuits multi-level configuration has been receiving increasing attention [61]–[66]. In multilevel topology, a synthesized staircase voltage waveform is derived from several levels of DC voltage sources obtained normally by using capacitor voltage sources. Fig. 4 shows the operation of multi level diode clamped converter. A typical SVM technique is used for controlling the half bridge. Fig. 4(a) shows the configuration of a three level half bridge. Fig. 4 (b) indicates voltage wave shape and the three voltage levels.

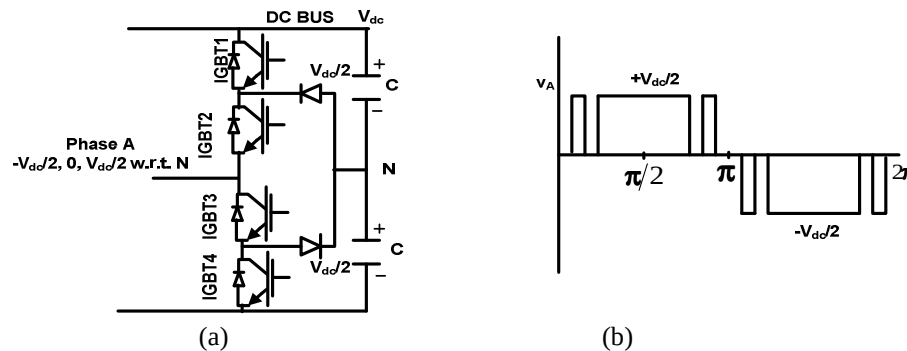


Figure 4. (a) Basic three level NPC VSI bridge converter (b) PWM wave Shape

Fig. 5 shows the operation of multi level based on flying capacitor technique [64]. Fig. 5 (a) shows the configuration of a phase half bridge of a three-cell flying capacitor multilevel inverter (FMCI). Fig. 5 (b) indicates voltage wave shape obtained from five level sine-triangular modulations.

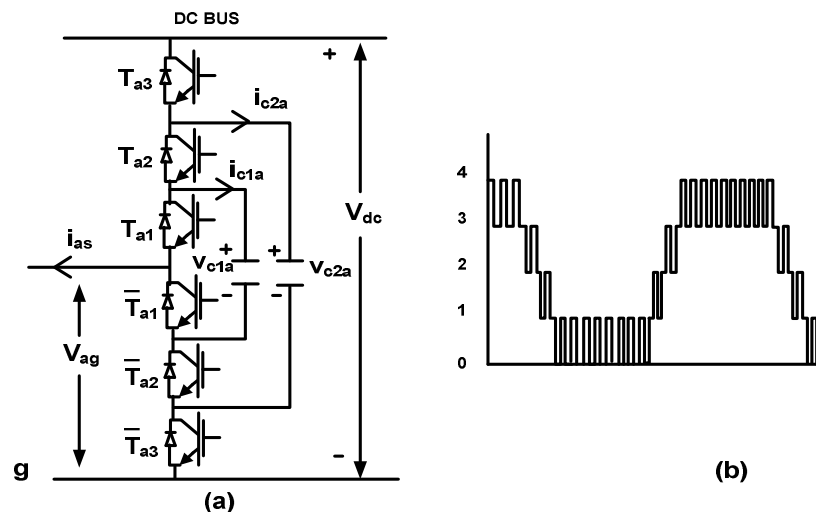


Figure 5 (a) Three-cell FCMI inverter topology (a phase) (b) Voltage waveform of a five-level sine-triangular modulation.

Cascaded H bridge inverter is another type of multilevel inverter which can be used with advantage [62]. The main advantages of multi-level converter vis-à-vis square-wave pulse converter are lower harmonic content, decreased device voltage stress and potentially higher converter voltage and thus higher power rating. As the compensation of autonomous system is mainly a low voltage high power operation, an IGBT bridge with PWM control provides an optimal solution.

5. SUPPLY SYSTEM CONFIGURATIONS

The configuration of the distribution supply system of an Autonomous Power System is guided by the type of load. Most loads on the distribution system are single phase two wire loads. Others with higher power ratings are usually three phase loads which can be a three wire type or a four wire type, having a neutral connection along with the three phases. Many three phase nonlinear loads like Adjustable Speed Drives (ASDs) do not require a neutral connection and are fed through a three phase three wire system. While most domestic loads like computers, and lighting loads are connected between one of the phases and the neutral.

5.1. DSTATCOM for two wire autonomous system:

A single phase DSTATCOM connected to two wire single phase Autonomous system is shown in the Fig. 6. The loads of such a system is compensated by a single phase DSTATCOM, which is usually a two leg bridge operating as a voltage source converter with a capacitor on the dc-bus acting as energy storage element [66]-[68].

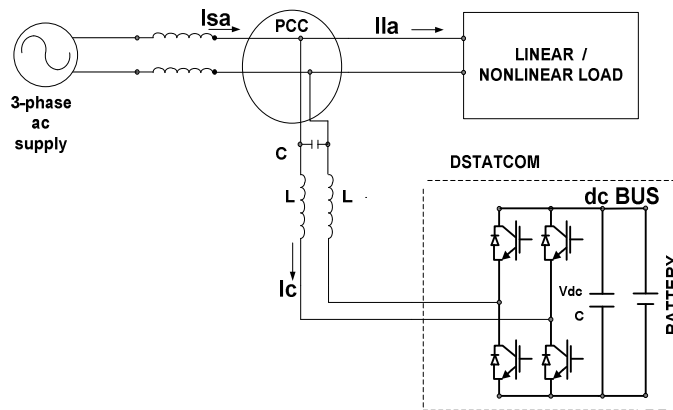


Figure 6. Single Phase DSTATCOM connected single phase Autonomous system

5.2. DSTATCOM for three wire autonomous system:

A DSTATCOM connected to three phase three wire Autonomous system is shown in Fig. 7. Adjustable Speed Drives (ASDs) are the major applications of three-phase three-wire converters [69]. For low voltage applications, the DSTATCOM is usually a single stage three legged voltage source converter with a capacitor on the dc-bus acting as energy storage element [56]-[58]. In the case of higher autonomous distribution voltage and higher power handling capacity multi pulse VSI, multi level VSI, cascaded multi-level VSI are used [60]-[66].

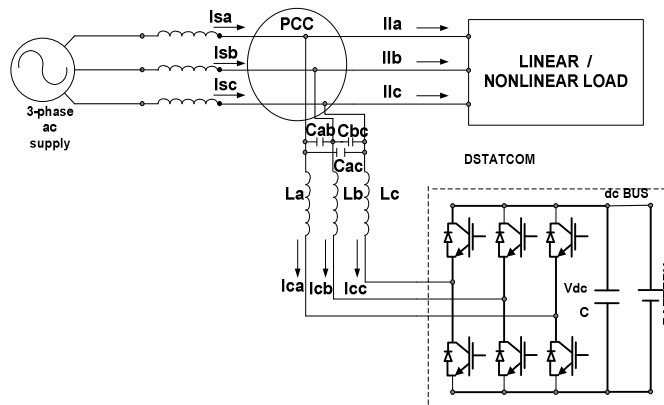


Figure 7. Three Phase Three Wire DSTATCOM connected to three phase three wire Autonomous system

5.3. DSTATCOM for four wire autonomous system

A typical three phase four wire DSTATCOM for an autonomous system is shown in Fig. 8. On the load side a large number of single-phase loads exits. These loads are provided for using delta-star transformers with the single-phase load connected between one of the phases and the neutral [70]. They

cause excessive neutral current, harmonics injection, reactive power burden and current unbalance. For compensation of these problems, three-phase four-wire compensating devices are used [71]-[75]. For developing such DSTATCOMS different configurations of VSI having capacitor mid-point [64]-[66], three single-phase H bridge VSI [55] [62], and four-pole VSI have been reported [71] [73] [75]. In the case of capacitor mid-point VSI configuration, Fig. 8, the entire neutral current of the unbalanced load flows through the dc bus capacitor. Hence such a configuration is suitable for small to medium rating systems. In the case of a four pole VSI configuration, Fig. 9, the fourth pole is used to generate current which is equal and opposite to the neutral current. Thus a higher rating is possible in this case. Three single phase H-bridge scheme provides an advantage of matching the voltages for the solid state devices which leads to better reliability.

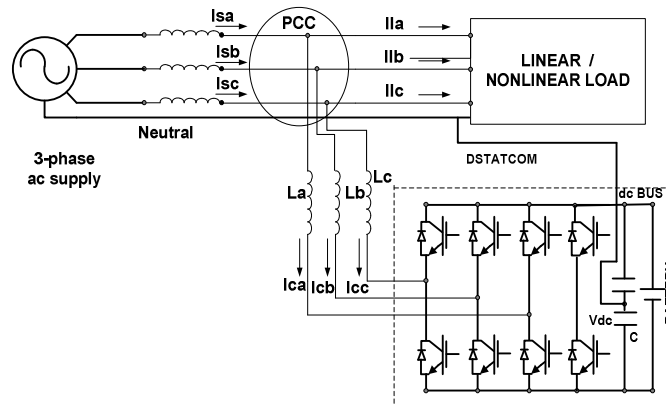


Figure 8. Three phase four wire autonomous system connected to DSTATCOM with neutral connected to capacitor mid-point of VSI.

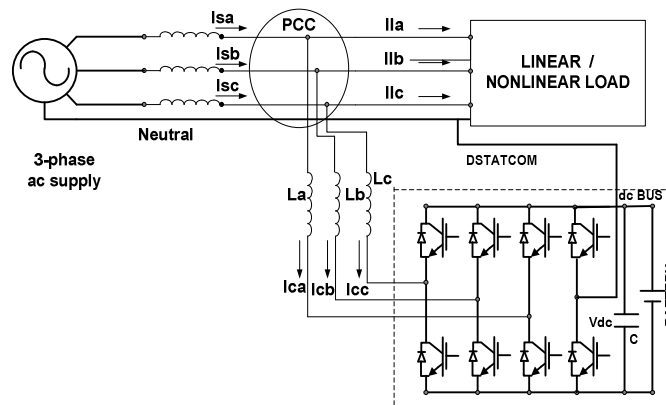


Figure 9. Three phase four wire autonomous system connected to DSTATCOM with four pole VSI.

6. DEVICES USED FOR CONVERTERS

In power electronics circuits, various types of controllable solid state switches like the conventional thyristor, GTO, IGBT, IEGT, IGCT or GCT, BJT and MOSFET [76]-[82] are used for voltage source converter, current source converter etc. Operating characteristics like the switching frequency/speed, switching losses, device rating, turn-on and turn-off characteristic, forward and reverse breakdown voltages, on-state voltage drop etc. varies from device to device. The conventional thyristor is a mature technology for SVC a second generation FACTS controller. It is commercially available in very high power rating, but it has a few drawbacks like no turn-off capability, high response time etc. So in earlier days BJT and MOSFETS were used in small ratings. The recent technology is of solid-state controllable turn off switches with better response time like GTO, IGBT, IGCT, etc [80]. For any particular compensation situation a trade off is made between such parameters like drive circuit requirement, switching frequency/speed, switching losses, cost of

device, etc. GTO is a mature technology for high power applications like the STATCOM for transmission lines. IGBTs are used for medium to small power applications and are used for in DSTATCOM catering for the compensation of the Autonomous systems. Due to their high switching frequency and speed they are used in PWM based controller.

The value of R_f and L_f connected in series with the VSI (Fig. 1) plays an important role in the implementation of the DSTATCOM. A large value of R_f increases the losses in the DSTATCOM. A small value of L_f switching ripples are injected into the PCC, and a large value of L_f affects proper tracking of the compensating current close to the desired value. A trade off is made in the values of L_f and R_f to obtain the optimum performance of the DSTATCOM. The VSI DC bus capacitor is another important parameter that affects the performance of the DSTATCOM. A convenient small capacitor causes ripples in the steady state and wide fluctuations in dc-bus voltage under transient conditions. A large capacitor on the other hand reduces ripples and fluctuations in the DC bus voltage, but adds to the cost and size of the DSTATCOM.

7. CONTROL METHODOLOGIES AND APPROACHES

The heart of the DSTATCOM used for compensation of an Autonomous Power system is its control system and its response to the dynamic change of the load depends on the methodology used for its control. Based on the desired performance to be achieved which are dependent on the operational requirements, type of application, system configuration and loss optimization, essential control parameters to be controlled, many control strategies of DSTATCOM power circuit are reported and are presented in [9-11] [15-19] [53-75]. The control of the DSTATCOM power circuit in general is achieved in four stages. The first stage involves sensing the essential AC and DC voltages and currents using PTs, CTs, Hall-effect sensors, etc to gather information about the dynamic condition of the load and the system. Based on this information some signals are synthesized using techniques like d-q synchronous rotating axis transformation [83-84], alpha-beta stationery reference frame transformations [85-86] and so on in the second stage. A reference signal is generated from this signal. Further the converter AC output voltage needs to be synchronized with the Autonomous system voltage. A phase locked loop is generally used to gather phase and frequency information of the fundamental positive sequence component of the system voltage. Then using the control methodology, the compensating commands in terms of current or voltage levels are generated in the third stage. The control methodology used in this stage can be categorized into linear [83-86], nonlinear [64] and special control techniques [87]-[89]. Then depending on the device configurations of the VSI, the gating signal for the solid state devices of the VSI are produced in the fourth stage.

The development of the compensating signals play an important part in deciding the rating and transient as well as steady-state performance of the DSTATCOM. The control methodologies used for generation of the compensating commands generally involve frequency domain and time domain control techniques. DSTATCOM using the time-domain methodologies sense the time-domain signals of instantaneous voltage and/or current vectors and synthesizes the d-q signals using the popular d-q synchronous rotating axis transformation [83] - [90]. Control techniques like PI or PID are then used to process the transformed signals to derive the compensating signals. In addition to this symmetrical component transformation and unit vector control are some of the other popular control schemes to extract the reference signals in time domain. In the PWM mode of control two popular control techniques, voltage control (VC) and current control (CC) are adopted [55]. The CC technique is widely reported in literature for linear and non linear control strategies. Under the linear control methodologies are reported control schemes using stationary PI controller, synchronous vector PI control, state feedback control, predictive control and deadbeat controls. The nonlinear control schemes encompass hysteresis control, delta modulation (DM) or pulse DM current control and online optimized controller.

Under the frequency domain control strategies based on Fourier analysis [91]-[93], Wavelet transform, Goertzel algorithm and Hilbert Transform [94]-[97] are reported. The on line application of the Fourier transform and wavelet transform involve complex and cumbersome computation and results in large response time, which make compensation of dynamically varying load difficult. Apart from this some control schemes are also reported which do not require generation of reference signals [98] [99]. To enhance controllability and operational performance of DSTATCOMs under various system conditions control strategies using of fuzzy logics, neural network, neuro-fuzzy artificial intelligence/ rule based techniques are also reported [100]-[104].

Two widely reported modes used for controlling the IGBT switches of the VSI are

- Carrier Based PWM control.
- Carrier less Hysteresis control.

7.1. Carrier based PWM control

In this control scheme, shown in Fig. 10, a high frequency carrier based sinusoidal PWM is used for generating the switching pulses for the IGBTs of the VSI. This algorithm is based on the instantaneous reactive power theory. The instantaneous voltage and current of the supply system and the load are measured. The three- phase system is transformed to a synchronously rotating reference frame using Park's transformation.

The instantaneous i_d reference current is generated by PI regulation of the dc terminal voltage with respect to a reference dc voltage. Similarly i_q reference current is generated by PI regulation of the ac terminal voltage of the VSI with respect to a reference ac terminal voltage. In case only power factor correction is desired, the reference i_q is set to zero. The decoupled i_d and i_q components obtained from abc to dq transformation of the measured instantaneous three phase current, are then regulated with two separate PI regulators with respect to the reference i_d and i_q currents obtained earlier. In order to synchronize the abc to dq0 transformation a Phase Locked Loop (PLL) is used. Fig. 9 shows the schematic diagram for the carrier based control of DSTATCOM using decoupled i_d and i_q control mechanism.

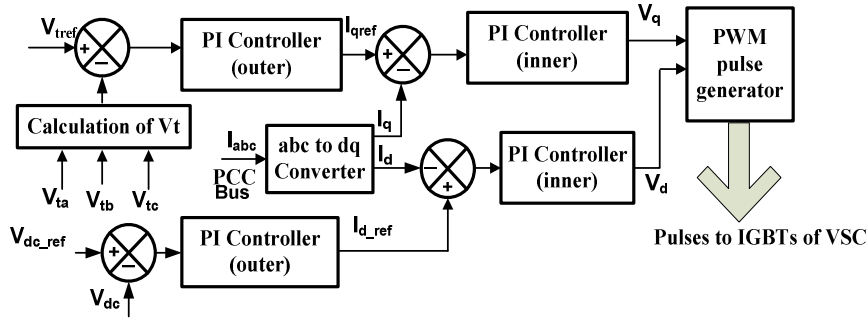


Figure 10. Schematic diagram for Carrier based PWM control

7.2. Modelling of carrier based control of DSTATCOM

The control of VSI of the DSTATCOM, shown in Fig. 9, is modeled in discrete mode using ode23tb on MATLAB platform. The discrete-time integrator block is used to implement the PI controller. Forward Euler method is used for integration. The discrete-time integrator block approximates $1/s$ by $T/(Z-1)$, which results in the following expression for the output at the n^{th} step .

$$Y(n) = Y(n-1) + KT * U(n-1) \quad (1)$$

$Y(n)$ is the output and $U(n)$ is the input to the controller

7.2.1 AC terminal voltage control

The three phase supply voltage (v_{sa} , v_{sb} and v_{sc}) are considered sinusoidal and hence their amplitude is computed as:

$$V_t = \sqrt{\{(2/3) (v_{sa}^2 + v_{sb}^2 + v_{sc}^2)\}} \quad (2)$$

The V_t computed above is compared with the desired terminal voltage V_{tref} . The ac voltage error $V_{er(n)}$ at the n^{th} sampling instant is

$$V_{er(n)} = (V_{tref} - V_{t(n)}) \quad (3)$$

Where $V_{t(n)}$ is the amplitude of the sensed three phase ac voltage at the PCC terminal at the n^{th} instant. The error $V_{er(n)}$ is fed to an outer PI controller, using discrete time integration, to generate the I_{qref} .

$$I_{qref(n)} = I_{qref(n-1)} + K_{ap} \{V_{er(n)} - V_{er(n-1)}\} + K_{ai} V_{er(n)} \quad (4)$$

Where K_{ap} and K_{ai} are the proportional and integral gain constants of the outer PI controller of the ac terminal voltage at the PCC

The actual I_q is generated by an 'abc to dq' convertor using parks transformation over the load current. The I_{qref} and I_q are compared and the error is fed to an inner PI current controller to generate V_q .

$$I_{qer(n)} = (I_{qref(n)} - I_{q(n)}) \quad (5)$$

$$V_{q(n)} = V_{q(n-1)} + K_{bp} \{I_{qer(n)} - I_{qer(n-1)}\} + K_{bi} I_{qer(n)} \quad (6)$$

Where K_{bp} and K_{bi} are the proportional and integral gain constants of the inner PI controller of the ac terminal voltage at the PCC

7.2.2 Control of the voltage at the dc terminal of the DSTATCOM

The V_{dc} of the dc bus is compared with the desired dc bus voltage V_{dc_ref} . The dc voltage error $V_{der(n)}$ at the n^{th} sampling instant is

$$V_{der(n)} = (V_{dc_ref} - V_{dc(n)}) \quad (7)$$

Where $V_{dc(n)}$ is the sensed dc voltage at the dc bus of the DSTATCOM at the n th instant.

The error is then fed to an outer PI controller to generate the I_{dref} .

$$I_{dref(n)} = I_{dref(n-1)} + K_{ap} \{V_{dcr(n)} - V_{dcr(n-1)}\} + K_{ai} V_{dcr(n)} \quad (8)$$

Where K_{ap} and K_{ai} are the proportional and integral gain constants of the outer PI controller of the dc bus voltage.

The actual I_d is generated by an 'abc to dq' convertor using parks transformation over the load current. The I_{dref} and I_d are compared and the error is fed to an inner PI current controller to generate V_d

$$I_{der(n)} = (I_{dref(n)} - I_{d(n)}) \quad (9)$$

$$V_{d(n)} = V_{d(n-1)} + K_{bp} \{I_{der(n)} - I_{der(n-1)}\} + K_{bi} I_{der(n)} \quad (10)$$

Where K_{bp} and K_{bi} are the proportional and integral gain constants of the inner PI controller of the dc bus voltage.

7.2.3 PWM controller

The V_d and V_q signals generated above are converted into modulation index 'm' and phase ' Φ ' which are then used by the PWM modulator for producing the required pulses for firing the IGBTs of the VSI. This causes the VSI to maintain the terminal voltage of the generator by generating / absorbing the required reactive current and supplying / absorbing active power from the generator to maintain the dc side voltage of the inverter.

7.3. Carrierless hysteresis control

Fig. 11 shows the control scheme for PI based carrier less hysteresis controller. The unit vectors for the in phase and the quadrature voltages are obtained from the supply voltage. The in-phase unit vectors (u_a , u_b and u_c) are computed by dividing the ac voltages v_a , v_b and v_c by their amplitude V_t . Another set of vectors called the quadrature unit vectors (w_a , w_b and w_c) is a sinusoidal function obtained from in-phase vector set (u_a , u_b and u_c). To regulate the PCC terminal voltage, its amplitude (V_t) is compared desired voltage (V_{tref}), and the error is processed by a PI controller. The output of the PI controller (I_{smq}^*) decides the amplitude of the reactive current to be generated by the DSTATCOM. Multiplication of the quadrature unit vectors (w_a , w_b and w_c) with I_{smq}^* yields the quadrature component of the reference (i_{saq}^* , i_{sbq}^* and i_{scq}^*).

To provide self supporting dc bus for the DSTATCOM, the charging current must be provided from PCC. In order to achieve this the dc bus voltage (V_{dc}) is sensed and compared with dc reference voltage (V_{dcref}). The error voltage is processed by a second PI controller. The output of the PI controller (I_{smd}^*) decides the amplitude of the active power component of the source current. Multiplication of the in-phase vectors (u_a , u_b and u_c) with I_{smd}^* yields the in-phase component of the reference source currents (i_{sad}^* , i_{abd}^* and i_{scd}^*). The reference source currents (i_{sa} , i_{sb} and i_{sc}) are obtained by adding the corresponding in-phase and the quadrature components. A pulse width modulation (PWM) current controller then compares the reference source currents (i_{sa}^* , i_{sb}^* and i_{sc}^*) with sensed source currents (i_{sa} , i_{sb} and i_{sc}) to generate the switching signals for the IGBTs of the DSTATCOM.

The hysteresis controller adds a hysteresis band $\pm h$ around the calculated reference current. When $i_{sa} - i_{sa}^* > +h$ pulses are generated for the lower level switches and when $i_{sa} - i_{sa}^* < -h$ pulses are generated for the upper level switches of the VSC.

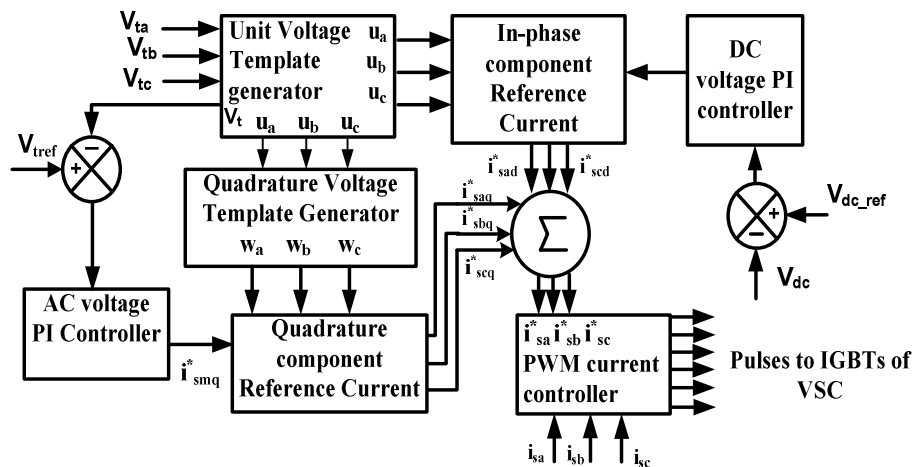


Fig. 11. Schematic diagram for Carrier-less hysteresis control of DSTATCOM.

7.4. Control algorithm of carrierless hysteresis control

The Three phase voltages at the PCC (v_a , v_b and v_c) are sinusoidal and hence their magnitude is computed as

$$V_t = \sqrt{\{(2/3) (v_a^2 + v_b^2 + v_c^2)\}} \quad (11)$$

The unit vectors u_a , u_b and u_c are derived as

$$u_a = v_a/V_t; \quad u_b = v_b/V_t; \quad u_c = v_c/V_t; \quad (12)$$

The unit vectors in quadrature, w_a , w_b and w_c , to the in-phase unit vectors, u_a , u_b and u_c , is derived using the following transformation

$$w_a = -u_b/\sqrt{3} + u_c/\sqrt{3}; \quad (13)$$

$$w_b = \sqrt{3}u_a/2 + (u_b - u_c)/2\sqrt{3} \quad (14)$$

$$w_c = -\sqrt{3}u_a/2 + (u_b + u_c)/2\sqrt{3} \quad (15)$$

7.4.1 Quadrature component of the reference source current

The error of the ac voltage at the PCC at the n^{th} sampling instant is

$$V_{er}(n) = V_{tref} - V_t(n) \quad (16)$$

Where V_{tref} is the amplitude of the reference ac terminal voltage at PCC and $V_t(n)$ is the amplitude of the sensed three phase ac voltage at PCC at the n^{th} instant. The amplitude $I_{smq(n)}$ of the quadrature component of the reference source current at n^{th} instant, is derived as output of the PI controller for maintaining ac terminal voltage constant at the n^{th} and is expressed

$$I_{smq}^*(n) = I_{smq}^*(n-1) + K_{pa} \{ V_{er}(n) - V_{er}(n-1) \} + K_{ia} V_{er}(n) \quad (17)$$

Where K_{pa} and K_{ia} are the proportional and integral gain constants of the PI controller, $V_{er}(n)$ and $V_{er}(n-1)$ are the voltage error in the n^{th} and $(n-1)^{\text{th}}$ instant. The quadrature components of the reference source currents are estimated as

$$i_{saq}^* = I_{smq}^* w_a; \quad i_{sbq}^* = I_{smq}^* w_b; \quad i_{scq}^* = I_{smq}^* w_c \quad (18)$$

7.4.2 In-phase component of reference source current

The dc bus voltage error $V_{dcer}(n)$ at the n^{th} sampling instant is and

$$V_{dcer}(n) = V_{dcref} - V_{dc}(n) \quad (19)$$

Where V_{dcref} is the reference dc voltage and $V_{dc}(n)$ is the sensed dc Link voltage of the DSTATCOM. The output of the PI controller for maintaining the dc bus voltage of the DSTATCOM at the n^{th} sampling instant is expressed as

$$I_{smd}^*(n) = I_{smd}^*(n-1) + K_{pd} \{ V_{dcer}(n) - V_{dcer}(n-1) \} + K_{id} V_{dcer}(n) \quad (20)$$

$I_{smd}^*(n)$ is considered as the amplitude of the active power component of the source current. K_{pd} and K_{id} are the proportional and integral gain constants of the dc bus PI voltage controller, respectively. In-phase components of the reference source currents are estimated as

$$i_{sad}^* = I_{smd}^* u_a; \quad i_{sbd}^* = I_{smd}^* u_b; \quad i_{scd}^* = I_{smd}^* u_c; \quad (21)$$

7.4.3 Total reference source currents

It is the sum of the in-phase and quadrature components of the reference source currents as

$$i_{sa}^* = i_{saq}^* + i_{sad}^* \quad (22)$$

$$i_{sb}^* = i_{sbq}^* + i_{sbd}^* \quad (23)$$

$$i_{sc}^* = i_{scq}^* + i_{scd}^* \quad (24)$$

7.4.4 PWM current controller

The reference source currents (i_{sa}^* , i_{sb}^* and i_{sc}^*) are compared with the sensed source currents (i_{sa} , i_{sb} and i_{sc}). The on/ off switching patterns of the gate drive of the IGBTs are generated from the PWM current controller. The current errors are computed as

$$i_{saerr} = i_{sa}^* - i_{sa}; \quad i_{sberr} = i_{sb}^* - i_{sb}; \quad i_{scerr} = i_{sc}^* - i_{sc}; \quad (25)$$

These current error signals are amplified and then compared with the triangular carrier wave. If the amplified current error corresponding to phase a (i_{saerr}) signal is greater than the triangular carrier wave signal, the switch S4 (lower device) of the phase 'a' leg of VSI is ON, switch S1 (upper device) of the phase

'a' leg of VSI is OFF. If the amplified current error signal corresponding to (i_{sref}) is less than the triangular carrier wave signal, switch S1 is ON, switch S4 is OFF. Similar logic applies to the other two phases 'b' and 'c'.

8. SPECIFIC APPLICATION AREAS OF DSTATCOM

Applications of DSTATCOM at distribution level to improve power quality is well documented in many references [5, 10-33, 41, 42, 44, 45-50, 57-77, 85-99]. The present day domestic and industrial loads induce harmonics, produce voltage dips, draw large reactive currents, cause unbalance in the supply current etc. Use of DSTATCOM helps in improving the power quality of Autonomous power systems [105] [106]. Self-excited induction generators (SEIGs) have become the back bone of Autonomous systems harnessing non-conventional energies like the wind power, micro hydro, etc. [107]-[109]. Improved control of SEIGs by Hysteresis current control techniques and other nonlinear approaches have been reported in [9, 106, 107, 108]. Controlling SEIGs to harness wind energy are discussed in [110 – 112]. For rural and remote Autonomous applications DSTATCOM with an energy storage system like battery or magnetic storage device are being widely utilized [9,109,111-119]. DSTATCOM is widely used in industries for mitigating voltage flickers caused by electric arc furnaces, rolling mills etc. [119] [120] where they can be used both in utility connected and Autonomous mode. Adjustable Speed Drives (ASDs) offer a major applications areas for the DSTATCOM [121] [122] Microgrid is another area where several Autonomous systems using VSIs to convert renewable energy or micro sources are inter-connected to provide quality power. [123]-[124]. In many Autonomous applications like aircraft, Ships and locomotives DSTATCOMs are used to provide compensation and quality power [125]-[127].

9. CONCLUSION

A review has been presented in this paper about the methods for improving the power quality aspect of the autonomous systems. DSTATCOM is the state-of-art dynamic shunt compensator of the custom power (CP) family used for Autonomous Power Systems. It is basically an offshoot of the STATCOM which is widely used to control, system dynamics under stressed condition at the transmission level. The backbone of this Autonomous Power system compensator is the self-communicating VSI built using controllable power electronic devices like IGBT, IGCT, etc. operating under PWM or hysteresis switching principle. DSTATCOM being a versatile reactive power compensator has taken the place of line commutating SVC, a relatively slow acting second generation dynamic shunt controller. In addition to the stand-alone usage of DSTATCOM in autonomous and distribution systems, this controller is an integral part of other CP devices like UPQC. Many commendable features of DSTATCOM in Autonomous systems reported with various circuit configuration and control methodologies has been reviewed in this paper to provide a clear perspective on various aspect of the device to researchers, engineers and manufacturers. A comprehensive review of the state-of-art DSTATCOM controller has been carried out in this paper to focus on new areas which has potential for research.

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