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Impact of Control Constraint on A Multi-Objective Buck Converter Design

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ABSTRACT

The current paper deals with a multi-objective design approach of power converters applied to a DC-DC buck structure. This approch consists on optimizing a preselected power architecture by minimizing a multi-objective function (volume and time response) under multi-physic constraints (efficiency, thermal, electromagnetic compatibility and control). This multi-objective optimization allows evaluating the impact of the control aspect on the converter design by considering the control criteria with the same importance as the conventional constraints. The obtained results confirm the influence of the control on the converter design parameters. They help the designer to choose suitable operating points depending on the desired performances in terms of volume and time response while respecting efficiency, junction temperatures and electromagnetic compatibility constraints.

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1. INTRODUCTION

In near future, power converters will be largely used in automotive domain. A good integration of these converters within vehicles needs to take into account multi-physic constraints during their design (thermal, efficiency, volume, cost, electromagnetic compatibility (EMC) …).

In this way, research activities have been devoted to design power converters using different approaches [1]-[9]. Most of these studies are focused on the design of defined converter architecture thanks to the designer experience. Moreover, the controller parameters calculation is carried out after the converter design so that the control aspect is decoupled from the other constraints.

Furthermore, some works have been interested to the space placement of power components to cheek thermal and electromagnetic compatibility (EMC) but just before the converter prototyping [10], [11].

In order to help the designer to select appropriate architecture and technologies and to remove risks on the 3D converter components placement early during the development phases of static converters, a dedicated pre-sizing approach carried out in three levels was developed [12].

The first level helps the designer to select easily an architecture and appropriate component technologies from specifications. Moreover, it allows estimating a major criterion (volume in our case) according to the selected technologies. The architecture choice is determined by an automated procedure according to specifications.

At the end of this first level, the designer can carry out a quick analysis about the feasibility of the application, refine the proposed choices or modify specifications.

In the second level, a mono-objective optimization under multi-physic constraints is carried out by considering the architecture and the component technologies selected in the first level. At the end of this level, optimized parameters allowing minimizing the objective function and respecting the imposed constraints are determined.

The third level consists on optimizing the space placement of the selected power components on a heat sink in order to remove the risk on the 3D integration of these components under thermal constraint (semiconductors junction temperature). This step is based on a coupling between an optimization environment (Matlab/SimulinkTM) and a finite element simulation environment (ComsolTM multi-physics). At the end of this level the optimized placement of the converter components is determined and the heat sink volume and the semiconductors junction temperatures are determined with high accuracy.

In this current paper we propose to focus on the second level to improve the optimization procedure and to explore the influence of the control aspect on a conventional design. In this context, a multi-objective optimization approach is proposed considering the control constraint with the same importance as habitual design aspects (volume, thermal, efficiency, EMC).

Preselected converter architecture and considered specifications are first presented. Then, analytical models are developed to take into account electrical, efficiency, thermal, EMC, control and volume constraints. Finally, the main results of the proposed approach are presented and the impact of the control aspect is discussed.

2. RESEARCH METHOD

To illustrate the proposed approach, a DC-DC buck converter with input filter is preselected as a support of study (Figure 1).

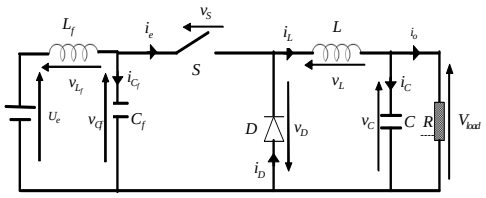

Figure 1. DC-DC Buck converter with an EMC input filter

The main considered specifications are the following:

- DC input network voltage: 42V
- DC output network voltage: 14V
- Output power: 1kW
- Thermal constraint: junction temperature ≤ 130°C
- Overall temperature 30°C
- Efficiency constraint: ≥ 80%
- Respect an EMC standard
- Electrical constraints : input and output voltage and current ripples ≤ 10% of the average values
- Objectives to be minimized: the total volume and the converter time response

In this design approach, a multi-objective optimization (volume and time response) under electrical, thermal, efficiency and EMC constraints is carried out. In order to perform this optimization, multi-physic models are developed to consider multi-physic constraints. Analytical modeling is adopted to carry out compromise between the computing time and the models accuracy [13], [14].

2.1. Electrical constraints models

Considered electrical constraints are input and output capacitors voltage ripples and input and output inductors current ripples. The calculation of these ripples depends on the converter architecture. In the case of a DC-DC buck converter (Figure 1) they can be calculated as follows [12]:

- Output (ΔV_C) and input (ΔV_{Cf}) capacitors voltage ripples:

$$\Delta V_C = \frac{\alpha \cdot (1 - \alpha) \cdot U_e}{8 \cdot L \cdot C \cdot F_s^2} \quad (1)$$

$$\Delta V_{C_f} = \frac{I_o \cdot \alpha \cdot (1 - \alpha)}{C_f \cdot F_s} \quad (2)$$

- Output (ΔI_L) and input (ΔI_{Lf}) inductors current ripples :

$$\Delta I_L = \frac{\alpha \cdot (1 - \alpha) \cdot U_e}{L \cdot F_s} \quad (3)$$

$$\Delta I_{L_f} = \frac{I_o \cdot \alpha \cdot (1 - \alpha)}{8 \cdot L_f \cdot C_f \cdot F_s^2} \quad (4)$$

Where:
U_e : the input voltage.
I_o : the mean value of the output current.
α : the duty cycle.
F_s : the switching frequency.
L and C: the buck inductance and capacitance.
L_f and C_f : the inductance and the capacitance of the input filter.

2.2. Efficiency constraint models

The efficiency model (5) considers the converter output power (Po) and the total losses dissipated in passive and active components (sum of capacitor, inductor and semi-conductor losses).

$$\text{efficiency} = \frac{P_o}{P_o + \sum \text{Losses}} \quad (5)$$

Capacitor losses:

The losses (P_c) in a capacitor can be calculated using the following simplified model:

$$P_c = R_c \cdot {I_{c\,rms}}^2 \quad (6)$$

Where R_c is the equivalent series resistance and I_{crms} the capacitor RMS current.

Inductor losses:

The losses in an inductor are due to copper and core losses.
The core losses evaluation is based on a generalized Steinmetz core loss model (7) [14].

$$P_{core} = C_m \cdot F_s^x \cdot B^y \quad (7)$$

P_{core} the core losses
F_s the operating switching frequency.
B the operating flux density.
C_m, x and y are coefficients depending on the magnetic circuit material technology, the operating frequency range and the operating temperature. These coefficients are identified from manufacturer's data sheets at the operating temperature 100°C.

Moreover, to evaluate the copper losses the following model is used (8):

$$P_{Copper} = R_L \cdot {I_{Lrms}}^2 \quad (8)$$

R_L and ILrms are the inductor resistance and RMS current.
Note that this model takes into account the skin effect by considering an 'ac' R_L resistance [15].

Semi-conductor losses:

Conduction and switching losses in a MOSFET and in a Schottky diode are calculated considering perfect current and voltage wiveformes as follows:

MOSFET :

$$P_{conduction(T_j)} = R_{s_{on}}(T_j) \cdot {I_{s_{rms}}}^2 \quad (9)$$

$$P_{switching} = \frac{1}{2} \cdot V_{s_{max}} \cdot I_{s_{max}} \cdot (T_{on} + T_{off}) \cdot F_s \quad (10)$$

Rs_{on} is the switch dynamic resistance in the conduction state which depends on its junction temperature.

Is_{rms}, Is_{max} and Vs_{max} are, respectively, the RMS current, the maximum current and the maximum voltage applied to the switch.

T_{on} and T_{off} are the switching times.

Diode:

$$P_{conduction(T_j)} = R_{d_{on}} \cdot {I_{d_{rms}}}^2 + V_d(T_j) \cdot I_{d_m} \quad (11)$$

Rd_{on} is the diode dynamic resistance.

V_d is the diode voltage drop which depends on the diode junction temperature.

Id_{rms} and Id_m are the RMS and the mean diode currents.

Note that the switching losses in the Schottky diode are obviously neglected.

2.3. Thermal constraint models

The switch and diode junction temperatures (T_{j_S} and T_{j_D}) can be estimated according to the modeling presented in Figure 2 considering a single heat sink. In this modeling, the switch and diode losses (P_S and P_D) are considered as heating sources and the thermal exchanges between a semiconductor junction and its base, between the base and the heat sink and between the heat sink and the environment are modeled by thermal resistances (junction-base: Rth_{jb_S} and Rth_{jb_D}, base-heat sink: Rth_{br_S} and Rth_{br_D}, heat sink–air: Rth_{ra}).

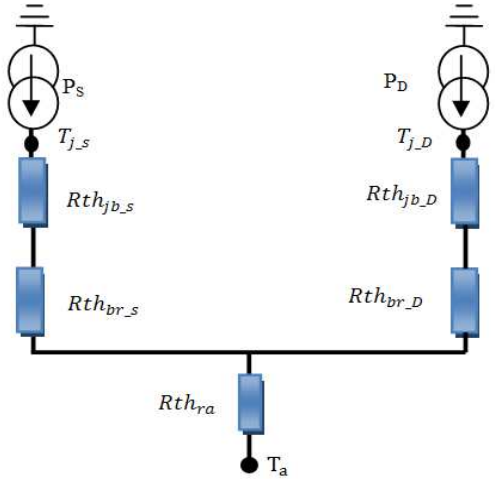

Figure 2. Electrical equivalent circuit for electro-thermal modeling of switch, diode and heat sink

Knowing the overall temperature Ta, the switch and diode junction temperatures are calculated from (12) and (13) respectively.

$$T_{j\_S} = T_a + (Rth_{jbs} + Rth_{brs}) \cdot P_{S(T_{js})} + Rth_{ra} \cdot \left[P_{S(T_{js})} + P_{D(T_{js})}\right] \quad (12)$$

$$T_{j\_D} = T_a + (Rth_{jbD} + Rth_{brD}) \cdot P_{D(T_{js})} + Rth_{ra} \cdot \left[P_{S(T_{js})} + P_{D(T_{js})}\right] \quad (13)$$

2.4. EMC constraint model

The EMC model is developed supposing that EMC disturbances can be decomposed into a differential mode and a common mode (Figure 3). From equivalent diagrams in each EMC mode, EMC disturbances can be analytically estimated [14], [16].

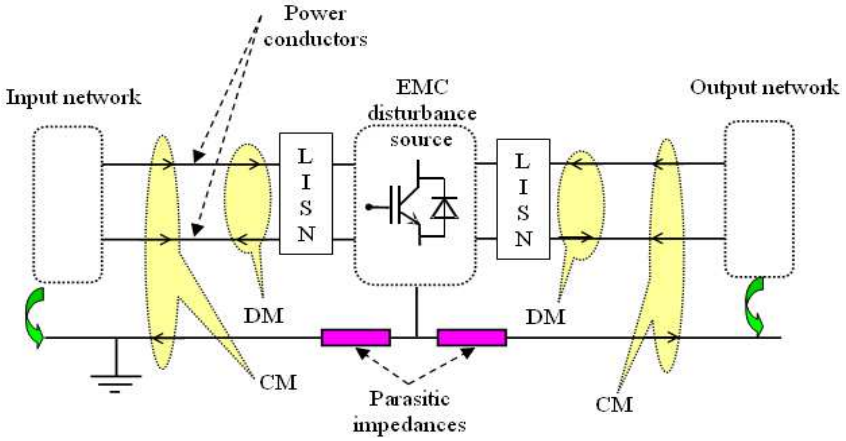

Figure 3. DM and CM EMC disturbances

The main parameters of this EMC model are the switching frequency, the inductance and the capacitance of the input filter and the maximal voltage and current in semiconductors. The aim of the design process is to determine the optimization parameters values allowing respecting the considered constraints including the EMC one.

2.5. Control constraint model

The considered control constraint is the converter stability. This constraint depends on the converter architecture and the adopted control law.

In the case of a buck converter (Figure 1) with an output voltage regulation using a PI controller, a linear open loop transfer function around the operating point (α_o,V_{co}) can be deduced (14).

$$TF_{converter}(s) = \frac{V_c(s)}{\propto(s)} = \frac{a_o}{b_o + b_1 \cdot s + b_2 \cdot s^2 + b_3 \cdot s^3 + b_4 \cdot s^4} \quad (14)$$

Where:
α: the duty cycle,
V_c: the output capacitor voltage (equals to the load voltage),
s: the Laplace transform variable,
a_o, b_o, b_1, b_2, b_3, b_4: coefficients depending on the converter parameters:

$$a_o = \frac{V_{bat}}{L_f \cdot C_f \cdot L \cdot C}$$
$$b_o = \frac{1}{L_f \cdot C_f \cdot L \cdot C}$$
$$b_1 = \frac{L_f \cdot \propto_o^2 + L}{R \cdot L_f \cdot C_f \cdot L \cdot C}$$
$$b_2 = \frac{L_f \cdot C_f + L \cdot C + L_f \cdot C \cdot \propto_o^2}{L_f \cdot C_f \cdot L \cdot C}$$
$$b_3 = \frac{1}{R \cdot C}$$
$$b_1 = 1$$

Because the presence of an EMC input filter, the stability is insured by constraining both the phase margin to be greater than or equals 45° and the real part of the closed loop poles to be strictly negative.

2.6. Multi-objective function model

In our case, two objective functions will be minimized together using Pareto front technique [17], [18]. The first one is the total volume (sum of passive and active components volumes) and the second one is the converter time response (15):

Objective= min(volume, time response) (15)

Knowing the controlled converter transfer function, the converter time response is calculated for each optimization point from the converter step response.

The volume models of passive components (inductors and capacitors) and active components (heat sink) are detailed bellow.

Capacitor volume:

At a specific maximal voltage, the volume of a capacitor is given for the considered technologies (film, tantalum and electrolytic aluminum) as a function of the capacitance (16) and by taken into account the admissible RMS current in the capacitor (17).

$$Vol_C = k_1 \cdot C^3 + k_2 \cdot C^2 + k_3 \cdot C + k_4 \quad (16)$$

$$I_{eff} = k_5 \cdot C^{k_6} \quad (17)$$

The coefficients k_i (i = 1 to 6) depend on the capacitor technology and the useful voltage applied to the capacitor. They are identified from a capacitor database for low voltage automotive applications (less or equal to 100V).

Note that equation 16 represents the volume of an elementary capacitor. If parallel connections are needed, the whole corresponding volume is deduced by multiplying the elementary volume by the number of connections.

Inductor volume:

For the inductor, four technologies are considered (Ferrite, Iron powder, MPP and High Flux). The volume (VolL) of an inductor (L) can be estimated using the following model [14]:

$$Vol_L = K_V \cdot \left(K_B \cdot \frac{L \cdot IL_{max} \cdot IL_{rms}}{B_{max} \cdot J} \right)^{\frac{3}{4}} \quad (18)$$

Where:

IL_{max} and IL_{rms}: max and RMS inductor current depending on the converter parameters including the switching frequency.

B_{max} and J: peak flux density and current density.

K_V : geometrical coefficient which characterizes the shape of the magnetic circuit.

K_B : winding coefficient which is the ratio of the winding and the copper areas.

Active component volume:

The active components volume is considered as the volume of the associated heat sink. This heat sink volume (Volhs) can be estimated by the following model:

$$Vol_{hs} = K_1 \cdot Rth_{hs}^{K_2} \cdot h \cdot e \quad (19)$$

Where:

K_1 and K_2 coefficients depending on the heat sink shape.

'h' and 'e' the height and the thickness of the heat sink respectively.

Rth_{hs} the thermal resistance of the heat sink.

These parameters are identified from manufacturer's datasheets.

3. RESULTS AND ANALYSIS

Remember that the aim is to optimize both the volume and the converter time response by respecting electrical, efficiency, thermal, EMC and stability constraints. These constraints have been introduced progressively.

Figure 4 shows the obtained Pareto optimization results (between volume and time response) under the following conditions:

- 1st case: only stability, electrical and efficiency constraints are considered,
- 2nd case: 1st case plus thermal constraint,
- 3rd case: 2nd case plus EMC constraint (all constraints are considered).

Note that the optimization has been carried out using Matlab genetic algorithm [17].

According to this Figure, the time response reduction leads to an increased converter volume and conversely. Moreover, the progressive integration of constraints yields time response and volume performances degradation which results in a Pareto curves translations. In addition, for high time response values, the volume obtained in the third case tends toward the volume of the second case. It means that the time response is adjusted in this range with the controller parameters which doesn't affect the converter volume. However, for low time response values, the time response is adjusted by both the controller and the converter parameters which increase the total converter volume.

Figure 5 shows the corresponding optimal switching frequency range variations according to the previous cases.

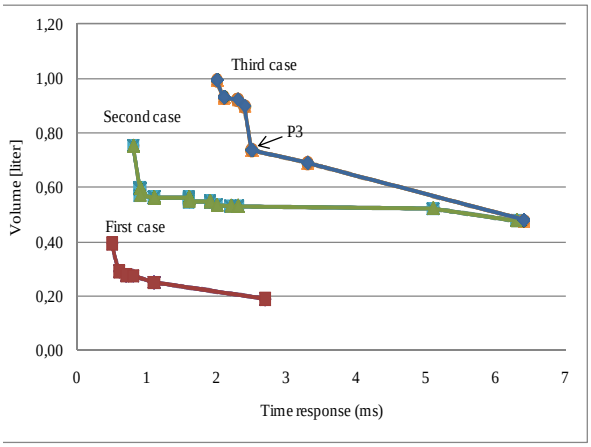

Figure 4. Pareto optimization results between volume and time response

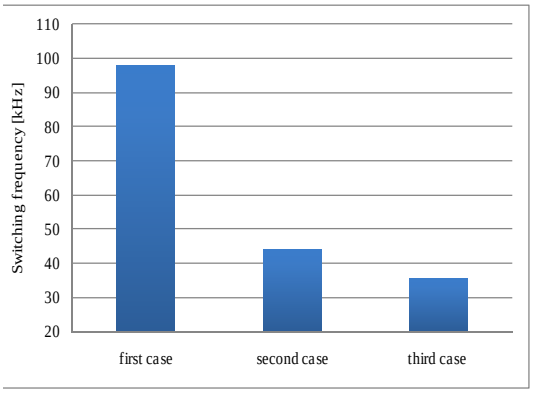

Figure 5. Optimal switching frequency range variations according to the imposed constraints

As expected, the corresponding optimal switching frequency range solution decreases by integrating more constraints. The obtained characteristics (Figures 4 and 5) show the direct impact of the control aspect on the converter design. They allow the designer to choose an operating point depending on the desired performances in terms of volume and time response.

Note that if time response performance is more important than volume constraint, the designer will choose left side solutions regarding point 'P3' on Figure 4. Otherwise, he will choose right side solutions.

Table 1 gives the main optimization results allowing to carryout compromise between the volume and the time response (point 'P3' on Figure 4 characterized by a volume of 0.73 liter and a time response of 2.5 ms).

Table 1. Main optimization results

Input filter inductance L_f (µH)	73.6
Input filter capacitance C_f (µF)	296
Output inductance L (µH)	89
Output capacitance C (µF)	190
Switching frequency F_s(kHz)	22
Heat sink thermal resistance (°C/W)	1.24
Proportional coefficient of the PI controller	$1.17\ 10^{-4}$
Integral time constant of the PI controller (µs)	5.92
Efficiency (%)	80
Switch junction temperature T_{j_S} (°C)	130
Diode junction temperature T_{j_D} (°C)	130
Maximal voltage ripple (%)	5.68
Maximal current ripple (%)	6.54

Note that to carry out compromise between volume, efficiency and thermal constraints, the obtained optimal frequency is 22 kHz. In fact, higher frequencies induce important semiconductors losses which make it impossible to respect the thermal and efficiency constraints.

Figure 6 shows the corresponding optimized EMC spectrum compared to the considered standard.

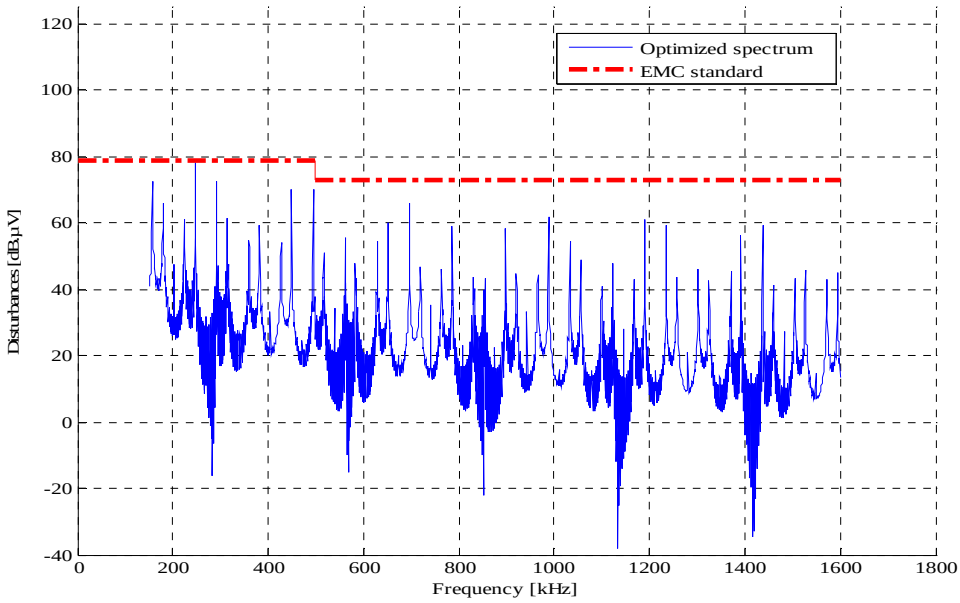

Figure 6. EMC spectrum

We can deduce that all constraints are respected. Note that the electrical constraint is largely respected (maximal ripple 6.54% compared to 10%) which means that this constraint is less important than the others constraints especially the EMC and thermal ones.

4. CONCLUSION

A multi-objective design approach of DC-DC buck converter was presented in this paper. It allowed minimizing the total volume and the converter time response under control, electrical, thermal, efficiency and EMC constraints. It has been shown that the converter control aspect has a direct impact on the converter design and should be considered with the same importance as the conventional constraints (volume, thermal, efficiency, EMC) especially if good dynamic performances are desired.

In future work, this control aspect will be considered in presence of some converter defaults (loss of voltage sensor information's for example). The aim will be the integration in the optimization approach of fault tolerant control architecture to insure uninterrupted operation.

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Claude Marchand is graduated from the Ecole Normale Supérieure de Cachan and he received the phD degree from Université Paris VI in 1991. Since 1988 he is with the Laboratoire de Génie Electrique de Paris (LGEP). From 1994 to 2000, he was assistant professor at the Institut Universitaire de Technologie of Cachan (Université Paris-Sud). Since 2000 he is professor at the Université Paris-Sud. He is head of the LGEP research department "Modelling and Control of Electromagnetic Systems". His research interests are in eddy current non-destructive testing and in design and control of electrical actuators.