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DSTATCOM Control Algorithms: A Review

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ABSTRACT

The concept that an inverter can be used as a generalized impedance converter to realize either inductive or capacitive reactance has been widely used to mitigate power quality issues of distribution networks. One such device is the DSTATCOM which is connected in shunt at the load end. The heart of the DSTATCOM is a converter. The control algorithm of the converter is very important. It causes the converter to address the power quality problems in efficient manner. This paper discusses the various control algorithms of the converter. The manners in which the power quality issues are mitigated by the converter are also explored. Simulations of the control algorithms are made on MATLAB platform to ascertain the effectiveness of each control method for power quality mitigation.

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1. INTRODUCTION

The development of technology and consequent up gradation of the loads of power system has brought about a paradigm change in the customer's outlook for the electrical power he is willing to receive. Adding to the problem of reactive power compensation [1], the proliferation of nonlinear loads is causing a higher level of harmonics in the received voltage. An alert customer now asks for a power supply that is voltage regulated, balanced, flickers free, without harmonics and without any outages. The concept of custom power was introduced by Hingorani [2]. Similar to FACTS devices which are used to solve issues related to the transmission lines, the custom power (CP) devices relates to the use of power electronic controllers to solve issues related to the distribution systems. Of the many CP devices available, DSTATCOM can solve most of the customer's load related power quality problems.

The concept of compensation has its genesis to reactive power compensation [3], which initially was conceived with fixed or passive capacitors. Later, Static var Compensator came into use for var compensation and voltage regulation at the load end [4]-[7]. These systems suffered from the following drawbacks: suffered from granularity or the minimum amount of var compensation possible; they exhibited poor dynamic performances; they had to be supplemented with filters as they injected harmonics into the network; they failed under low voltage conditions; and they did not provide for load balancing and load leveling.

The answer to the above was found in the DSTATCOM, which was conceived from the concept of STATCOM [8]-[10] used for transmission line compensation. A DSTATCOM [11]-[13] is basically a shunt connected bidirectional converter based device which can act as generalized impedance converter to realize either inductive or capacitive reactance by changing its output voltage levels [14]. By proper tracking of the

load current the converter can generate such voltages and currents so that the harmonics and oscillations generated by the load current do not get transmitted to the supply side. A state of art DSTATCOM is capable of cancelling or suppressing; the effect of poor load power factor, the effect of poor voltage regulation, the harmonics introduced by the load, the dc offset in loads such that the current drawn from the source has no offset, the effect of unbalanced loads such that the current drawn from the source is balanced, and if provided with an energy storage system, it can perform load leveling when the source fails.

2. PRINCIPLE OF LOAD COMPENSATION BY DSTATCOM

The schematic diagram for load compensation using DSTATCOM is shown in Figure 1. A current controlled voltage source converter is assumed at the heart of the DSTATCOM. Hence for an ideal case, the DSTATCOM is replaced by an ideal current source i_c. Further, as is generally the case, the load is assumed to be reactive, nonlinear and unbalanced. First, assume the load L-1 is without a compensator. Hence, i_s flowing through the feeder is also unbalanced & distorted and consequently, voltage at PCC bus will also be unbalanced & distorted.

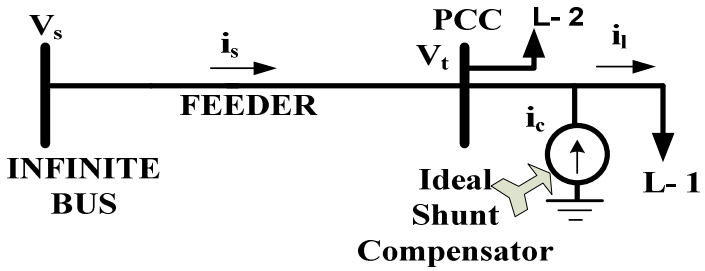

Figure 1. Schematic Diagram of Load Compensation.

Ideally, the utility would like to see a load drawing unity power factor with fundamental and positive sequence current. Without the compensator, i_s will be same as i_l i.e. reactive, unbalanced and distorted. To mitigate the problem, the compensator must inject current such that i_s becomes fundamental, positive sequence and in-phase with the PCC voltage. Applying KCL to PCC,

$$i_s + i_c = i_l$$
$$\text{hence} \quad i_s = i_l - i_c \tag{1}$$

Thus, the compensator must generate a current i_c such that it cancels the reactive, harmonic and the unbalance components of the load current.

3. SYSTEM CONFIGURATION

A typical distribution system has been considered for studying the working of the DSTATCOM and its controls there in. Figure 2 shows the proposed distribution side of the power system, consisting of an Infinite bus, the DSTATCOM and the delta connected RL load.

4. OVERVIEW OF CONTROL ALGORITHMS

The essential features of any control scheme are fast response, flexibility, robustness and ease of implementation. For a DSTATCOM, the control algorithm is implemented by using the following steps:

- The supply and the load voltages & currents are measured using either Hall Effect transducers or any other sensor.
- The supply reference current is calculated first.
- The compensating current of the DSTATCOM is then calculated.
- Comparing the load current with the compensating current, the triggering pulses for the IGBTs of the inverter bridge are then produced.
- This causes the inverter to produce the requisite compensating current to perform the load compensation.

Generation of proper triggering pulses for the IGBTs of the VSC is very crucial for proper implementation of the load compensation.

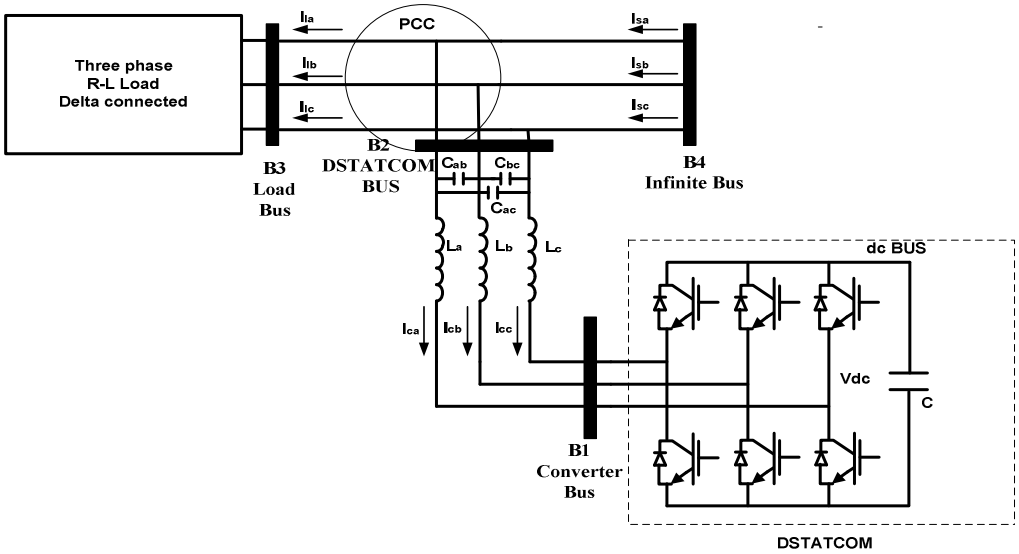

Figure 2. Schematic of a typical Distribution System compensated by DSTATCOM.

The advent of the low switching loss IGBTs has enabled the designers to shift from Fundamental Frequency Switching (FFS) to Pulse Width Modulation (PWM). Further, custom power being a relatively low power application, PWM methods offer a more flexible option than fundamental frequency switching methods favored in FACTS applications. Though various topologies of VSC have been reported, single 3-phase bridge with six IGBT switches is widely reported for DSTATCOM. From time to time, various schemes were reported to generate the pulses for turning on the inverter switches, with each scheme having some or the other advantages. It has been observed that all the schemes broadly fall into the following categories: phase shift control, carrier based PWM control, and carrier less hysteresis control.

DSTATCOM is simulated on MATLAB platform using each of the control schemes and their performances are compared. The parameters of the system used are given in the annexure.

5. PHASE SHIFT CONTROL

The Phase Shift Control [15] scheme is simple. The objective is to maintain a constant voltage at the load terminal. The control algorithm exerts a voltage angle control and generates a phase shift in the output voltage of the VSC with respect to the ac supply voltage. An error signal is generated by comparing the measured PCC voltage with the desired or the reference voltage. The error signal is fed to a PI controller to generate an angle δ to drive the voltage error to zero. Thus the PCC voltage is regulated at the desired value. The PWM generator phase-modulates the sinusoidal voltage signal by angle δ and generates the switching signals for the VSC switches by comparing it with a triangular carrier signal. The dc side voltage is maintained by a separate dc source. A schematic diagram for phase shift control of DSTATCOM is shown in Figure 3.

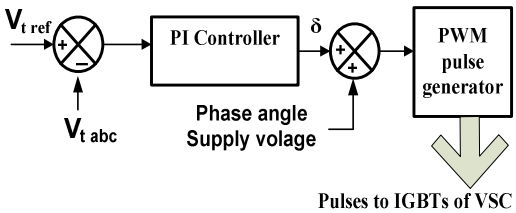

Figure 3. Schematic diagram for phase shift control.

The positive aspects of this type of control are: this control algorithm is easy to implement and is sufficiently robust, and requires only voltage measurement. Current and reactive power measurements are not required. However, it suffers from the following disadvantages:

- It does not have a self supporting dc bus and requires a separate dc source to pre-charge the dc side capacitor & maintain its voltage during the operation of DSTATCOM.
- It assumes that the supply side voltage is balanced and without harmonics, since fundamental wave form is used to obtain the phase angles of the supply wave form.
- There is no provision for harmonic suppression in case the load connected to PCC is nonlinear.
- This method results in generation of active power by the VSC along with the var.

This method is not much reported because of the above deficiencies. Hence simulation of this method is not carried out.

6. CARRIER BASED PWM CONTROL.

The schematic diagram for the Carrier based PWM Control is shown in Figure 4. A fixed frequency carrier based sinusoidal PWM is used for generating the switching pulses for the IGBTs of the VSC [16]-[19]. This algorithm is based on the instantaneous reactive power theory. The instantaneous voltage and current of the supply system and the load are measured. The three-phase system is transformed to a synchronously rotating reference frame using Park's transformation [20] [21]. Compensation is achieved by control of i_d and i_q. The real power p and the reactive power q injected into the system by the DSTATCOM, under dq reference frame is given by :

$$p = v_d i_d + v_q i_q \quad (2)$$
$$q = v_q i_d - v_d i_q \quad (3)$$

For a balanced three phase system $v_q = 0$ [16]. Thus the id and iq completely describes the instantaneous value of real and reactive power produced by the DSTATCOM.

$$p = v_d i_d \text{ and } q = -v_d i_q \quad (4)$$

The instantaneous i_d reference current is generated by PI regulation of the dc terminal voltage with respect to a reference dc voltage. Similarly, i_q reference current is generated by PI regulation of the ac terminal voltage of the VSC with respect to a reference ac terminal voltage [18][19]. In case only power factor correction is desired, the reference i_q is set to zero. The decoupled i_d and i_q components obtained from abc to dq transformation of the measured instantaneous three phase current, are then regulated with two separate PI regulators with respect to the reference i_d and i_q currents obtained earlier. In order to synchronize abc to dq0 transformation, a Phase Locked Loop (PLL) is used.

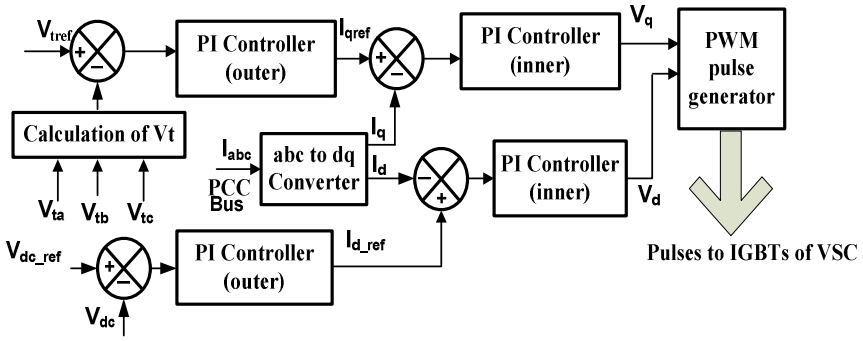

Figure 4. Schematic diagram for carrier based control.

7. ALGORITHM OF CARRIER BASED CONTROL OF DSTATCOM.

The control of VSC of the DSTATCOM, shown in Figure 4, is modeled in discrete mode using ode23tb on MATLAB platform [22]. The discrete-time integrator block [23] is used to implement the PI controller. Forward Euler method is used for integration. The discrete-time integrator block approximates 1/s by T/(Z-1), which results in the following expression for the output Y(n) at the n^{th} step .

$$Y(n) = Y(n-1) + KT^* U(n-1) \quad (5)$$

Where U(n-1) is the input to the controller at the $(n-1)^{th}$ step. T is the discretization time interval.

7.1. *Terminal Voltage Control.*

The three phase supply voltages (v_{sa} v_{sb} and v_{sc}) are considered sinusoidal and hence their amplitudes are computed as:

$$V_t = \sqrt{\{(2/3)\ (v^2_{sa} + v^2_{sb} + v^2_{sc})\}} \quad (6)$$

The value of V_t computed above is compared with the desired terminal voltage V_{tref}. The ac voltage error $V_{er(n)}$ at the n^{th} sampling instant is

$$V_{er(n)} = (V_{tref} - V_{t(n)}) \quad (7)$$

Where $V_{t(n)}$ is the amplitude of the sensed three phase ac voltage at the PCC terminal at the n^{th} instant. The error $V_{er(n)}$ is fed to an outer PI controller, using discrete time integration, to generate the I_{qref} .

$$I_{qref\,(n)} = I_{qref\,(n-1)} + K_{ap}\{V_{er(n)} - V_{er(n-1)}\} + K_{ai} V_{er(n)} \quad (8)$$

Where K_{ap} and K_{ai} are the proportional and integral gain constants of the outer PI controller of the ac terminal voltage at the PCC

The actual value of I_q is generated by an abc to dq convertor using Park's transformation over the load current. The I_{qref} and I_q components are compared and the error is fed to an inner PI current controller to generate V_q .

$$I_{qer(n)} = (I_{qref\,(n)} - I_{q(n)}) \quad (9)$$
$$V_{q(n)} = V_{q(n-1)} + K_{bp}\{I_{qer(n)} - I_{qer(n-1)}\} + K_{bi} I_{qer(n)} \quad (10)$$

Where K_{bp} and K_{bi} are the proportional and integral gain constants of the inner PI controller of the ac terminal voltage at the PCC

7.2. *Control of the Voltage at the dc terminal of the DSTATCOM.*

The V_{dc} of the dc bus is compared with the desired dc bus voltage V_{dc_ref}.
The dc voltage error $V_{der(n)}$ at the n^{th} sampling instant is

$$V_{dcer(n)} = (V_{dc\_ref} - V_{dc(n)}) \quad (11)$$

Where $V_{dc(n)}$ is the sensed dc voltage at the dc bus of the DSTATCOM at the n^{th} instant.
The error is then fed to an outer PI controller to generate I_{dref} .

$$I_{dref\,(n)} = I_{dref\,(n-1)} + K_{ap}\{V_{dcer(n)} - V_{dcer(n-1)}\} + K_{ai} V_{dcer(n)} \quad (12)$$

Where K_{ap} and K_{ai} are the proportional and integral gain constants of the outer PI controller of the dc bus voltage.

The actual I_d is generated by an 'abc to dq convertor using parks transformation over the load current. The signals I_{dref} and I_d are compared and the error is fed to an inner PI current controller to generate V_d

$$I_{der(n)} = (I_{dref\,(n)} - I_{d(n)}) \quad (13)$$
$$V_{d(n)} = V_{d(n-1)} + K_{bp}\{I_{der(n)} - I_{der(n-1)}\} + K_{bi} I_{der(n)} \quad (14)$$

Where K_{bp} and K_{bi} are the proportional and integral gain constants of the inner PI controller of the dc bus voltage.

7.3. *PWM current Controller.*

The V_d and V_q signals generated above are converted into modulation index 'm' and phase 'ϕ' which are then used by the PWM modulator for producing the required pulses for triggering the IGBTs of the VSC. This causes the VSC to maintain the terminal voltage of the generator by generating / absorbing the required reactive current and supplying / absorbing active power from the generator to maintain the dc side voltage of the inverter.

The advantageous features of this scheme are:
- It incorporates a self supporting dc bus
- The active and reactive power control achieved through i_d and i_q control are decoupled from each other.
- The dc bus control/ regulation are decoupled from the ac bus control like voltage regulation or power factor correction and load balancing.
- Switching of devices of VSC is done at fixed frequency. Thus switching losses can be limited within the rating of the devices.
- This type of control is inherently linear & robust and uses PI or PID controls, which are very easy to implement in real time and are less complex in hardware.

However it suffers from the following disadvantages:
- Very little harmonic suppression is achieved. Additional series and shunt filters need to be connected for removal of harmonics.
- As four PI controllers are used, response time is more.
- The scheme is based on synchronization with the fundamental frequency using a PLL. In the case of distorted mains the PLL may produce errors.
- The scheme is applicable for balanced three phase three wire systems. It cannot be used for single phase systems.
- During transient conditions, the supply current shoots up to a very high value.
- A larger series filter can be connected on the ac side to limit transients and harmonics. However it shall reduce the var generating capacity of the VSC.

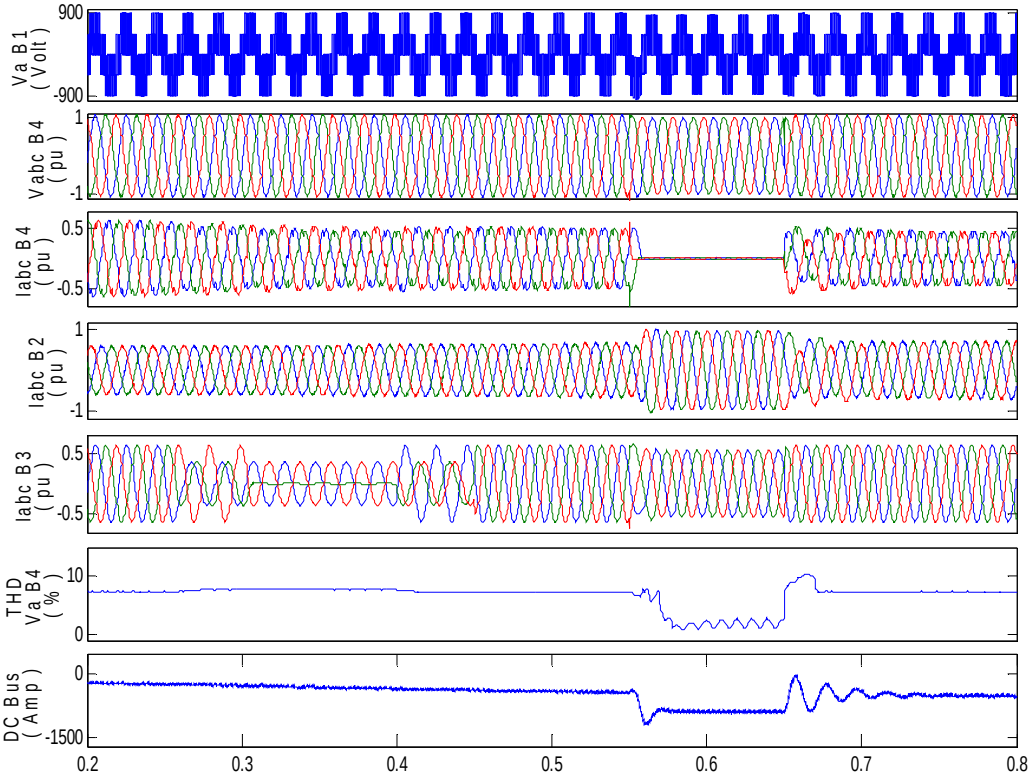

Figure 5. Response of DSTATCOM using carrier based PWM.

Figure 5 shows the simulated results of the DSTATCOM for a linear RL load, demonstrating voltage regulation, load balancing and load leveling. Simulation starts with three phase delta connected load. The supply current $I_{abc\ B4}$ & supply voltage $V_{abc\ B4}$ are balanced with the supply voltage at 1.0 pu. At 0.25s one phase is disconnected from the supply at PCC. Then at 0.3s another phase is disconnected, leaving only one phase connected to the supply. At 0.4s and 0.45s, one phase followed by another phase is reconnected to PCC, giving again a balanced load.

During the period 0.25s to 0.45s, although the load current $I_{abc\ B3}$ is unbalanced, the supply current $I_{abc\ B4}$ & voltage $V_{abc\ B4}$ are very little affected, resulting in the voltage being regulated at 1.0pu and also

demonstrating the load balancing capability of DSTATCOM. During the period 0.55s to 0.65s, the supply is disconnected from the load ($I_{abc\ B4} = 0$). However the DSTATCOM maintains the power supply to the load with the energy source connected at its dc bus, and the load current $I_{abc\ B3}$ is maintained at the same level i.e., 0.6pu. This demonstrates the load leveling capability of DSTATCOM.

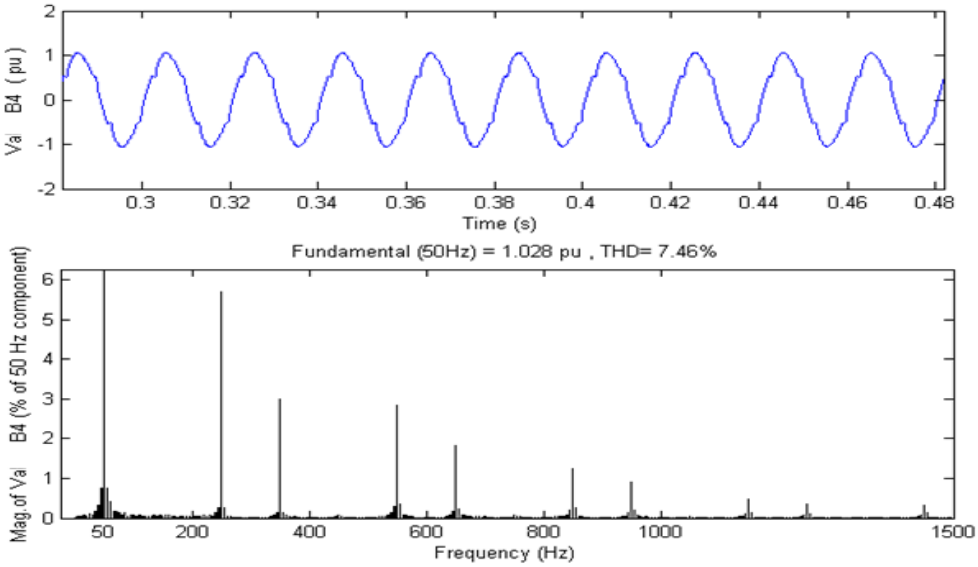

Figure 6. Harmonic Spectrum of source voltage for carrier based PWM control.

Figure 6 demonstrates the harmonic spectrum of the source voltage $V_{a\ B4}$ with balanced and unbalanced linear load. The total harmonic distortion of the voltage is very small. The DSTATCOM effectively compensates the harmonics of the consumer loads. This is achieved using series and shunt filters.

8. CARRIER LESS HYSTERISIS CONTROL.

This compensation scheme is very versatile and is widely reported for power factor correction and voltage regulation, in addition to load balancing, harmonic suppression and load leveling [24]-[27]. Various methods are reported for deciding the magnitude of the reference active and reactive current to be generated by the DSTATCOM. Simplest method reported is with the use of PI controller.

Figure 7 shows the control scheme for PI controller based carrier less hysteresis controller. The unit vectors for the in-phase and the quadrature voltages are obtained from the supply voltage. The in-phase unit vectors (u_a, u_b and u_c) are computed by dividing the ac voltages v_a, v_b and v_c by their amplitude V_t. Another set of vectors called the quadrature unit vectors (w_a, w_b and w_c) is a sinusoidal function, obtained from in-phase vector set (u_a, u_b and u_c). To regulate the PCC terminal voltage, its amplitude V_t is compared with the desired voltage V_{tref} and the error is processed by a PI controller. The output of the PI controller (I^*_{smq}) decides the amplitude of the reactive current to be generated by the DSTATCOM. Multiplication of the quadrature unit vectors (w_a, w_b and w_c) with I^*_{smq} yields the quadrature component of the reference current (i^*_{saq}, i^*_{sbq} and i^*_{scq}).

To provide self supporting dc bus for the DSTATCOM, the charging current must be provided from the PCC. In order to achieve this, the dc bus voltage (V_{dc}) is sensed and compared with the dc reference voltage (V_{dcref}). The error voltage is processed by a second PI controller. The output of the PI controller (I^*_{smd}) decides the amplitude of the active power component of the source current. Multiplication of the in-phase vectors (u_a, u_b and u_c) with I^*_{smd} yields the in-phase component of the reference source currents (i^*_{sad}, i^*_{abd} and i^*_{scd}). The reference source currents (i_{sa}, i_{sb} and i_{sc}) are obtained by adding the corresponding in-phase and the quadrature components. A pulse width modulation (PWM) current controller then compares the reference source currents (i^*_{sa}, i^*_{sb} and i^*_{sc}) with sensed source currents (i_{sa}, i_{sb} and i_{sc}) to generate the switching signals for the IGBTs of the DSTATCOM.

The hysteresis controller adds a hysteresis band ± h around the calculated reference current. When (i_{sa} - i^*_{sa}) > +h, pulses are generated for the lower level switches and when (i_{sa} - i^*_{sa}) < -h, pulses are generated for the upper level switches of the VSC.

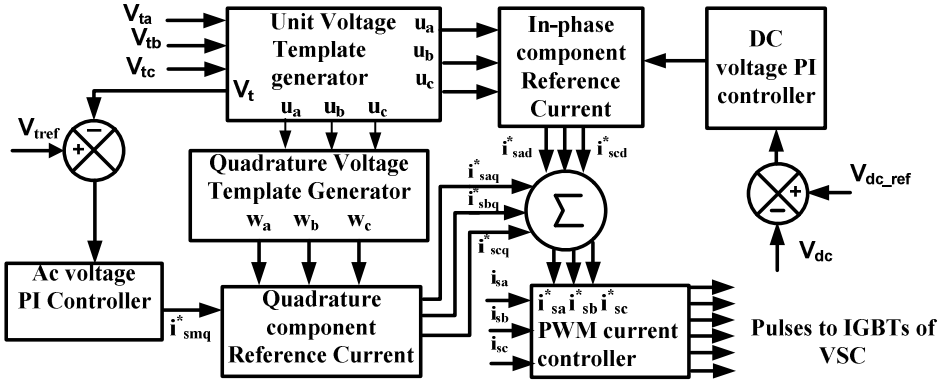

Figure 7. Schematic diagram for Carrier-less hysteresis control of DSTATCOM.

9. ALGORITHM OF CARRIER LESS HYSTERESIS CONTROL.

The three phase voltages at the PCC (v_a, v_b and v_c) are sinusoidal and hence their magnitude is computed as:

$$V_t = \sqrt{\{(⅔)(v^2_a + v^2_b + v^2_c)\}} \quad (15)$$

The unit vectors u_a, u_b and u_c are derived as

$$u_a = v_a / V_t; \quad u_b = v_b / V_t \; ; \quad u_c = v_c / V_t \; ; \quad (16)$$

The unit vectors in quadrature (w_a, w_b and w_c), are derived from the in-phase unit vectors (u_a, u_b and u_c), using the following transformation

$$w_a = -u_b / \sqrt{3} + u_c / \sqrt{3} \; ; \quad (17)$$
$$w_b = \sqrt{3}\, u_a /2 + (u_b - u_c) / 2\sqrt{3}; \quad (18)$$
$$w_c = -\sqrt{3}\, u_a / 2 + (u_b - u_c) / 2\sqrt{3}; \quad (19)$$

9.1. Quadrature component of the Reference Source Current.

The error of the ac voltage at the PCC at the n^{th} sampling instant is

$$V_{er(n)} = V_{tref} - V_{t(n)} \quad (20)$$

Where V_{tref} is the amplitude of the reference ac terminal voltage at PCC and $V_{t(n)}$ is the amplitude of the sensed three phase ac voltage at PCC at the n^{th} instant. The amplitude $I^*_{smq(n)}$ of the quadrature component of the reference source current at n^{th} instant, is derived as output of the PI controller for maintaining ac terminal voltage constant at the n^{th} instant and can be expressed as :

$$I^*_{smq(n)} = I^*_{smq(n-1)} + K_{pa}\{V_{er(n)} - V_{er(n-1)}\} + K_{ia}V_{er(n)} \quad (21)$$

In the above, K_{pa} and K_{ia} are the proportional and integral gain constants of the PI controller, $V_{er(n)}$ and $V_{er(n-1)}$ are the voltage error in the n^{th} and $(n-1)^{th}$ instant. The quadrature components of the reference source currents are estimated as

$$i^*_{saq} = i^*_{smq}\, w_a \; ; \quad i^*_{sbq} = i^*_{smq}\, w_b \; ; \quad i^*_{scq} = i^*_{smq}\, w_c \; ; \quad (22)$$

9.2. In-Phase Component of Reference Source Current.

The dc bus voltage error $V_{dcer(n)}$ at the n^{th} sampling instant is

$$V_{dcer(n)} = V_{dcref} - V_{dc(n)} \quad (23)$$

where V_{dcref} is the reference dc voltage and $V_{dc(n)}$ is the sensed dc link voltage of the DSTATCOM.

The output of the PI controller for maintaining the dc bus voltage of the DSTATCOM at the n^{th} sampling instant is expressed as

$$I^*_{smd(n)} = I^*_{smd(n-1)} + K_{pd}\{V_{dcer(n)} - V_{dcer(n-1)}\} + K_{id}V_{dcer(n)} \quad (24)$$

$I^*_{smd(n)}$ is considered as the amplitude of the active power component of the source current. K_{pd} and K_{id} are the proportional and integral gain constants of the dc bus PI voltage controller, respectively. In-phase components of the reference source currents are estimated as

$$i^*_{sad} = i^*_{smd}\, u_a\,; \quad i^*_{sbd} = i^*_{smd}\, u_b\,; \; i^*_{scd} = i^*_{smd}\, u_c\,; \quad (25)$$

9.3. Total Reference Source Currents.

The total reference source current is the sum of in-phase and quadrature components of the reference source currents.

$$i^*_{sa} = i^*_{saq} + i^*_{sad} \quad (26)$$
$$i^*_{sb} = i^*_{sbq} + i^*_{sbd} \quad (27)$$
$$i^*_{sc} = i^*_{scq} + i^*_{scd} \quad (28)$$

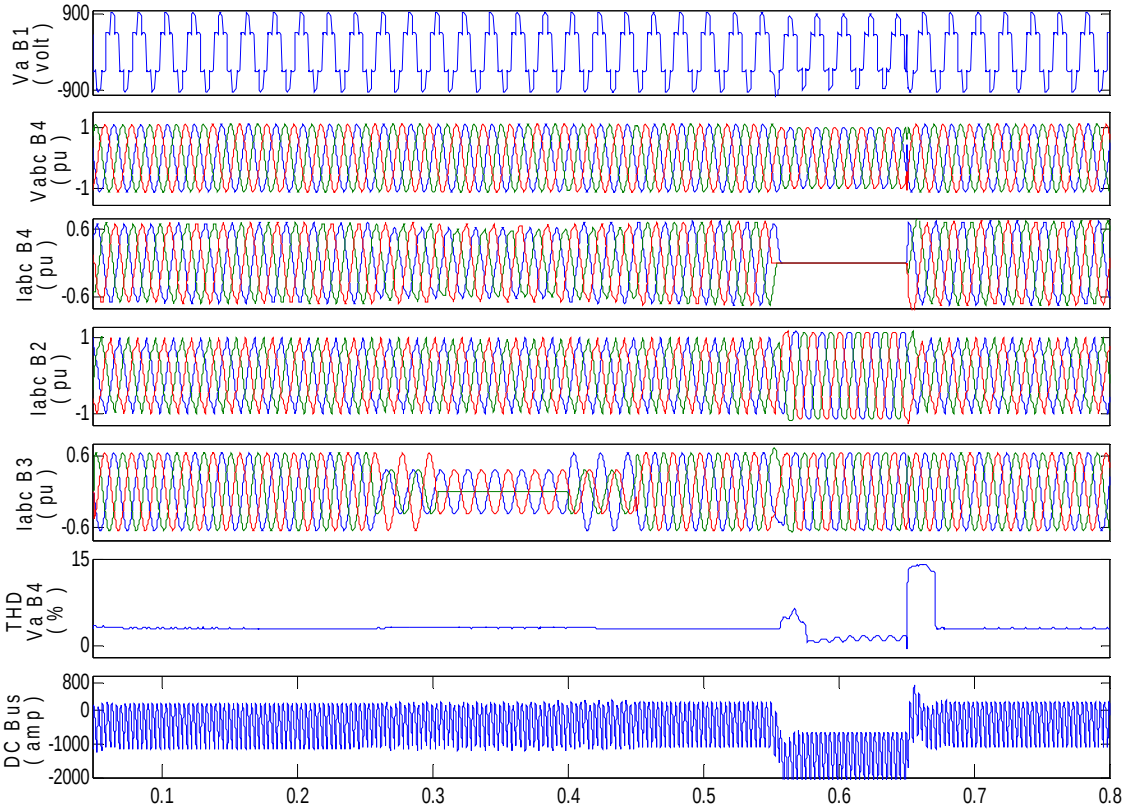

Figure 8. Response of DSTATCOM using carrier less hysteresis current control.

9.4. PWM Current Controller.

The reference source currents (i^*_{sa}, i^*_{sb}, and i^*_{sc}) are compared with the sensed source currents (i_{sa}, i_{sb}, and i_{sc}). The on/off switching patterns of the gate drive of the IGBTs are generated from the PWM current controller. The current errors are computed as

$$i_{saerr} = i^*_{sa} - i_{sa}\,; \quad i_{sberr} = i^*_{sb} - i_{sb}\,; \quad i_{scerr} = i^*_{sc} - i_{sc} \quad (30)$$

These current error signals are amplified and then compared with the triangular carrier wave. If the amplified current error corresponding to phase 'a' (i_{saerr}) signal is greater than the triangular carrier wave

signal, the switch S4 (lower device) of the phase 'a' leg of VSC is made ON, switch S1 (upper device) of the phase 'a' leg of VSC is made OFF. If the amplified current error signal corresponding to (i_{saerr}) is less than the triangular carrier wave signal, switch S1 is made ON and switch S4 is made OFF. Similar logic applies to the other two phases 'b' and 'c'.

Figure 8 shows the simulated results of the DSTATCOM for a linear RL load, demonstrating voltage regulation, load balancing and load leveling. The simulation starts with three phase delta connected load. The supply current $I_{abc\ B4}$ & supply voltage $V_{abc\ B4}$ are balanced with the supply voltage at 1.0pu. At 0.25s, one phase is disconnected from the supply at PCC. Then, at 0.3s, another phase is disconnected, leaving only one phase connected to the supply. At 0.4s and 0.45s, one phase followed by another phase is reconnected to PCC, giving again a balanced load. During the period 0.25s to 0.45s, although the load $I_{abc\ B3}$ is unbalanced, the supply current $I_{abc\ B4}$ and voltage $V_{abc\ B4}$ are very little affected, with the voltage being regulated at 1.0 pu. This demonstrates the load balancing capability of DSTATCOM. During the period 0.55s to 0.65s, the supply is disconnected from the load ($I_{abc\ B4}$ = 0). However, the DSTATCOM maintains the supply to the load with the energy source connected at its dc bus and the load current is maintained at the same level i.e., 0.6pu. This demonstrates the load leveling capability of DSTATCOM.

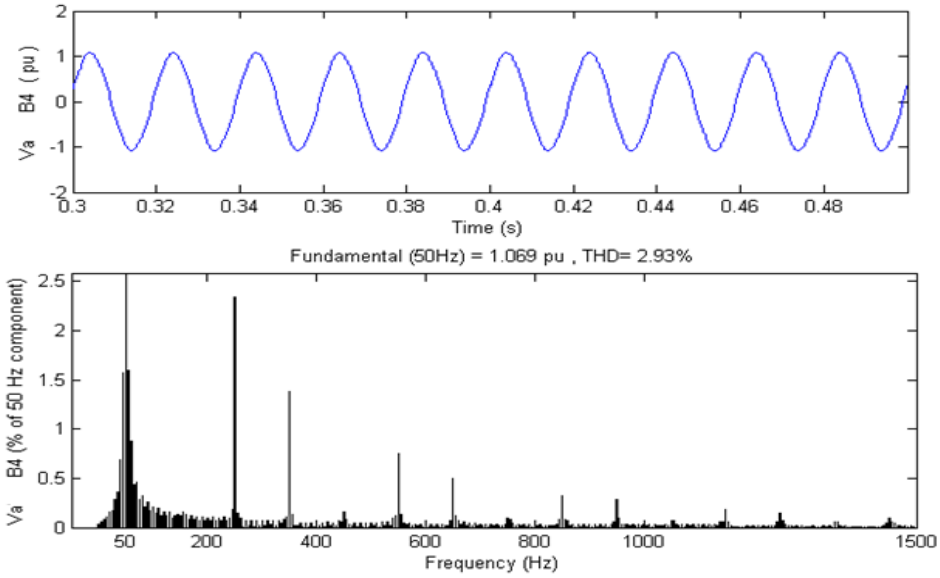

Figure 9. Harmonic Spectrum of Source Voltage for Carrier less Hysteresis control.

Figure 9 demonstrates the harmonic spectrum of the source voltage $V_{a\ B4}$ with balanced and unbalanced linear load. The total harmonic spectrum of the voltage is very small. The DSTATCOM compensates the harmonics of the consumer loads to within that specified by IEEE 519 standards without any additional filters.

The negative aspects of this scheme are: the ripples on the dc side are greatly increased (as shown in Figure 8) and needs proper filtering; switching of the converters, depending on the dynamics of load, may be at considerable high frequency, causing excessive switching losses in the devices; and hardware implementation of the control is complex and more difficult to configure.

Some of the positive factors of this scheme are:

- The algorithm has built-in property of self supporting dc bus.
- It is very simple, robust and has automatic current limiting capability.
- Its transient response is better.
- It can limit the THD of source current to around 2.93%, which is within IEEE – 519 standard.
- It has two PI controllers as compared to four in the earlier case. It also does not require a PLL and the complex abc to dq transformation. This enhances its dynamic response.
- The algorithm can be easily modified to incorporate advanced control methods in place of the two PI controllers to enable quicker estimation of reference currents, resulting in better response for the DSTATCOM.
- Compensation for three phase four wire systems can be easily achieved with addition of a fourth leg to the VSC and a separate control for the same.

10. CONCLUSION

A comparative study of the basic algorithms used for control of DSTATCOM is presented in this chapter. The merits and demerits of each scheme are brought out by conducting simulation studies. It is found that a DSTATCOM, notwithstanding the algorithm used, does reactive power compensation, voltage regulation, harmonic reduction, load balancing and load leveling.

APPENDIX

DSTATCOM	INFINITE BUS	LOAD
Rated voltage = 415 V, 3 Phase, 50 Hz.	Rated Voltage = 415 V, 3 Ph. 50	3 ph. Delta connected load with
Interface inductor = 800μH, 0.004Ω	Hz.	Per ph. P = 100 kW & Q = 5 kvar.

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