

Closed Loop Control of Soft Switched Interleaved Buck Converter

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Article Info

Article history:

Received Jul 24, 2012

Revised Aug 15, 2012

Accepted Aug 21, 2012

Keyword:

Buck converter

Interleaved

Microcontroller

Resonant component

Zero Current Switching

ABSTRACT

Design, Modeling and Simulation of a closed loop control is presented for Interleaved Buck Converter with Soft Switching. The features of the closed loop system are to reduce the switching losses and load current sharing among the parallel connected converters. The control system of the converter is designed using PWM technique. In order to improve the transient response and dynamic stability of the converters, the controller parameters are designed based on current mode control. Resonant components thus designed enable the application of zero current switching for both the converters connected in parallel thereby maintaining greater efficiency and minimizing voltage and current oscillations. The system analysis, design and performance are verified through simulation using MATLAB/Simulink environment. The simulation approach reveals the high speed dynamic performance of the closed loop system designed using robust PID controller. The laboratory prototype of the Buck converter is developed to verify the controller platform using PIC16F877A microcontroller.

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1. INTRODUCTION

Switched mode dc-dc converters are the most efficient power electronic systems that convert an unregulated dc input voltage into a regulated dc output voltage. Switched mode power supplies when compared with the linear power supplies are smaller in size, much more efficient and have high power density. Therefore they are used extensively in personal computers, computer peripherals, communication, medical electronics and adapters of consumer electronic devices to provide different level of dc voltages. Among the basic topologies of dc-dc converters buck converters are widely used in portable consumer electronics. In general dc-dc converters are time invariant, non linear dynamic systems. The non linear nature of the dc-dc converters arise mainly due to switching power devices, inductors and capacitors. One inherent disadvantage of buck converter is its reliance on large passive components. The increase in switching frequency reduces the size of components but it leads to various converter losses thereby reducing the efficiency when used particularly in light loads. In order to overcome these limitations soft switching methods are used [1].

Soft switching techniques such as zero voltage switching and zero current switching substantially reduce the switching losses resulting in higher efficiency. This paper particularly deals with zero current switching which facilitates the following advantages: (i) Before the initiation of the next switching cycle the inductor current is zero inferring higher efficiency. (ii) Zero current switching always forces the inductor to begin its charging at zero current which limits the peak value of the inductor current to

exactly twice the average current. This is quite desirable for both steady states and instantaneous switching cycle relationships [2].

In high power applications, it is often required to associate the converters in series or in parallel due to the unavailability of a single device to withstand the voltage stress or current stress. The advantages of connecting the converters in parallel called interleaving are: (i) input current ripple is reduced (ii) inductor size is reduced (iii) current rating of the semiconductors are reduced (iv) good current sharing among the converter modules (v) I^2R losses and inductor ac losses are reduced (vi) easier system maintenance and expansion (vii) increased system reliability. The main challenge in the field of Power Electronics is emphasized more on the control aspects of the dc-dc converters. The control approach requires effective modeling and a thorough analysis of the converters.

The main objective of a control scheme is to make the system to track the desired reference input even in the presence of noise, modeling error and disturbances. In control system, controller plays a vital role by generating appropriate control signal for the system to regulate the performance. In spite of the advancements in process control techniques, PID (Proportional – Integral – Derivative) controller is still popular in closed loop control. In most of the industries PID controllers are widely used due to their simplicity, applicability, low power consumption and ease of implementation. A simple Ziegler-Nichols tuning rule is one of the most popular methods of tuning to obtain reasonable good initial setting of PID controllers because of familiarity and ease of use [3].

The design of feedback compensator requires a dynamic model of the switching converter. In order that the transient analysis and control design are easy a number of equations must be solved in a sequence. This problem can easily be solved by arriving at a single equation describing the converter approximately over a number of switching cycles using state space averaging technique. The zero current switching (zcs) interleaved Buck converter with PID controller has been designed, modeled and simulated using MATLAB/Simulink. The main objective is to implement this control scheme to the converter which describes its operation, implementation, simulation performance and also to study the performance of the converter with source and load variations.

2. DESIGN OF ZCS INTERLEAVED BUCK CONVERTER

2.1 Buck Converter:

The output voltage of the Buck converter which is shown in Figure 1 is always less than the input voltage and is given by,

$$V_o = dV_s \quad (1)$$

Where $d = \frac{T_{on}}{T}$ is the duty cycle ratio, T_{on} is the on time of the semiconductor switch and T is the switching period. To ensure the continuous current mode of conduction the selected value of inductance should be greater than the critical value of the inductor L_c which acts as a boundary condition for continuous and discontinuous current mode of operations [3].

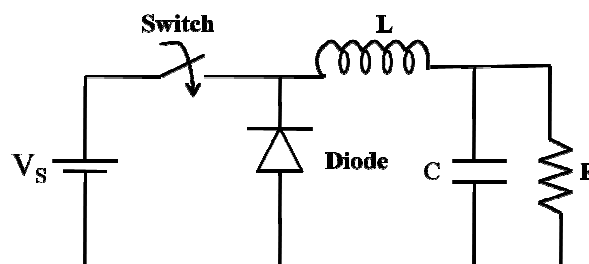


Figure 1. Schematic diagram of Buck converter

The buck converter comprises of an inductor L , a capacitor C , a semiconductor switch and a diode. The critical value of inductance is given by,

$$L_c = (1 - d) \frac{R}{2f_s} \quad (2)$$

The inductor value must be chosen by considering the fact that the magnitude of the ripple current in the output capacitor as well as the load current is determined by the appropriate inductor value. Hence, normally a ripple current of 10% to 20% of the average output current is assumed for the design to achieve good performance of the converter. The value of inductor is determined by,

$$\Delta I_L = \frac{V_S T d(1-d)}{L} \quad (3)$$

The capacitor value is determined by assuming the output voltage ripple as 1% to 2% of the output voltage. The capacitor value is determined by,

$$\Delta V = \Delta I_L * \frac{1}{8f_s C} \quad (4)$$

The following are the parameters considered for design: $V_S=48V$, $V_O=12V$, $f_s=50$ kHz, $L=2.16 \times 10^{-4}$ H, $C=1.736 \times 10^{-5}$ F and $R=1.44\Omega$

2.2. Zero Current Switching Buck Converter:

The switches of the zero current switching (ZCS) Buck converter turn on and off at zero current. The circuit shown in the Figure 2 consists of the inductor connected in series with the switch to achieve ZCS. This type of connection is called as L type connection which is advantageous than the other type of connection called the M type. In M type of connection an amount of energy is trapped in the inductor due to the recovery times of the practical devices. This results in the voltage transients across the switch. This condition favors the L type over M type.

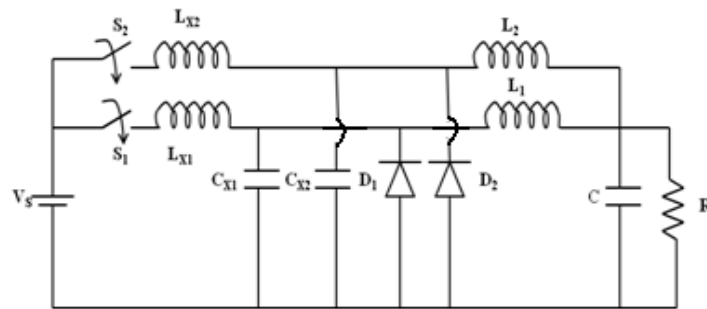


Figure 2. Schematic diagram of ZCS Interleaved Buck Converter

The ZCS Interleaved Buck Converter comprises of the resonant component inductors L_{X1} , L_{X2} and capacitors C_{X1} and C_{X2} , inductors L_1 and L_2 , a capacitor C , two semiconductor switches, two diodes D_1 and D_2 and a load resistor R .

The resonant components can be determined as follows:

The ratio between the peak resonant current and the load current is given by the following equation,

$$x = \frac{I_m}{I_o} = \frac{V_S}{I_o} \sqrt{\frac{C_x}{L_x}} \quad (5)$$

The value of inductor L_x and the capacitor C_x are determined by,

$$T = \frac{\pi V_S}{x I_o} C_x + \frac{2V_S}{I_o} C_x \quad (6)$$

and

$$L_x = \left(\frac{V_S}{x I_o} \right)^2 C_x \quad (7)$$

The following are the parameters considered for design: $L_{X1} = L_{X2} = 5.89\mu H$ and $C_{X1} = C_{X2} = 7.584\mu F$

3. MODELING OF ZCS INTERLEAVED BUCK CONVERTER

The ZCS interleaved buck converter is modeled using state space averaging technique in which the design is carried out in time domain based on their performance indices. Therefore the converter specifications are very well met. This method is highly significant for this kind of converters since the PWM converters are the special type of non linear systems which is switched in between two or more non linear circuits depending upon the duty ratio [4]. The unique feature of this method is that the design can be carried out for a class of inputs such as impulse, step or sinusoidal function in which the initial conditions are also incorporated. As a general case state space averaging method for two switched basic PWM converters is discussed now. The inductance currents and capacitance voltages are state variables and matrix form of equation is mentioned below,

$$\dot{X} = A_1x + B_1u \quad (8)$$

$$\dot{X} = A_2x + B_2u \quad (9)$$

where x is a state variable vector, u is a source vector, A_1, B_1, A_2, B_2 are the system matrices respectively.

The significance of state space averaging technique lies in replacing the above two sets of state equations by a single equivalent set described as follows,

$$\dot{X} = Ax + Bu \quad (10)$$

The A and B matrices are the weighted averages of actual matrices describing the switched system given by the following equations,

$$A \equiv dA_1 + (1 - d)A_2 \quad (11)$$

$$B \equiv dB_1 + (1 - d)B_2 \quad (12)$$

where d is the duty cycle ratio. Based on the above discussion, state model of Interleaved Boost converter is derived and is discussed now.

Mode of operation is assumed as continuous conduction since higher power densities are possible only with this mode of operation. During this mode D_1 and D_2 are always in complementary states with the switches S_1 and S_2 respectively that is when S_1 is on, D_1 is off and vice versa. Similarly when S_2 is on, D_2 is off and vice versa. Accordingly four modes of switching states are possible and the corresponding state equations are arrived as follows:

Mode 1: S_1 and S_2 are on

$$\dot{X} = A_1x + B_1V_S \quad (13)$$

$$x = \begin{bmatrix} i_1 \\ i_2 \\ i_{Lx1} \\ i_{Lx2} \\ V_{Cx1} \\ V_{Cx2} \\ V_C \end{bmatrix} \quad (14)$$

where i_1 and i_2 are currents flowing through the inductances L_1 and L_2 , i_{Lx1} and i_{Lx2} are the currents flowing through the resonant inductances L_{x1} and L_{x2} , V_{x1} and V_{x2} are the voltages across the resonant capacitances and V_C is the capacitance voltage respectively.

Mode 2: S_1 is on and S_2 is off

$$\dot{X} = A_2x + B_2V_S \quad (15)$$

Mode 3: S_1 is off and S_2 is on

$$\dot{X} = A_3x + B_3V_S \quad (16)$$

Mode 4: S_1 and S_2 are off

$$\dot{X} = A_4x + B_4V_S \quad (17)$$

where,

$$A_1 = \begin{bmatrix} 0 & 0 & 0 & 0 & \frac{1}{L_1} & 0 & \frac{-1}{L_1} \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{L_2} & \frac{-1}{L_2} \\ 0 & 0 & 0 & 0 & \frac{-1}{L_{x1}} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_{x2}} & 0 \\ \frac{-1}{C_{x1}} & 0 & \frac{1}{C_{x1}} & 0 & 0 & 0 & 0 \\ 0 & \frac{-1}{C_{x2}} & 0 & \frac{1}{C_{x2}} & 0 & 0 & 0 \\ \frac{1}{c} & \frac{1}{c} & 0 & 0 & 0 & 0 & \frac{-1}{RC} \end{bmatrix} \quad (18)$$

$$A_2 = \begin{bmatrix} 0 & 0 & 0 & 0 & \frac{1}{L_1} & 0 & \frac{-1}{L_1} \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_2} \\ 0 & 0 & 0 & 0 & \frac{-1}{L_{x1}} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{L_{x2}} & 0 \\ \frac{-1}{C_{x1}} & 0 & \frac{1}{C_{x1}} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{1}{c} & \frac{1}{c} & 0 & 0 & 0 & 0 & \frac{-1}{RC} \end{bmatrix} \quad (19)$$

$$A_3 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_{x1}} \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{L_2} & \frac{-1}{L_2} \\ 0 & 0 & 0 & 0 & \frac{-1}{L_{x1}} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_{x2}} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{-1}{C_{x2}} & 0 & \frac{1}{C_{x2}} & 0 & 0 & 0 \\ \frac{1}{c} & \frac{1}{c} & 0 & 0 & 0 & 0 & \frac{-1}{RC} \end{bmatrix} \quad (20)$$

$$A_4 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_1} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{L_{x1}} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_{x2}} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{1}{c} & \frac{1}{c} & 0 & 0 & 0 & 0 & \frac{-1}{RC} \end{bmatrix} \quad (21)$$

$$B_1 = B_2 = B_3 = B_4 = \begin{bmatrix} 0 \\ 0 \\ \frac{1}{L_{x1}} \\ \frac{1}{L_{x2}} \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (22)$$

The average state model takes the form described as follows:

$$\dot{X} = [A][X] + [B][U] \tag{23}$$

Where $[A] = A_1d_1 + A_2d_2 + A_3d_3 + A_4d_4$, $[B] = B_1d_1 + B_2d_2 + B_3d_3 + B_4d_4$, $[U] = V_S$ and the duty cycle ratio is given by $d_1 + d_2 + d_3 + d_4 = 1$. The output equation is defined as follows,

$$y = [0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 1] \begin{bmatrix} i_1 \\ i_2 \\ i_{Lx1} \\ i_{Lx2} \\ V_{Cx1} \\ V_{Cx2} \\ V_C \end{bmatrix} \tag{24}$$

4. CLOSED LOOP CONTROL SCHEME FOR DC-DC CONVERTER

The closed loop control system for the ZCS Interleaved Buck converter with PID controller feedback is shown in the Figure 3.

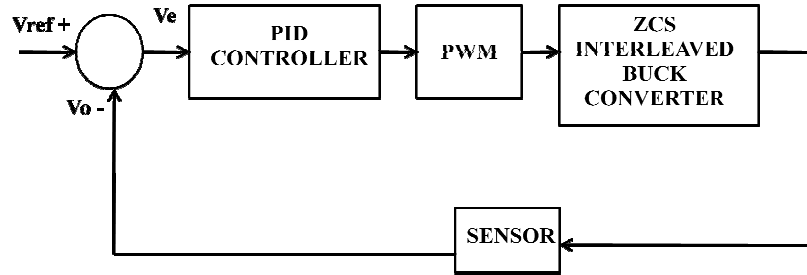


Figure 3. Functional Block diagram of closed loop control of dc-dc converter

The ultimate aim in designing the controller is to minimize the error between V_o and V_{ref} . As seen from the Figure 3, the important functional blocks that are evident are: PID Controller, PWM (Pulse Width Modulation) and dc-dc converter. The PID Controller acts as a compensator and generates the control signal by compensating the error signal (V_e). PWM block is for the generation of driver signal obtained from the compensator. The error (V_e) between the output voltage (V_o) and reference voltage (V_{ref}) is processed by the compensator block with PID Controller algorithm to generate control signal. The control signal significantly affects the converter characteristics and therefore effective tuning of the controller is one of the desired aspects of the control system. The fine tuned PID controller generates the duty cycle command corresponding to the error signal which is then converted as switching pulses using the PWM functional block.

5. DESIGN OF ROBUST PID CONTROLLER

The typical closed loop system using PID controller is shown in the Figure 3. The ideal continuous time PID controller can be expressed as,

$$u(t) = k_p \left[e(t) + \frac{1}{T_i} \int_0^t e(t) dt + T_d \frac{d}{dt} e(t) \right] \tag{25}$$

Where $u(t)$ is the control output, k_p is constant coefficient of the proportional gain, T_i is the integral time, T_d is the derivative time and $e(t)$ is the error between the V_{ref} and V_o . The transfer function corresponding to the PID controller is given as,

$$u(s) = \left[k_p + \frac{k_i}{s} + k_d s \right] e(s) \tag{26}$$

Where $k_p, k_i = \frac{k_p}{T_i}$ and $k_d = k_p T_d$ are the proportional, integral and derivative gains of the controller respectively [3]. K_p, T_i and T_d are calculated according to Ziegler – Nichols tuning rules. This method is an accurate heuristic method for determining good settings of PID controllers. This method is based on the empirical knowledge of the ultimate critical gain P_{cr} , which is given by $\frac{2\pi}{\omega}$, where ω is the natural frequency of oscillation of the converter under consideration. The Ziegler – Nichols tuning formulae is illustrated in the Table.1

Table 1. Ziegler – Nichols tuning rules for PID Controller design

Sl.No	Parameters	Formulae
1	Proportional gain(k_p)	$0.6 P_{cr}$
2	Integral Time (T_i)	$0.5 P_{cr}$
3	Derivative Time (T_d)	$0.125 P_{cr}$

P_{cr} value is obtained by the careful evaluation of the converter by assuming appropriate natural frequency of oscillation. The k_p value thus obtained is properly tuned in order that the system tracks the required step response. The main objective in tuning the controller is to choose the parameters in such a way that the control signal generates the accurate duty cycle command for the regulation of the dc-dc converter under consideration, irrespective of the source voltage or load disturbance. Hence it presents the faster dynamic response which is evident from the simulation results. The k_p, k_i and k_d values thus designed for the converter stages are shown in Table 2.

Table 2. Tuned Values for the Converter stages

Sl.No	Converter	k_p	k_i	k_d
1	Buck Converter	2.56	7873	2.08×10^{-4}
2	Interleaved Buck Converter	2.5	6801	1.7×10^{-5}
3	ZCS Interleaved Buck Converter	0.33	17.89×10^3	1.522×10^{-6}

6. SIMULATION RESULTS

The ZCS Interleaved Buck Converter with PID Controller is designed and simulated using MATLAB/Simulink. The design is carried out in time domain and hence the converter specifications such as rise time, settling time, peak overshoot and steady state error are achieved as per the Industrial standards and is illustrated in Table.3. The simulation has been carried out for variable voltage source and variable load not limiting to R load, which is illustrated in Table 4. The simulation results for the output current i_o , inductor currents i_1 and i_2 , output Voltage V_o with PID Controller for ordinary Buck converter, interleaved one and for zcs interleaved Buck converter are shown in Figure 3 (a), 3(b) and 3(c) respectively.

Table 3. Performance Parameters for the Converter Stages

Sl.No	Converters	Rise Time(s)	Settling Time(s)	Peak Overshoot(%)	Steady State Error(V)
1	Buck Converter	0.01	0.0125	0	0
2	Interleaved Buck converter	0.01	0.013	0	0.002
3	ZCS Interleaved Buck Converter	0.012	0.014	0	0.02

It is obviously understood from the simulation results that for the input transients of 44V-46V-48V, the output voltage of the Buck converter and interleaved one are maintained constant, which is considered as 12V. In Figure 3 (a), the output voltage settles down much faster and hence the dynamic performance of the converter is improved. No undershoots and overshoots are evident. The output voltage ripple is almost negligible. It is understood from Figure 3(b), the two inductors L_1 and L_2 share the current equally and hence good current sharing is being achieved which is one of the major advantages in designing the controller. The simulation results of ZCS Interleaved Buck converter shown in Figure 3(c) reveal the fact that the PID controller is the robust one in which the results are in concurrent with the mathematical calculations. The converter is designed in time domain and hence the converter specifications are very well met. In this case also the output voltage regulation is achieved for the same voltage transients with much lesser settling time

and there is no overshoot or undershoot. The current sharing among the inductors is maintained in this converter stage also.

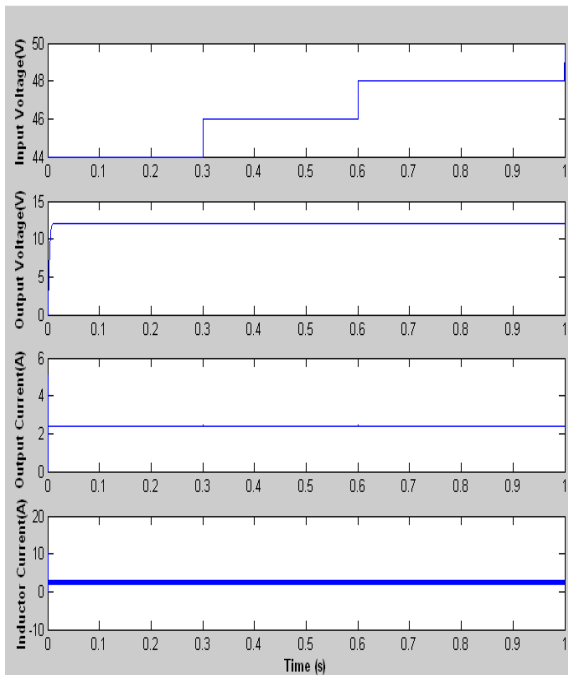


Figure3 (a) Simulation results for Buck converter

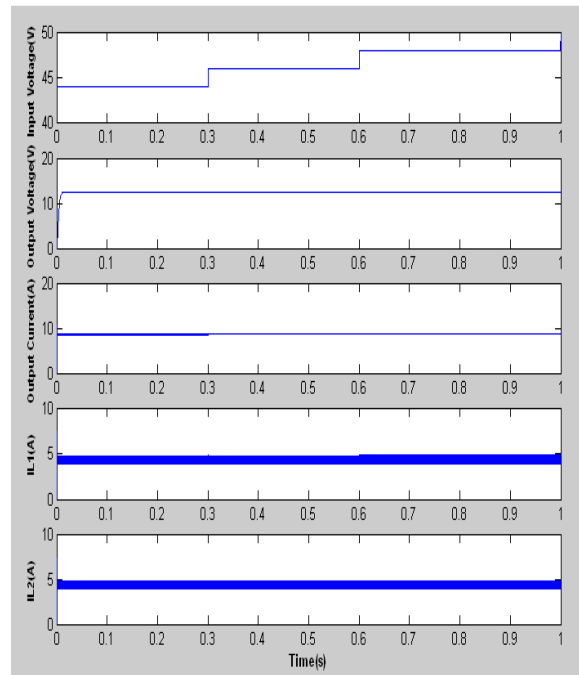


Figure 3 (b) Simulation results for Interleaved Buck Converter. (I_{L1} – Inductor Current1, I_{L2} – Inductor current 2)

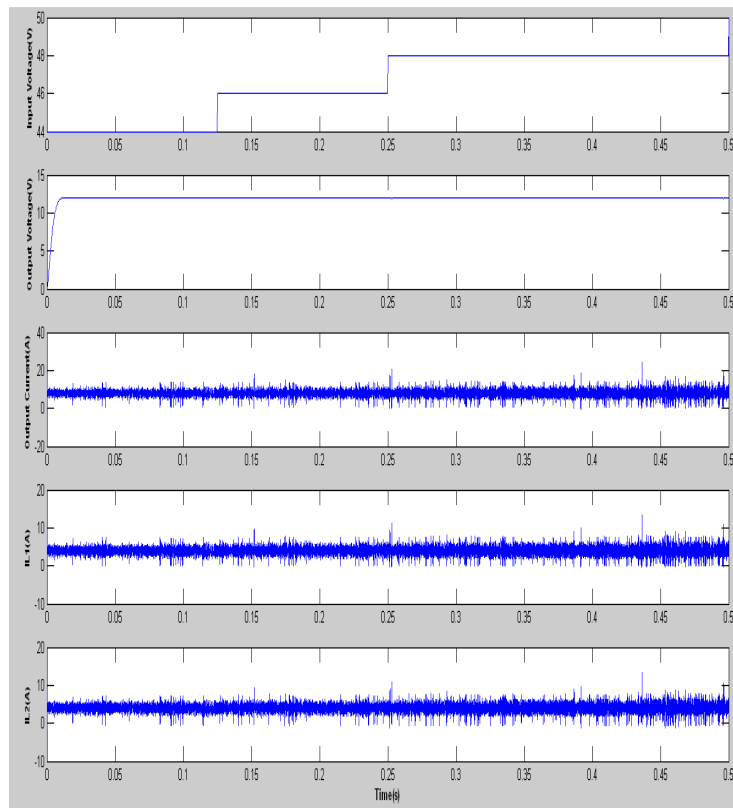


Figure 3(c). Simulation results for ZCS Interleaved Buck Converter

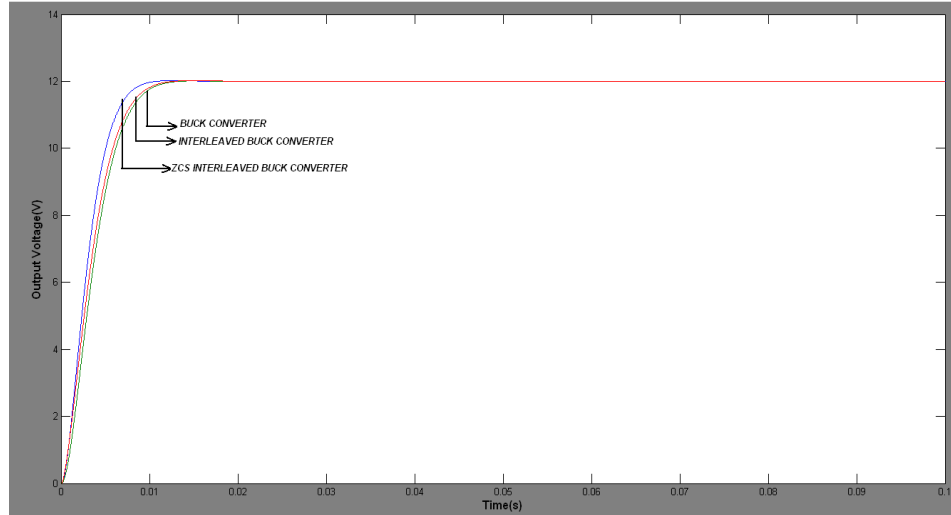


Figure 4. Output Voltage Comparison for the three stages

The output current contains some ripple which is evident from Figure 3(c) that needs some improvement. Figure 4 shows the output voltage comparison between the three stages. It is understood that all the three waveforms start from zero and attain their steady state for both Input and Output transients. The Buck converter waveform settles a few milli seconds earlier when compared with the other two stages. In all the three stages of converter the dynamic performance has been improved which shows that the controller thus designed is simple, robust, easy to design and implement and highly efficient.

Table 4. Output Voltage for Load Variations

SLNo	R(Ω)	L(H)	E(V)	Reference Voltage(V)	Output Voltage (V)		
					Buck Converter	Interleaved Buck Converter	ZCS Interleaved Buck Converter
1	1.44	-	-	12	12	11.99	12.01
2	2	-	-	12	12	11.99	12.03
3	5	-	-	12	12	12	12.01
4	1.44	10×10^{-6}	-	12	12	11.99	12.01
5	2	100×10^{-6}	-	12	12	12.02	12.01
5	5	100×10^{-6}	5	12	12	12.09	12.03

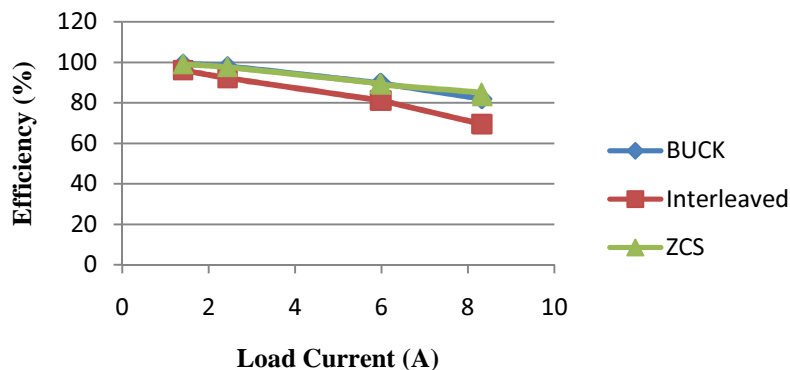


Figure 5. Comparison of Efficiencies

The efficiency of the ordinary Buck Converter, Interleaved Buck converter and ZCS Interleaved Buck Converters are determined and are shown against the load current in Figure 5. The efficiency of the

interleaved state is slightly lesser than the ordinary Buck converter where as the efficiency of the Interleaved converter with zero current switching is much improved. It is almost same and even high at some load currents when compared with the ordinary Buck converter stage. The highest efficiency is obtained as 98% with a load resistance of 1.44Ω.

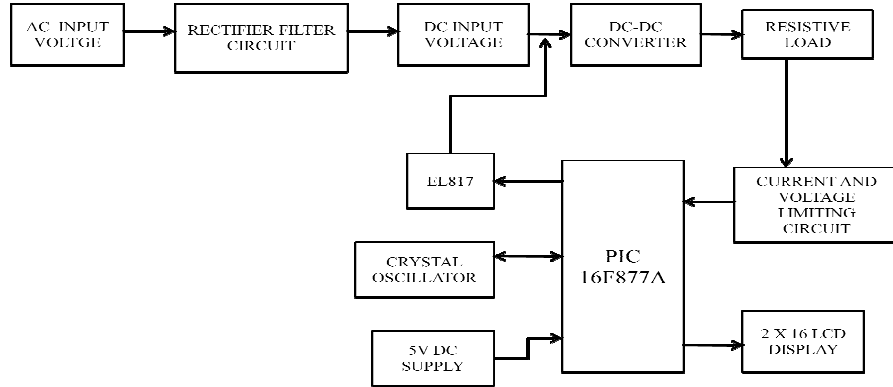


Figure 6. Block Diagram for the Hardware set up

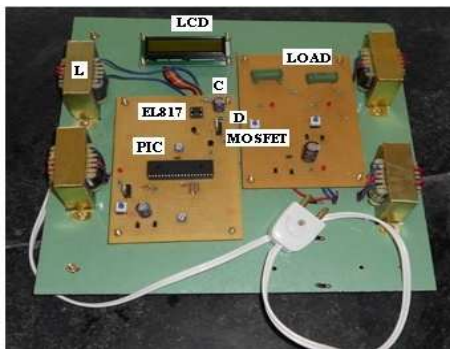


Figure 7. Prototype model of the dc-dc converter



Figure 8(a) Output Voltage Measured using Multimeter



Figure 8(b). Output Measured with Oscilloscope (Scale: y-axis: 1 div and 10Volts/div)

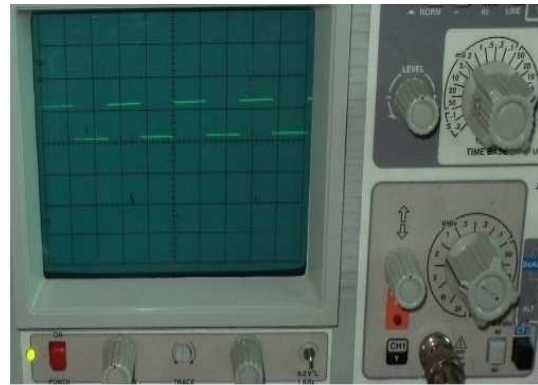


Figure 8(c). Gate Pulse (Scale: x-axis:2.5divX20μs/div = 20kHz)

7. HARDWARE RESULTS

The experimental setup for closed loop control of the Buck converter is implemented using PIC microcontroller (PIC16F877A). The PIC microcontroller is used to implement the controller platform and programming is done using the software micro C. The PIC microcontroller is able to automatically generate

the required duty cycle in order that the system tracks the desired set value. The Hardware set up consists of the Power supply circuit, dc-dc converter, PIC microcontroller, crystal oscillator, optocoupler, 2X16 liquid crystal display, current and voltage limiting circuits. The experimental set up is carried out using the following values:

$$L = 10\text{mH}, C = 100\mu\text{F}, R = 1\text{k}\Omega, V_S = 18\text{V}, V_{\text{ref}} = 10\text{V}, \text{MOSFET} - \text{P55NF06}, \text{DIODE} - \text{1N4007}$$

The Block diagram of the entire set up is shown in Figure 6. Here the 230V ac supply is stepped down and is converted in to 18V dc supply which is given to the converter. The load used is the resistive load across which the output voltage is to be regulated. Optocoupler (EL814) is used to isolate the high voltage side from low voltage side. The PID controller parameters thus designed are programmed using micro C language and implemented through the PIC16F877A microcontroller. The PIC16F877A microcontroller has special features such as High performance RISC CPU with an operating speed of 20MHz and 200ns instruction cycle, flash memory of 14.3kB, programmable code and power saving code protection, 10 bit, 8 channel A/D converter, 33 I/O pins, and 5 I/O ports with self reprogrammable features. The prototype model is shown in Figure 7. The output voltage measured across the load is shown in Figure 8 (a) and Figure 8 (b) respectively.

The output thus shown settles down faster in the range of ms and controller works effectively thereby tracking the reference voltage. The steady state error is observed which needs further improvement. The waveform thus observed in the oscilloscope shows no evidence of overshoots or undershoots. The simplified version of the program codes are written to implement the PID controller. In order that the PID loop should be speeded up the multiply routines are limited to 8x8 signed multiply routine with a 16 bit signed result [10].

8. CONCLUSION

A closed loop control system has been designed for the ZCS Interleaved Buck converter in continuous time domain using robust PID controller. The simulation results thus obtained using MATLAB/Simulink is in concurrence with the mathematical calculations. The controller thus designed for the Buck converter is implemented using PIC16F877A as a control platform and the results are illustrated. The mathematical analysis, simulation study and the experimental study show that the controller thus designed achieves tight output voltage regulation and good dynamic performances and higher efficiency. The soft switching thus implemented reduces the switching stress and losses and hence leading to highest efficiency of 98% with the load value as 1.44Ω. The controller enables good current sharing among the parallel connected Buck converters. This method is topology independent and also can be extended for any of the applications such as power factor preregulation, photovoltaic cell and speed control applications. The prototype developed using microcontroller is more suitable for portable electronic systems and more effective and easy to be implemented.

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