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A High Regulated Low Ripple DC Power Supply Based on LC Filter and IGBT

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ABSTRACT

Filaments operating at a high temperature region would require ripple free current constant power source for their heating purposes. Introduction of ripple in the power supply would result in high power loss, aberrant, unpredictable temperature rise etc. High current ripple can also extenuate the life of electrolytic capacitors used in the circuit. In this paper we propose a scheme in which we would not only use simple, low cost, easily available electronic components but also reduce the value of ripple factor to <0.1% and load regulation to 0.1%.

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1. INTRODUCTION

Advances in fast-switching insulated-gate bipolar transistor (IGBT) technology and cost-effective, high-speed control processors have significantly matured constant current voltage power source technology. There is also currently an increasing demand for high current, low ripple highly regulated controlled power supplies for the heating purposes in high temperature filaments. To meet these requirements has been a challenge in the design of filament power supplies, considering non-ideal characteristics of the devices, perturbations in the power source, and variations in the load. As the research in high-energy physics progresses and as the particle accelerators find more new applications in industrial and medical areas, better regulated filament power supplies are in constant demand.

This paper presents a new scheme to design a high current constant dc power supply. The system uses elements from analog electronics for controlling purposes. We mainly employ the property of IGBT that change in the Gate to emitter voltage can alter the current through it in the linear region of its operation. The controller circuit is designed such that by sensing the change in the output voltage it will generate sufficient amount of gate-to-emitter voltage which will change the current through it, thus changing the load voltage. This process continues until the load voltage has reached to the desired value. Some fluctuations will be present load voltage but these fluctuations are not comparable to the load voltage, i.e. ripple factor is very small. Also for any sudden change in load the output voltage does not fluctuate too much from the set value, i.e. regulation is also small.

2. RESEARCH METHOD

circuit topology and principle

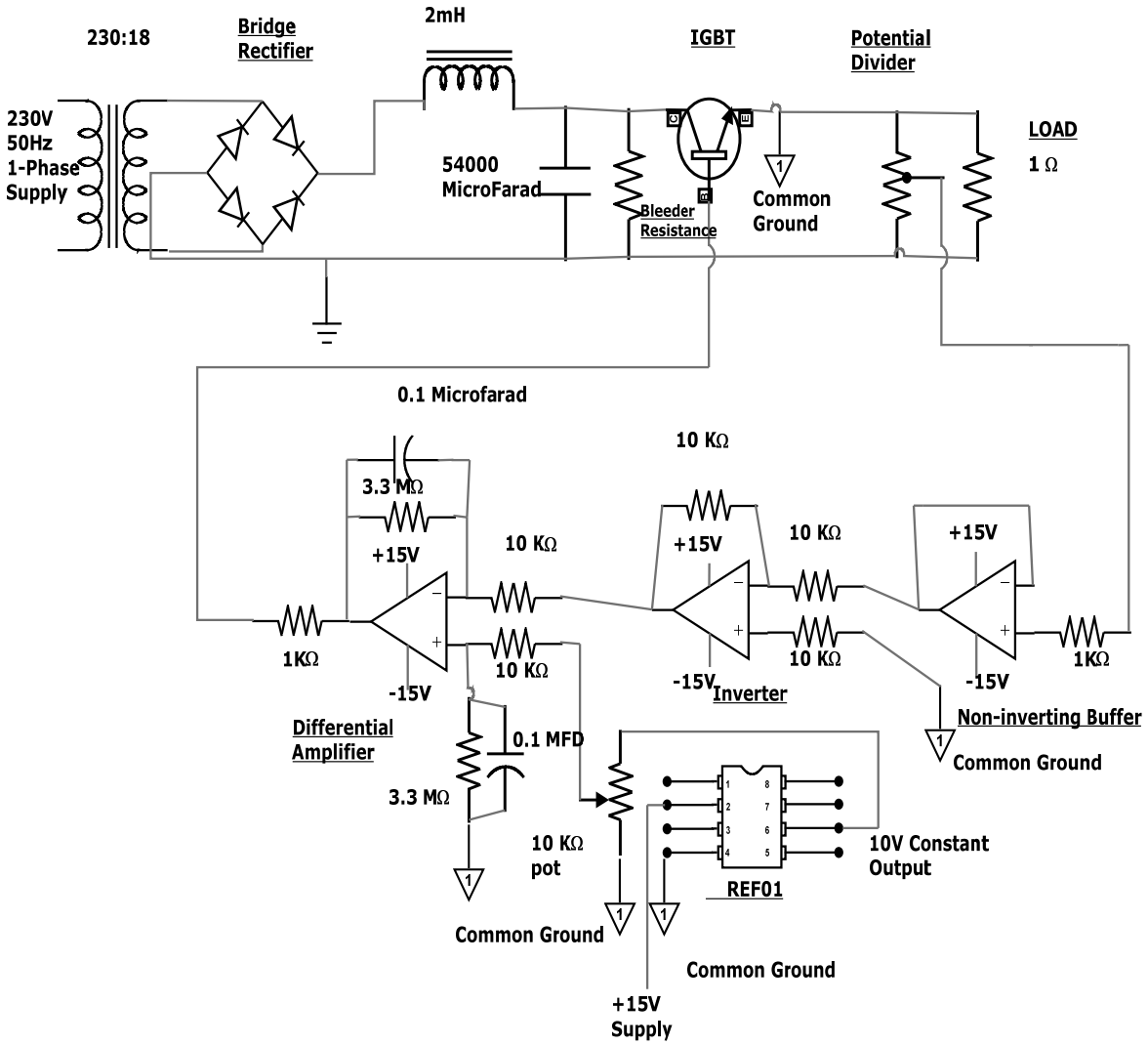

Figure 1. Circuit topology and principle

The circuit topology of the proposed filament power supply scheme is shown above. The circuit consists of a diode converter, L-type LC filter, bleeder resistance, IGBT, potential divider, a non-inverting buffer, inverter, a differential amplifier & REF01.

For our experimentation purpose a 180VA, 230V/18V transformer is used to produce an output of 10V, 10A. An excess of 8V is taken into design consideration to compensate for the forward voltage drop in rectifier & IGBT. Full wave rectifier Bridge is used to rectify the AC output of the transformer to a DC voltage. A L type LC filter is used to reduce harmonics in the output waveform of the rectifier. A bleeder resistance is also provided to supply a path for the capacitor of the filter to discharge when power supply is turned off. G4PH50UD IGBT is used for the purpose of keeping the output voltage constant. Two 10k resistors, connected in series, are connected in parallel with the load & voltage feedback is taken from the middle point.

In the voltage controller circuit, the buffer is used to avoid loading effects. Since we are taking the feedback voltage with respect to the high potential point of the load, the feedback voltage will be negative w.r.t the ground of the load circuit. So we require this inverter to have the output voltage positive w.r.t the voltage of the emitter of the IGBT, so that the IGBT can be fired The inverted output of the previous stage is

fed to the inverting terminal of the op amp and reference voltage is fed to the non-inverting terminal of the op amp by a pot. By changing the output of the pot we can change the voltage across of the load.

If we fix the pot voltage at certain level the load voltage will remain at a certain level and the rest part of the circuit will try to keep this voltage constant as far as possible with change in load current. For this purpose the pot require a fixed voltage source. Here we are using REF01 chip as a constant voltage generator which will generate 10V DC when we supply +12V to it. Reference input is fed in to the voltage controller by using a stable 10V source REF01 chip. Using a 10K resistor in series with a pot the input is varied and as the non-inverting input changes the output varies accordingly. Between the output of the pot and the ground a parallel combination of resistor and a capacitor is used. This helps in reduction of fluctuation of the pot output, thus stabilizes the voltage across the load.

Higher value of resistors are used to avoid following of higher current through the controller circuit, otherwise it will load the primary load circuit and unexpected result will be obtained. A capacitor of 0.1 mF is connected across the inverting and output terminal of the op amp to reduce the oscillation of the output.

Filter Design

For an inductor filter, the ripple factor increases as the load resistance increases. For the capacitor filter on the other hand the ripple factor decreases with the increase of load resistance. If these two filters are combined as in an L-type LC filter, the ripple factor should not depend on load resistance (RL).

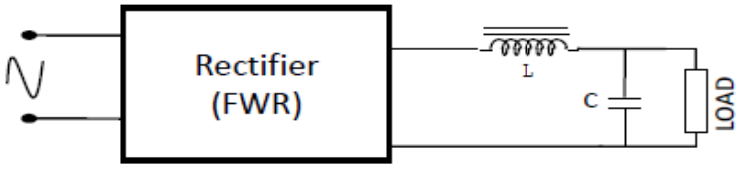

Figure 2. L-type LC filter

If an LC filter is connected to an output of a full-wave rectifier, the output of the filter as follows:

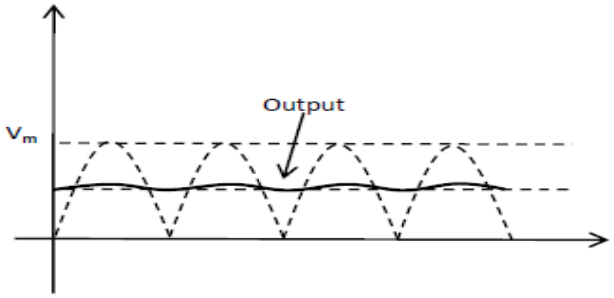

Figure 3. The output of the L-type LC filter

For a small value of L, the capacitor C will be charged to the peak voltage V_m to cut off the diodes. The diode current will then flow in short pulses. As L increases, the current pulses are smoothened out to flow for longer times with diminished amplitudes.

As L exceeds a critical inductance LC, one diode or the other always conducts. Thus input voltage v and input current I are full-wave rectified sine-waves. Hence with an inductance greater than the critical value, the input voltage v to the filter can be approximated by

$$v = \frac{2Vm}{\pi} - \frac{4Vm}{3\pi} cos2\omega t.$$

If the inductor is perfect having no dc resistance, the dc output voltage is $V_{dc} = \frac{2V_m}{\pi}$.

A. Regulation:

In practise, the inductor is imperfect. If R is the total resistance of one-half of the transformer secondary, the diode and the inductor in series, the dc output voltage across the load will be $V_{dc} = \frac{2V_m}{\pi} - I_{dc}R$
The percentage regulation is $\frac{V_{NL}-V_{FL}}{V_{FL}}.100 = \frac{R}{R_L}.100$

B. Ripple factor

The ripple current flowing through L does not give appreciable ripple voltage across R_L provided the reactance X_C of C at the ripple frequency is much less than R_L.
So, for an LC Filter,

$X_C << R_L$ and $X_L >> X_C$

at the angular frequency 2ω. Here, $X_L=2\omega L$ is the reactance of L at 2ω. Therefore, the ac component of the current through the L is mainly determined by X_L, so that R.M.S. ripple current is

$$I'_{rms} = \frac{\sqrt{2}V_{dc}}{3X_L}$$

where $V_{dc} = 2V_m/\pi$
The output ripple voltage produced by I'rms flowing through the C, is
$V'rms = I'_{rmsXC} = (\sqrt{2}\, X_c)/(2X_L)\, V_{dc}$
The ripple factor is :

$$\gamma = \frac{V'_{rms}}{V_{dc}} = \frac{\sqrt{2}X_c}{3X_L} = \frac{\sqrt{2}}{12\omega^2 LC}$$

Thus γ is independent of R_L, as expected.

C. Critical Inductance

If L is larger than its critical value LC, as assumed in our analysis, the current I does not drop to zero. The current I has a dc component $I_{dc}=V_{dc}/R_L$ and a sinusoidal ac component of peak value $(4V_m)/(3\pi X_L)$. Hence, I_{dc} must exceed the negative peak value of the ac component, i.e.

$\frac{V_{dc}}{R_L} \geqslant \frac{4V_m}{3\pi X_L}$ or, $\frac{2V_m}{\pi R_L} \geq \frac{4V_m}{3\pi X_L}$

Or, $X_L \geq \frac{2R_L}{3}$ L=L_C & as we know X_L=2ωL

$$\boldsymbol{L_C = \frac{R_L}{3\omega}}, \textit{ at line frequency of 50Hz} \boldsymbol{L_C = \frac{R_L}{300\pi} = \frac{R_L}{950}}$$

For our experimentation, V_{dc}=10V and I_{dc}=10A

We know, $V_{dc}=\frac{2V_m}{\pi}$.
So, $V_m = \frac{\pi}{2}$, V_{dc}=15.708V
So, $V_{R.M.S.}=V_m/\sqrt{2}$=11.1 V
Load resistance $R_L = V_{dc} / I_{dc}$ =1Ω

It is discussed that $L_C = \frac{R_L}{3\omega}$. From this L_C (critical inductance) comes out to be 1.06mH. We choose L=2mH.
An estimation of the value of capacitor can be made from this condition $X_C << R_L$. From this equation value of C_{min} = 1.6mF. So we should choose capacitor of value greater than C_{min} .From the expression of ripple factor, we know,

$$\gamma = \frac{\sqrt{2}}{12\omega^2 LC}$$

Choosing ripple factor, we can get the value of capacitor required.

Table 1. The value of capacitor required

Ripple Factor	Capacitor required
5%	11.9mF
2%	29.8mF
1%	59.7mF

We choose capacitor of 54 mF & the ripple caused by this 1.1% which can be further improved as a voltage regulator is employed.
So, we have chosen the value of the inductor to be 2mH and a bleeder resistance of value 1kΩ.

- Operation of the IGBT

The turning on of the device is achieved by increasing the gate voltage V_{GE} so that it is greater than the threshold voltage V_{th}. This results in an inversion layer forming under the gate which provides a channel linking the source to the drift region of the device. Electrons are then injected from the source into the drift region while at the same time junction J_3, which is forward biased, injects holes into the n- doped drift region. This injection causes conductivity modulation of the drift region where both the electron and hole densities are several orders of magnitude higher than the original n- doping. It is this conductivity modulation which gives the IGBT its low on-state voltage because of the reduced resistance of the drift region. Some of the injected holes will recombine in the drift region, while others will cross the region via drift and diffusion and will reach the junction with the p-type region where they will be collected. The operation of the IGBT can therefore be considered like a wide-base p-n-p transistor whose base drive current is supplied by the MOSFET current through the channel.

Calculation of the system behaviour

a. Transfer Function

Let the feedback voltage to the buffer is V_F (w.r.t the ground of the controller supply). The output of the buffer will be then V_1=V_F. Next one is an inverting amplifier. So its output will be V_2= - V_1.

The next op-amp is working as a differential amplifier. In its non-inverting input is the reference is fed. Let the reference voltage be V_C w.r.t. the ground of the voltage controller ground. Considering V_2 be its inverting terminal input, the output will be,

$$Vo=(1+\frac{Zf}{R1})\ Vc-(\frac{Zf}{R1})V2;$$

On simplification we get,

$$Vo= (1+\frac{Zf}{R1})Vc+(\frac{Zf}{R1})Vf;$$

$$Or,\ Vo= (1+\frac{Zf}{R1})Vc+(\frac{Zf}{R1})Vf;$$

Here the for feedback purpose we take half of the load voltage. Now since the ground of power supply of the voltage controller is connected to the emitter of the IGBT so the ground is at V_L potential. So V_F= V_L/2- V_L.
So,

$$Vo= (1+\frac{Zf}{R1})Vc-(\frac{Zf}{R1})(\frac{Vl}{2}-Vl);$$

$$Or,\ Vo=(1+\frac{Zf}{R1})Vc-(\frac{Zf}{R1})\frac{Vl}{2};$$

Now the voltage V_0 is with respect to the emitter. So this voltage can be considered as the voltage between the Gate and Emitter terminal of the IGBT, responsible for the firing of the IGBT.
So,

$$V_{GE}=Vo=(1+\frac{Zf}{R1})Vc-(\frac{Zf}{R1})\frac{Vl}{2};$$

Now this voltage will determine to what extent the IGBT will be forward biased i.e. its resistance. The parameter trans-conductance gives us the ratio of the collector current and gate to emitter voltage.
So we can also write $I_L=G_{fe}.V_{GE}$;
[where G_{fe} is the trans conductance of the IGBT]
Now since the load resistance is 1 Ω,so the load voltage

$V_L=I_L$ x 1Ω
Or, $V_L[1+G_{fe}(Z_f/2R_1)]=V_c.G_{fe}.(1+Z_f/R_1)$;

[where Z_F is the feedback path impedance]

Or, $\frac{Vl}{Vc}=\frac{Gfe(1+\frac{Zf}{R1})}{1+Gfe(\frac{Zf}{2R1})}$;

Taking Laplace Transformation,

$$\frac{Vl(s)}{Vc(s)}=\frac{Gfe(1+\frac{\frac{R2}{sC2}}{R1(R2+\frac{1}{sC2})})}{1+Gfe(\frac{\frac{R2}{sC2}}{2R1(R2+\frac{1}{sC2})})};$$

Or, $\frac{Vl(s)}{Vc(s)}=\frac{Gfe(1+\frac{R2}{R1(sC2.R2+1)})}{1+Gfe(\frac{R2}{2R1(sC2.R2+1)})}$;

Or, $\frac{Vl(s)}{Vc(s)}=\frac{[s+\frac{R1+R2}{R1.R2.C2}]}{[s+\frac{2R1+Gfe.R2}{2R1.R2.C2}]}$;

$\frac{Vl(s)}{Vc(s)}=\frac{K*(s+a)}{(s+b)}$

is the required transfer function of the voltage controller circuit.
where k=G_{fe}; a=$\frac{R1+R2}{R1.R2.C2}$; b=$\frac{2R1+Gfe.R2}{2R1.R2.C2}$;

b. Estimation of Output for given Input:

We have already obtained, $\frac{Vl(s)}{Vc(s)}=\frac{[s+\frac{R1+R2}{R1.R2.C2}]}{[s+\frac{2R1+Gfe.R2}{2R1.R2.C2}]}$;

Or, $V_L(s)=\frac{[s+\frac{R1+R2}{R1.R2.C2}]}{[s+\frac{2R1+Gfe.R2}{2R1.R2.C2}]}V_C\ (s)$

Now considering a step Input $V_C(s)=V_C/s$, we get

$V_L(s)=\frac{[s+\frac{R1+R2}{R1.R2.C2}]}{[s+\frac{2R1+Gfe.R2}{2R1.R2.C2}]}\frac{V_C}{s}$

Putting the values R_1=10KΩ; R_2=3.3MΩ; C=0.1μF and applying Final Value Theorem, we get

$$v_L(t)=\lim_{s\to 0}\left(\frac{\left[s+\frac{R1+R2}{R1.R2.C2}\right]}{\left[s+\frac{2R1+Gfe.R2}{2R1.R2.C2}\right]}.\frac{1}{s}\right)V_C$$

or,$v_L(t)=2V_C$

So, the output voltage i.e. the voltage across the load will be 2 times that of the ref setting, i.e. the relationship between input-output should be linear.

c. Estimation of Rise Time:

By definition, rise time is the time required for the response to rise from 10% to 90% of its steady value. So, we can estimate the rise time theoretically by applying a step change in the ref input and can calculate the rise time. Theoretically calculated rise time should be close enough to the practical value; exact match is not expected as there is mismatch between the value we assumed and practical value of the circuit components.

Now considering a step Input $V_C(s) = V_C/s$;

$$V_L(s) = \frac{K(s+a)}{s(s+b)}.V_C;$$

$$V_L(s) = K[\frac{1}{s+b} + \frac{a}{s(s+b)}]V_C;$$

$$V_L(s) = K.V_C[\frac{a}{b.s} + (1-\frac{a}{b})(\frac{1}{s+b})];$$

$$V_L(t) = K.V_C[\frac{a}{b} + (1-\frac{a}{b})\, e^{-bt}] * u(t);$$

where u(t)=1 for t>=0;u(t)=0 elsewhere.

Rearranging the expression we get

$$V_L - \frac{K.a}{b}Vc = K.Vc.\frac{b-a}{b}.e^{-bt};$$

$$t = \frac{1}{b}\ln\left(\frac{K(b-a)Vc}{b.Vl - K.a.Vc}\right);$$

In our case R_1=10KΩ; R_2=3.3MΩ; C=0.1μF;
Now by taking G_{fe}=30;
We get K=30; a=836.36; b= 12503;
Now for input voltage V_C=4.962V,
Load Voltage of V_L=9.97V;

$$\text{We get } t=(\frac{1}{12503})\ln\left(\frac{30(12503-836.36)4.962}{12503x9.97-30x836.36x4.962}\right);$$

$t = 7.46 \times 10^{-4}$ sec; t=746.07 μs.

Since by definition, rise time is the interval for the response to rise from 10% to 90% of its steady value so we can estimate the rise time to be 596.856 μs.

EXPERIMENTAL RESULTS

- Variation of Output w.r.t Input:

Table 2. Variation of Output w.r.t Input

Reference input through pot (volts)	Load Voltage (volts)	Theoretically obtained Load Voltage (volts)
0.0	0	0.0
0.502	0.980	1.04
1.003	2.000	2.006
1.500	3.014	3.0
2.002	4.037	4.004
2.501	5.055	5.002
3.007	6.085	6.014
3.501	7.09	7.002
4.005	8.12	8.01
4.503	9.14	9.006
4.927	10.0	9.854

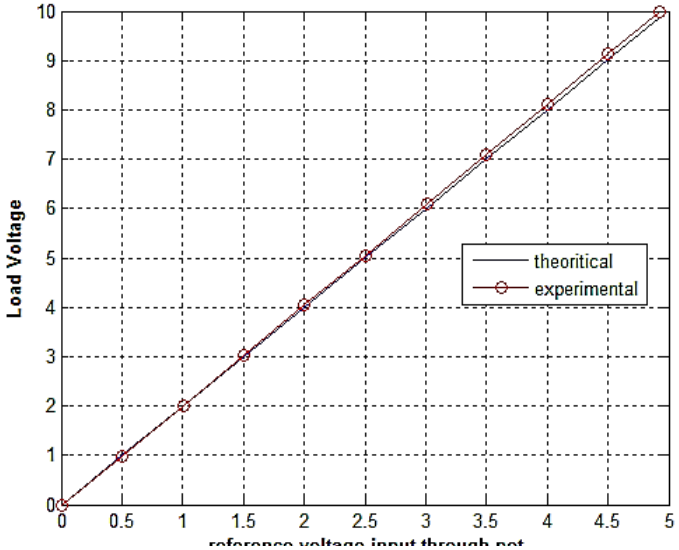

Figure 4. The variation of output voltage across the load

The variation of output voltage across the load is quite linear with the variation of the input

➢ ***Rise time:***

By using a switch at the ref input we suddenly switch on the ref input to its maximum setting. This operation can be treated as step change in input and the output obtained will be the step response of the system. The plot gives us the step response of the system. CH1(yellow) is the output & CH3(purple) is the ref input

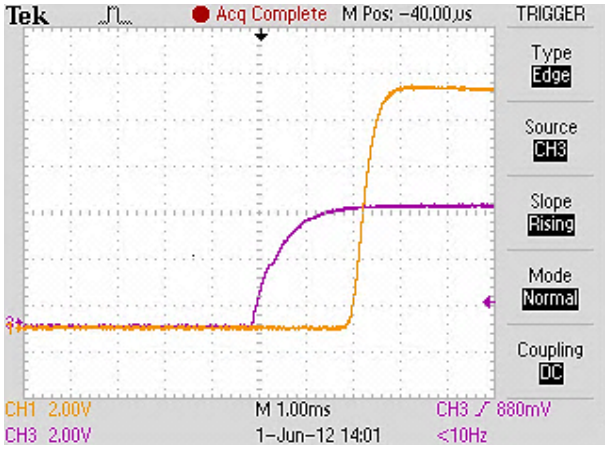

Figure 5. Rise time

There is a significant amount of delay between the input and output. This is the loop delay is caused due to the all form of capacitances (actual & stray) in the circuit. Proper wiring and using more linear circuit component can reduce this delay.

Here the Channel 1 is the connected across the load. The oscilloscope reported a rise time of 608 µs. our calculated value was 596.856 µs, close enough to the practical value.

➢ Load Regulation:

For a reference input of 4.94V the output voltage across load is 10.016V in full load condition. Now using a switch we disconnect the load from the circuit and the voltage across the feedback resistors is 10.02V i.e. no load voltage at that ref setting is 10.05V.

So, the regulation at full load comes out to be,

$(V_{NL}-V_{FL})/V_{FL}.100\%=$

$((10.02-10.016)/10.016)x100\%=0.109\%$

Voltage regulation is quite good. There is no appreciable change in the output voltage at maximum ref setting from no load to full load condition, which is a necessary condition for voltage regulator.

➢ Line Regulation:

Line regulation is the capability to maintain a constant output voltage level on the output channel of a power supply despite changes to the input voltage level. In our case, the nominal supply voltage is 230V AC.

Table 3. Line regulation

Input voltage to the transformer (V)	%of nominal voltage	Voltage across Load (V)
200	-13%	10.01
210	-8.7%	10.01
230(nominal value)	0	10.01
250	8.7%	10.02
260	13%	10.02

The line regulation is within (10.02-10.01)/10.01 x 100% = 0.1%

➢ Response Time

Under full value of output voltage of 10V we have checked the response time. In our case, the system turns out to be little more sluggish than normal electronics circuit.CH3 (yellow) corresponds to the output wave form & CH1 (purple) corresponds to the input ref voltage waveform.

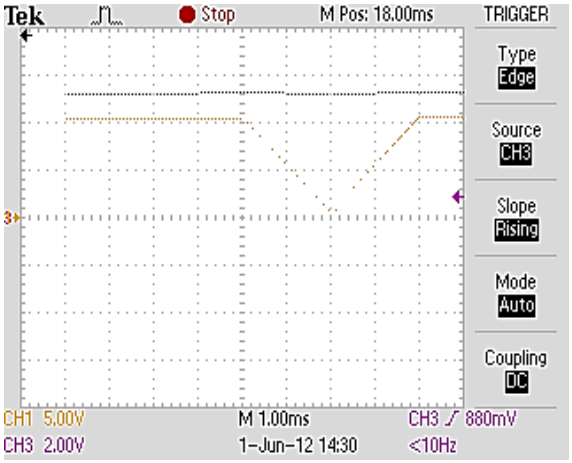

Figure 6. Response time at no load

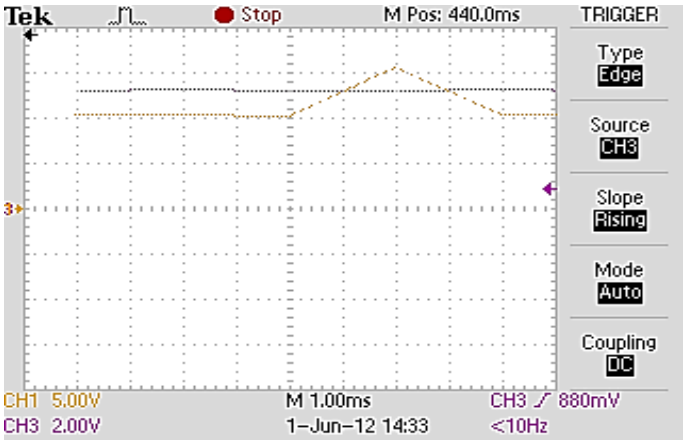

Figure 7. Response time at full load

➢ Ripple Factor

CH3 (yellow) corresponds to the output wave form & CH1 (purple) corresponds to the input ref voltage waveform. The ripple is calculated at full value of the reference input.

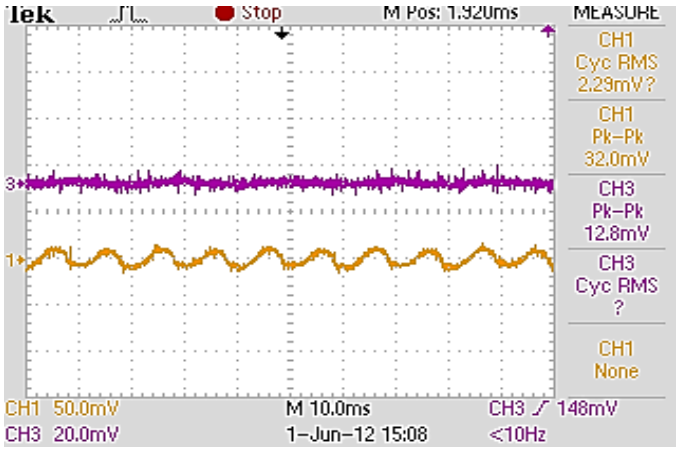

Figure 8. Ripple Factor at full load

Ripple =12.8mV$_{pk-pk}$ =7.8mV$_{R.M.S}$

Ripple factor=$\gamma=\frac{Vrrms}{Vdc}=\frac{7.8*10^{-3}}{10.03}$x100%=0.077%

OBSERVATION

It can be observed that during transition from no load to full load there is a dip in the output voltage. This can be explained as since at no load there is small current through the IGBT, the capacitor is discharging at slower rate. Now if we suddenly switch on the load then suddenly full load current will start flowing through the circuit causing the voltage across the capacitor to drop. This will decrease the voltage across the load which will change the feedback voltage and the voltage regulator will take necessary measures to increase the load voltage back to its previous value.The reverse case happens during the transition from full load to no load.

3. CONCLUSION

The 0.1µF capacitor & 3.3MΩ resistors are connected to the non-inverting terminal of the differential op-amp to match the impedance in the feedback path. The identical impedance in both input

terminals helps in the greater noise cancellation from the output due to subtractive property of the differential amplifier.

It's also noticeable that there is a significant decrease in the ripple factor from theoretical calculation due to due to fast controlling action of the controller circuit. The rise time is also quite low to ensure fast dynamic response.

Also it's observed that increasing the gain of the differential stage up to a certain optimum level actually increases the linearity of the input output response as the base signal of the IGBT is also amplified. Further increase in the gain would result in non-linearity due to saturation of the amplifier.

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