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Modular Multilevel Converters Part-I: A Review on Topologies, Modulation, Modeling and Control Schemes

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ABSTRACT

This article is devoted to the Multi-level inverters review and in particular to the form and function of modular multilevel inverters (MMI), with their different topologies, modulation, modeling and control schemes Detailed analysis with their functions of MMI has been made in comprehensive manner with existing literature available till date. All existing methods are compared in detail with proposal for the best methods available. The article has made strategic conclusions on MMI to make the system more robust in operation with less complexity in design and control.

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1. INTRODUCTION

Many investigations in the field of modular multi-level inverters have led to successful operation in HVDC systems. In recent times, in the power transmission era, for very long distances, high voltage DC (HVDC) transmission lines based on current source inverters (CSI) and voltage source inverters (VSI) are found to be offering more economic and cost effective power transmission. But, recently HVDC transmission systems based on VSI have received increasing attention due to many opportunities like the grid access of weak AC networks, independent control of active and reactive power, supply of passive networks and black start capability, high dynamic performance and small space requirements.

In particular, the novel power converter topology for MMI (Modular Multi level Inverter) has been intensively researched, developed, and valuated against many features like high modularity, simple scalability, low expense of filters, robust control, simple in design and redundancy. This converter is composed by identical power cells connected in series, each one built up with standard components, enabling the connection to high voltage poles. Although the MMI and derived topologies offer several advantages, simultaneously they also introduce a more complex design of the power circuit and control goals, which have been the main reason for the recent and ongoing research. Furthermore, Medium Voltage Converters are an interesting area for the application of MMIs. This paper is organized in four sections. Section-1 introduces the MLI, reveals different topologies applied to MLI and discusses their basic advantages. Section -2 discusses the different modulation scheme and their comparison. Section-3 shall discuss the different control techniques and Section-4 deals about the modeling and finally conclusion with recommendations are provided.

1.1. Modular Multilevel Inverter (MMI)

- It requires an isolated DC source as an input supply.
- Benefits of multilevel inverters are obtained without compromising of quality of multi-level waveform.
- Modular realization, easily scalable to different power and voltage level.

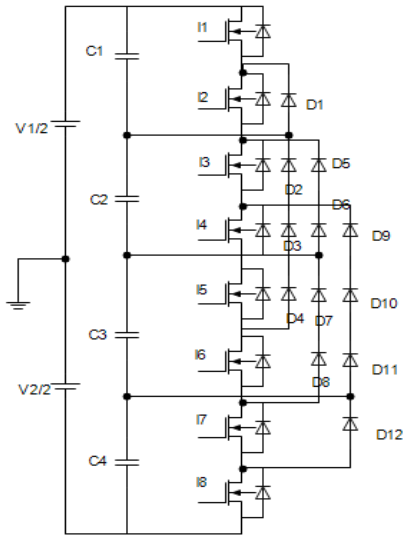

Figure 1. Five Level diode clamped multi-level inverter

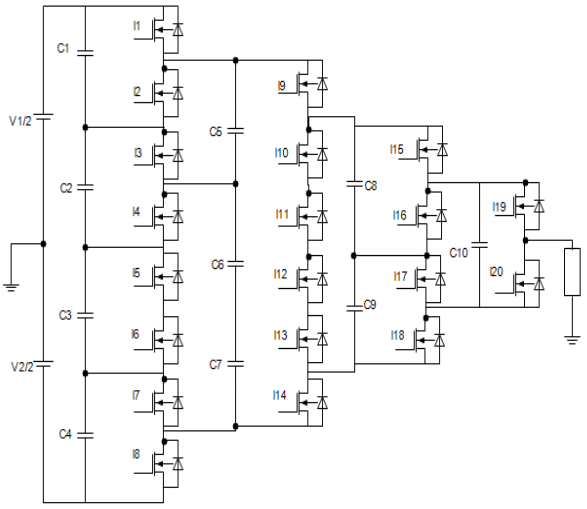

Figure 2. Five Levels generalized multi-level inverter

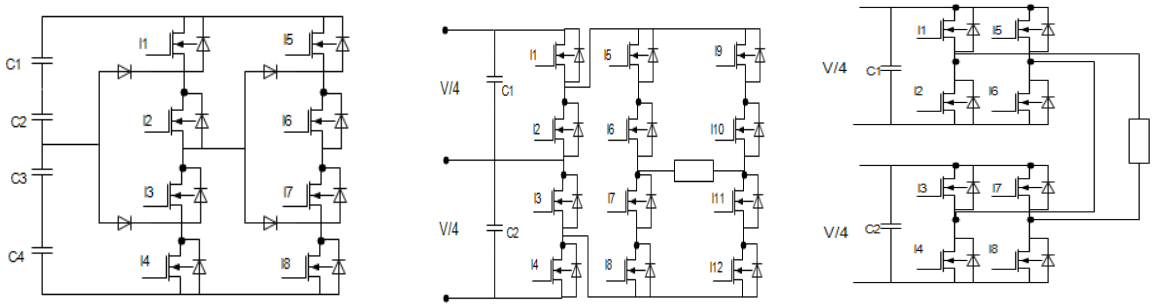

Figure 3(a), (b),(c). Five level Multi level clamped MLI, Reverse voltage MLI, cascaded MLI

- Faulty cells can be easily bypassed.
- The internal arm currents are not chopped.
- Protection chokes (L_{arm}) are inserted into the system. They do not disturb the operating voltage of the semiconductor, since the currents are not chopped.
- The sub modules are two terminal devices. There is no need to supply the DC side capacitor with energy.
- Voltage balancing is not critical.
- Switching cells both control the DC side and AC side.
- Low switching losses.
- No bulk capacitors needed.
- Low switching frequency, high quality output, reduced voltage steps in the switches.
- Modular realization, easily scalable to different levels.

- Redundancy can be easily achieved by using more scales than required, faulty cells can be easily bypassed.
- Internal arm currents are not chopped.

Based on existing literature and after careful review, sub-division can be done as follows:

- Single star bridge cells (SSBC)
- Single delta bridge cells (SDBC)
- Double star chopper cells(DSCC)
- Double star bridge cells(DSBC)
- Double star hexagonal cells(DSHC)

In this article it considered and reviewed about the five level inverter. In Figure 1, it shows about the Five Level diode clamped multi-level inverter (NPCMLI), Figure 2 shows about the topology of generalized multi-level inverter(GMLI), In Figure 3 Figure 3(a), (b), (c) it shows Multi level clamped MLI (CCMLI), Reverse voltage MLI(RVMLI), cascaded MLI respectively(CMLI).The basic differences between multilevel clamped MLI (MCMLI) and all other MLI, which are cited in above Figures are shown in table1.A new transformer less four-leg topology is suggested for shunt compensation [1]. In "Accelerated Model of Modular Multilevel Converters in PSCAD/EMTDC" [2] and in "High-Power Modular Multilevel Converters With SiC JFETs" [3], the possibility of building a MLI using silicon carbide (SiC) switches has been studied. In "Active Redundant Sub-module Configuration in Modular Multilevel Converters" [4], the MLI is based on the cascaded connection of identical sub modules (SMs) enabling additional redundancies. In the papers "Active Redundant Sub-module Configuration in Modular Multilevel Converters" and "The Multilevel Modular DC Converter" [4, 5], the configuration of the MMC topology with redundant SMs is proposed and the effects of active redundancies is demonstrated. In the IEEE Transaction paper on Industrial electronics "Hybrid Electric Vehicle Power Management Solutions Based on Isolated and Non-isolated Configurations of Multilevel Modular Capacitor-Clamped Converter" [6], it is mentioned that the MLI has become an increasingly important topology in medium- and high-voltage applications. In [7] the various configurations of a multilevel modular capacitor-clamped converter (MMCCC) are presented, and it also reveals many useful and new formations of the original MMCCC for transferring power in either an isolated or no isolated manner. In [8] it proposes a novel topology of a multilevel modular capacitor-clamped dc-dc converter. [9] provides the idea of voltage balancing of the capacitors of different sub-modules comprising the converter. In [10], it proposes a modulation strategy for the MLI which provides the voltage balancing of the capacitors of different sub modules comprising the converter. In [11-15] it states that HVDC transmission systems are becoming increasingly popular when compared to conventional ac transmission. HVDC VSCs can offer advantages over traditional HVDC current source converter topologies, and as such, it is expected that HVDC VSCs will be further exploited with the growth of HVDC transmission. In [16-20], the modular multilevel cascade converter (MMCC) family based on cascade connection of multiple bidirectional chopper cells or single-phase full-bridge cells are discussed. In [21-25], a discussion on new ac/ac modular multilevel topology for connecting two three-phase systems is provided. The operating principle is explained, and characteristic waveforms are given. In [26-30], it is clearly mentioned that an onshore horizontal axis wind turbine, generator and converter are usually in the nacelle on the top of the tower, while the grid step-up transformer is placed at the bottom. Also, a new ac/ac modular multilevel converter (M^2LC) family is expected to be introduced. The new concept stands out due to its modularity and superior control characteristics. Multilevel voltage-source converter topologies are widely used today in high-power applications such as medium-voltage drives. On the other hand, studies on matrix converters (MCs) have been mainly limited to the low power range. A modular multilevel cascade inverter based on double-star bridge-cells (MMCI-DSBC) is expected to be one of the next-generation medium-voltage PWM inverters intended for grid connections [31-35].

Table 1. Basic comparison of inverter with their number of requirements

Topologies	M I	GMCSI	RVMLI	GMLI	CMCI	CCMLI	NPCMLI
Sources	2	1	3 ($\frac{m-1}{2}$)	3 ($\frac{m(m+1)}{2}$ -1)	$\frac{3m-1}{2}$	3(m-1)	3(m-1)
Diodes	12(m-1)	6 ($\frac{m-1}{2}$)	3(3(m-1))	6 ($\frac{m(m+1)}{2}$ -1)	6(m-1)	6(m-1)	6(m-1)
Switches	12(m-1)	6 ($\frac{m-1}{2}$)	3(3(m-1))	6 ($\frac{m(m+1)}{2}$ -1)	6(m-1)	6(m-1)	6(m-1)
Clamp diodes	0	0	0	0	0	0	3(m-1)(m-2)
Clamp cap	0	0	0	0	0	$\frac{3(m-1)(m-2)}{2}$	0
Inductors	2	$\frac{m-3}{2}(\frac{m-3}{2}+1)$	0	0	0	0	0
Transformer	0	0	3	0	0	0	0

The main advantages of coupled inductors will lead to the smaller size & lighter weight. The basic operation and the requirements of the inductors are:

- These inductors are necessary to handle the voltage difference between top and bottom side of the converter.
- These inductors can limit the fault current in case of the faults if any arises.

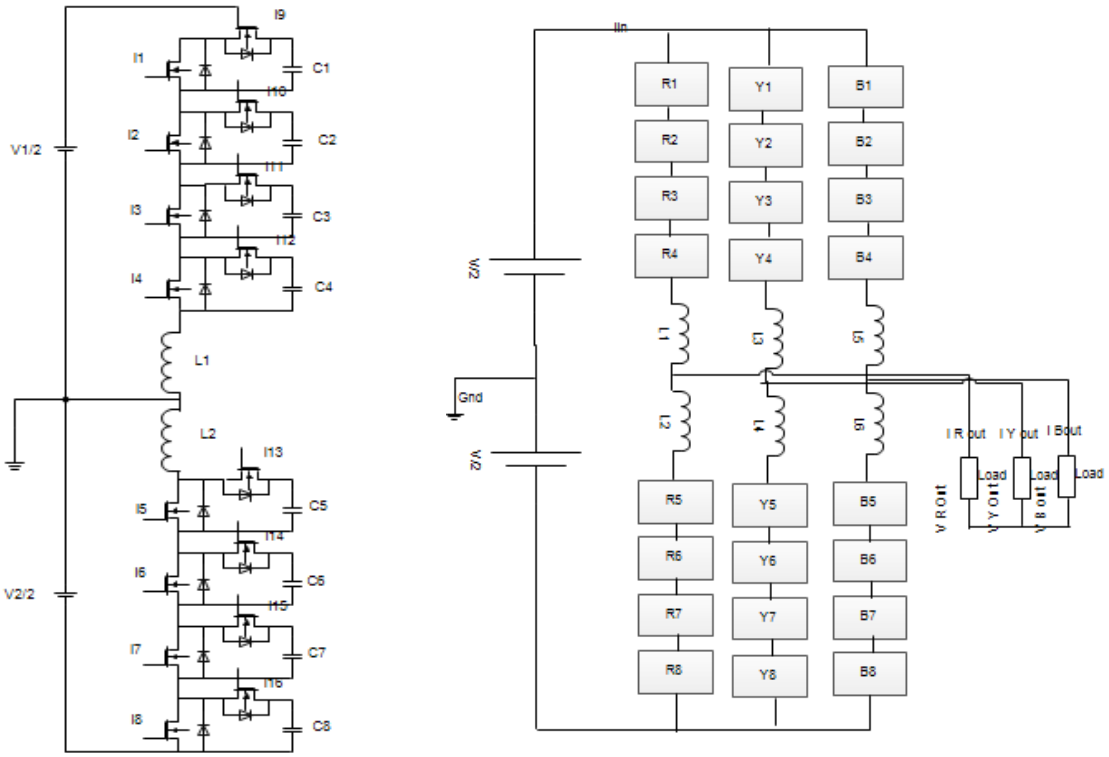

Figure 4. Five Level Modular MLI with chopper cells and details of its three phase system

2. MODELLING OF A MODULAR MULTI-LEVEL INVERTER

Modular multi-level inverter for a single phase out of three phases have shown in Figure 4. By applying basic KCL and KVL in Figure 4.

$$it_r = i_{cir} + \frac{i_r}{2} \tag{1}$$

$$i_{br} = i_{cir} - \frac{i_r}{2} \tag{2}$$

$$i_{cir} = \frac{1}{2}\,(i_{tr} + i_{br}) \tag{3}$$

$$i_{cir} = \overline{i_{cir}} + \widetilde{i_{cir}} \tag{4}$$

Whereas, it_r is the current passing through 'R' phase top limb, ib_r is the current passing through 'R' phase bottom limb, i_{cir} is the circulating current passing in 'R' phase between top and bottom of the limb. 'n' indicates number of limbs connected in MLI [36-40]. This circulating current is the unique feature of this topology. This current consists of both DC & AC component, where the DC(i_0) component is

$$\overline{i_{cir}} = \frac{i_0}{3} \tag{5}$$

For the phase 'R', which is shown in above, if we apply Kirchhoff's law for both the upper to lower,

$$V_{tr}= \frac{Vdc}{2} - \sum_{n=1}^{N} Vntr - L_{top}. \frac{d_{itr}}{dt} - R_{top} . i_{tr} \quad (6)$$

$$V_{br}= - \frac{Vdc}{2} + \sum_{n=N+1}^{2N} Vnbr + L_{bot}. \frac{d_{ilr}}{dt} + R_{bot} . i_{br} \quad (7)$$

Whereas, Vt_r is the voltage across 'R' phase top limb and neutral, Vb_r is the voltage across 'R' phase bottom limb and neutral, L_{top} and L_{bot} are the arm inductors in 'R' phase top and bottom of the limb. By applying equations (1) and (2) in equations (6) and (7), we have the total voltage V_{Rphase} is (6) + (7),

$$V_{Rphase} = ½ [\sum_{n=N+1}^{2N} Vnbr - \sum_{n=1}^{N} Vntr] - L_{top+bot}. \frac{d_{ir}}{dt} - R_{top+bot} . i_r \quad (8)$$

By this it clearly shows that the output voltage depends upon the current 'i_r' and difference of voltage injected by the cells. From equation (8), as long as the $L_{top+bot}$ (L_{tot}) presents in the circuit, Then the losses will be there and the voltage output will always vary.Where as $R_{top+bot}$ represents as R_{tot}.
The circulating current can be expressed as:

$$L_{tot} . \frac{d_{icir}}{dt} + R_{tot} . i_{cir} = \frac{V_{dc}}{2} - \frac{[\sum_{n=N+1}^{2N} Vntr - \sum_{n=1}^{N} Vlnr]}{2} = \frac{V_{cir}}{2} \quad (9)$$

Here, $L_{tot} . \frac{d_{icir}}{dt} + R_{tot} . i_{cir}$ is voltage drop of one limb that can be referred to as difference of lower and upper arm.
Many conclusions can be made out of above equation (9).

- The arm voltage drop is equal to the difference of source voltage and sum of voltages of upper and lower modules [41-45].
- The i_{cir} depend upon the DC bus voltage and sum of cell voltages. Consequently, by adding or subtracting the same voltage amount from both arms will not affect to the AC side output voltage; but will affect circulating current [46-50].

$$V_{tr} = \sum_{n=1}^{N} Vntr = \frac{V_{dc}}{2} - V_{tr} + \sum \frac{V_{tr}}{2} \quad (10)$$

$$V_{lr} = \sum_{n=N+1}^{2N} Vnbr = \frac{V_{dc}}{2} + V_{br} + \sum \frac{V_{tr}}{2} \quad (11)$$

2.1 Modulation Strategies

There are mainly two methods of modulation strategies

- Zero voltage applied to the arm inductors (ZV).
- Voltage applied to the arm inductors (VA).

1) In this strategy (ZV), the voltage provided by the upper and lower inductors is zero i.e. $V_{tr} = V_{lr}$. So, the voltage levels provided by them are 0 or $\frac{V_{DC}}{N}$, hence the number of levels obtained by them is N+1. The number of inserted cells is constant.

2) In this strategy (VA), upper and lower cells have different voltage levels V_{tr} and V_{br}, to generate different voltage across the limbs. This leads to higher number of voltage levels in the output voltage which is equal to 2N+1. Here the number of inserted cells is not constant, which is equal to N+1, N, N-1respectively. In this method, the circulating current can be controlled. But due to presence of circulating currents, higher ripples will be present and to reduce the ripple content, a large number of inductors are required.

Table 2. Sub module Operation.

S_{main}	$S_{auxilairy}$	V_{out}	Current	Power Path	Cap Status
ON	OFF	0	$i_0 > 0$	I_1	Unchanged
ON	OFF	0	$i_0 < 0$	Dm_1	Unchanged
OFF	ON	V_{dc}	$i_0 > 0$	I_9	Discharging
OFF	ON	V_{dc}	$i_0 < 0$	D_{x1}	Charging

For N- level inverter, voltage across each capacitor - $\frac{V_{dc}}{n-1}$. Number of capacitor required is $6N-6$ and there is no requirement of clamping diodes and also the switching devices are double. Each voltage is obtained by turning ON four switches, out of which two switches belong to the top and the other two switches belong to the bottom.

Table 3. Switching Sequence of five level MMI

	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8
$\frac{1}{2}V_{dc}$	1	1	0	0	0	0	1	1
0	1	0	1	0	0	1	0	1
0	0	1	1	0	1	0	0	1
0	0	1	0	1	1	0	1	0
0	1	0	0	1	0	1	1	0
$-\frac{1}{2}V_{dc}$	0	0	1	1	1	1	0	0

For modular multilevel converters,
M = $^{2A_m}/_{(n-1)A_c}$ $m_f = \frac{f_c}{f_m}$, where f_m,A_m & f_c, A_c frequency and amplitude of carrier and modulating waves, which is shown in Figure 5.

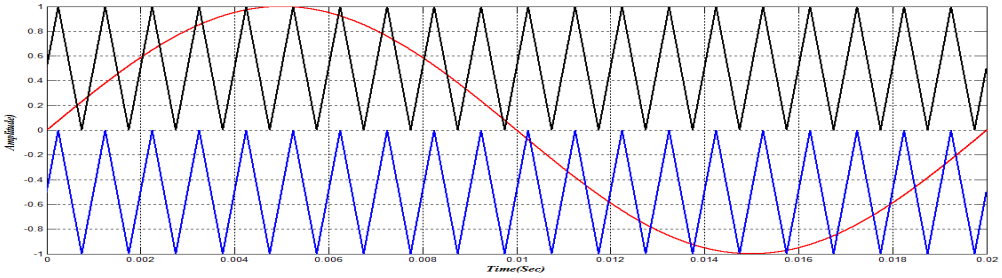

Figure 5. Sinusoidal Pulse width modulation technique.

As shown in Figure 4, it has main switch and diode as I_1 and D_{m1} respectively and has the auxiliary switch and diode as I_9 and D_{x1} respectively. The detailed capacitor charging and discharging status has been shown in table 2. The switching status of a five level MMI is shown in table 3 nine level modular multilevel inverter is shown in table 4.

Table 4. Switching Sequence of nine level MMI

	s_1	s_2	s_3	s_4	s_5	s_6	s_7	s_8	x_1	x_2	x_3	x_4	x_5	x_6	x_7	x_8
$\frac{Vdc}{2}$	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1
$-\frac{Vdc}{2}$	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0

The number of $\frac{1}{4}V_{dc}$ will be 16 and the number of $-\frac{1}{4}V_{dc}$ will be 16, so the total number of switching states for positive and negative $\frac{1}{4}V_{dc}$ is 32 states where as in the redundant states, the power paths of a sub module as follows
For 1 0 1 0 state when i_a >0 , the conduction state S_{m1} D_{x2} & C_2 and Sx_4, Da_3 &C_4 and for i_a <0 the conduction state S_{x2} D_{a1} & C_2 and Sa_3, Da_4 C_4.

3. CONTROLLING OF A MODULAR MULTI-LEVEL INVERTER

One important problem associated with modular multilevel converter is circulating current issues at balanced load condition and unbalanced load condition. Here, mainly two types of conditions are considered:

- Under balanced condition, only positive sequence of current will flow in the buffer inductor or arm inductor.
- Under unbalanced condition, all positive, negative and zero sequence of current will flow in the buffer inductor or arm inductor.

In order to control the respective components, in literature [30-42] it considers Dual vector current controller. [16, 17, 18] estimated this by using arm inductance and stored capacitance. In this case, it was concluded that as the arm inductance increases, the circulating current will decrease, but if we increase the value of inductance, the cost and space requirement will increase. So, there is need to control the circulating current instead of increased inductance. In [19] it proposes that under balanced conditions, negative sequence component of circulating current in each arm rotates at double the line frequency. So, Δ(delta) control method was stated which states that by transforming the a-c-b sequence with a double line frequency into d-q sequence at rotational reference frame. But this method was not able to eliminate the circulating current totally at underbalanced conditions. In [26] it proposed a control method with analyses of instantaneous power of each leg, and also an algorithm to reduce the circulating currents and d-c link voltages ripples; but has a disadvantage of inclusion of double line frequency ripple. In [40], it has proposed a-b-c reference frame to control the circulating currents but has the disadvantage of generating a delay and it cannot improve the transient response occurring in the inner balancing currents. In [44] it proposed a model predictive control which took ac-side current, circulating currents and sub-module voltage balancing, by detecting the switch status to minimize the cost function. But, this study [20-23] analyses each phase's instantaneous power to reduce the active power ripple, when negative sequence component was generated. This instantaneous power begins with the positive, negative and zero sequence components with double frequencies and dc components. But the disadvantage of this method is the use of a complicated PIR notch filter used to control each component separately.

3.1 Inner Current Suppression of a MMC

Due to presence of the capacitor in sub-modules, the peak value of the current is increased compared to theoretical values.

$$V_{top} + V_{bot} + L_{tot}.\frac{d_{ir}}{dt} + L_{tot}.\frac{d_{iL}}{dt} = V_{dc} \quad (12)$$

$$I_{top} = i_{cir} + \frac{i_{load}}{2} \quad (13)$$

$$I_{bot} = i_{cir} - \frac{i_{load}}{2} \quad (14)$$

$$V_{load\_ref} = \frac{V_{dc}}{2} M \cdot \cos(\omega_0 t) \quad (15)$$

$$L.\frac{d_{ir}}{dt} + L.\frac{d_{iL}}{dt} = L\frac{d}{dt}(i_r + i_L) = 0 \quad (16)$$

$$V_{an} = \frac{V_{dc}}{2} - V_{top} = V_{bot} - \frac{V_{dc}}{2} \quad (17)$$

$$V_{r\_ref} = \frac{V_{dc}}{2}(1 - M\cos(\omega t)) \quad (18)$$

$$V_{L\_ref} = \frac{V_{dc}}{2}(1 + M\cos(\omega t)) \quad (19)$$

Each Sub modules consists of both AC and DC components of voltages.

$$V_r = \overline{V_{tr}} + \widetilde{V_{tr}} \quad (20)$$

$$V_r = \overline{V_L} + \widetilde{V_L} \quad (21)$$

The voltage across each inductor is:

$$L.\frac{d_{ir}}{dt} + L.\frac{d_{iL}}{dt} = 2L.\frac{d_{icir}}{dt} = V_{dc} - (\overline{V_{top}} + \widetilde{V_{bot}} + \overline{V_L} + \widetilde{V_L}) \quad (22)$$

In steady state,

$$i_{cir} = I_{dc} + \sum_{k=2,4,6} ik\ cos\ (k\omega ot + \varphi ic) \quad (23)$$

$$P_{active} = V_{dc}.\ i_{cir} \quad (24)$$

$$i_{cir} = \frac{\text{Pactive}}{\text{Vdc}} = \frac{Rload.(V\varphi load/(Rn+\omega loadn))}{Vdc} \quad (25)$$

$$i_u = i_{cir} + \frac{i_{load}}{2} = 1.50 + 4.33\ \sin\ (100\prod t - 8.19°) \quad (26)$$

$$i_L = i_{cir} - \frac{i_{load}}{2} = 1.50 - 4.33\ \sin\ (100\prod t - 8.19°) \quad (27)$$

$$i_{u\_rms} = i_{L\_rms} = \sqrt{icir\ square + square\ of\ \frac{il}{\Omega}/2} \quad (28)$$

The capacitor voltage and inductor currents under balanced condition's as shown in fig6 and 7 respectively.

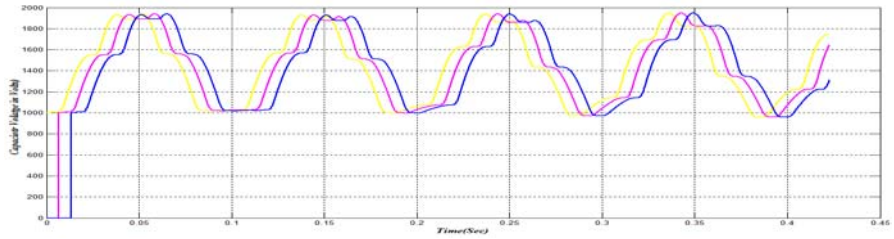

Figure 6. Capacitor currents is a five level MMI by using Sinusoidal Pulse width modulation technique

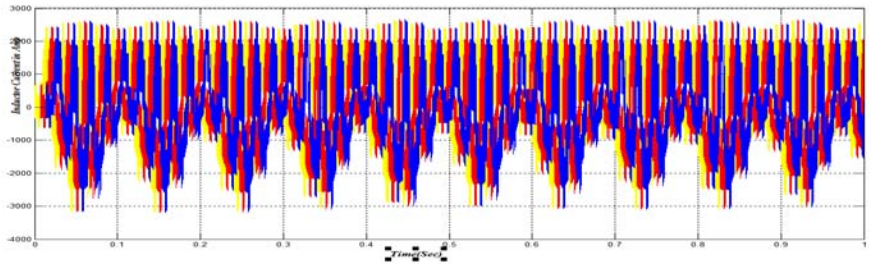

Figure 7. Inductor currents is a five level MMI by using Sinusoidal Pulse width modulation technique

3.2. Circulating Current Suppression Method

Due to unbalance in the upper and lower arm of the MMI, circulating currents will develop. These even harmonics and circulating currents can be suppressed by:

$$\text{Re } h(s) = \frac{K_h.\ S}{s^2+(k\omega_0)^2} \qquad (h = 2, 4, 6\ldots\ldots) \quad (29)$$

$$H(s) = \frac{i_{cir(s)}}{i_{cirr.f\ (s)}} = \frac{2Ls\ (\sum_{h=2,4,6\ldots} \frac{K_h.S}{s^2+h(\omega 0)^2})}{1+2Ls\ (\sum_{h=2,4,6\ldots} \frac{K_h.S}{s^2+(h\omega 0)^2})} \quad (30)$$

But i_{cir} will consist of the DC components also.

$$H_c(j_o) = \frac{2Lj\omega\left(\sum_{h=2,4} \frac{-jK_h.\omega}{-\omega^2+(h\omega 0)^2}\right)}{1-2Lj\omega\left(\sum_{h=2,4} \frac{-jK_h.\omega}{-\omega^2+(h\omega 0)^2}\right)} \quad (31)$$

By considering the upper arm, the output voltage of the upper arm is:
$V_{top} = V_{dc}/4$, which lies in between : $k_1 * V_{top} < V_{top} < (k_1+1)\ V_{top}$; where k_1 is a positive integer, Kh is a proportional constant. In order to produce a voltage 'V_r' at a certain time, k_1 sub-modules capacitors will be insufficient and if we consider (k_1+1), sub-module capacitors then it will generate over voltage. Hence, k_1 module is taken as I_r to provide major part, and (k_1+1) is taken as O_μ for the remaining part.

$$k_1 = \int \frac{V_r}{V_{rtop}} = \int \frac{V_r}{(\frac{V_{dc}}{N})} \quad (32)$$

Then the reference voltage can be calculated as:

$$V_{r\_ref} = V_r - k_1 . \frac{V_{dc}}{N} \quad (33)$$

3.3. Capacitor Voltage Balancing Method

In order to control the voltage balancing of the sub module capacitor there are mainly two ways

- Virtual loop mapping
- Selective virtual loop mapping

These two methods are based on the comparison of the capacitor voltage .In this method it shall use a counter up counter method to control the mapping relations which will be equal to or less than the carrier frequency. The range of counter is 0-(Counter-1) [34-37].

The above method is applicable only when the system is operated at well balanced conditions. But the system will not be balance in practical due to variation in circulating currents, modulation singles. So, the accuracy of the method is applicable here. One more method is proposed in the literature [44-63], where there is a need to sort the capacitor voltages frequently due to which more time will be consumed and this also requires more number of hardware components and it will become complex at higher voltage levels.
Instead, if once pick the maximum and minimum values of capacitor voltages and their corresponding directions.

3.4. Synchronous Sampling Control and its Effect

In order to minimize the delay of PWM signal, a synchronous sampling control is used. Here [47-53], it has been considered with a continuous model instead of discrete model, due to the following advantages:

- Discrete model do not allow an analytical approach to model the converter and design the control system.
- Numerical solutions of sub-module with higher number of switching require considerable time.

Considering 'N' sub-modules per arm, M is modulation index.
If M = 0, then all modules in the arms are bypassed; and if M=1, then all the sub-modules are inserted.

$$\text{Ideal capacitance of the arm, } C^{arm} = C/N \quad (34)$$

$$\text{Effective arm capacitance, } C^{eff(m)} = C^{arm}/\ m(t) \quad (35)$$

where m is the number of arms.
The sum of all capacitance in the arm,

$$V_c^m = m(t).\ V_c^{\varepsilon}(t)$$
$$i(t) = C^{eff(m)} . \frac{d}{dx}(V_c^{\varepsilon}(t)) = [C^{arm} / m(t)].[\frac{d}{dx}(V_c^{\varepsilon}(t))] \quad (36)$$

The voltage level and THD are determined by the sampling frequency. If the number of sub-modules and MI are constant, then two critical values of sampling frequency can be found out.

$$f_1\text{: Higher limit of } f_s\text{: } f_s < f_1 \quad (37)$$

f_2: Higher limit of B : $f_s > f_2$ (38)

$$N_{level} = \frac{f_s}{2f_0} + 1 \ (f_s < f_1) \quad (39)$$

$$N_{sm+1} \quad (f_s > f_2) \quad (40)$$

The critical values of sampling frequency can be found out by using the following:

$$\begin{aligned} dV_{ref} &= \frac{k}{2} V_{dc} \omega_0 \cos(\omega_0 t)\, dt \\ &= \frac{k}{2} V_{dc} \omega_0 \cos(\omega_0 t)\, T_s \\ &= k.V_{dc}.\pi.\frac{f_0}{f_s}\cos(\omega_0 t) \end{aligned} \quad (41)$$

The lower value of sample frequency indicates that its sampling interval is equal to single capacitor voltage

'V_C'. It occurs at $\omega_0 = \frac{\pi}{2} - \omega_0 t_s$ (42)

$$dV_{ref|min} = k.V_{dc}.\pi.\frac{f_0}{f_s}\cos(\omega_0 t) \quad (43)$$

$$\omega_0 t = \frac{\pi}{2} - \omega_0 t_s = V_{cap} = k.N_{sm}.\pi.\frac{f_0}{f_s}\sin 2\pi\frac{f_0}{f_s} = 1. \quad (44)$$

If $f_s \gg 2\pi f_0$, then

$$2.k.N_{sm}\frac{\pi^2.{f_0}^2}{f_s^2} = 1 \quad (45)$$

$$\text{So, } f_1 = \pi f_0 \sqrt{2.k.N_{sm}} \quad (46)$$

The upper value of voltage can be calculated at $\omega_0 t = 0$

$$\begin{aligned} dV_{ref|max} &= k.V_{dc}.\pi.\frac{f_0}{f_s}\cos(\omega_0 t)|\ \ \omega_0 t = 0 = V_c \\ &= k.N_{sm}.f_0.\pi \end{aligned} \quad (47)$$

THD can be calculated as $THD = \sqrt{\frac{\sum_{n=2}^{\infty} V}{V_{e-l-1}}}$ (48)

- Sample frequency V_s.THD N=20, 30, 50, 100, 200…. f_0=50Hz, k=0, 0.1, 0.2, …1.
- N_{sm} V_s THD
- K π THD

The above all equations can be written in the form of state space:

$$\frac{d}{dt}\begin{bmatrix} i_{cir} \\ V_{cu}^{\varepsilon} \\ V_{cL}^{\varepsilon} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & -\frac{N_{uv}}{2L} & -\frac{N_{Lv}}{2L} \\ \frac{N_{uv}}{C^{arm}} & 0 & 0 \\ \frac{N_{Lv}}{C^{arm}} & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{cir} \\ V_{cu}^{\varepsilon} \\ V_{cL}^{\varepsilon} \end{bmatrix} + \begin{bmatrix} \frac{V_d}{2} \\ \frac{N_{uv}.i_v}{2C^{arm}} \\ -\frac{N_{Lv}.i_v}{2C^{arm}} \end{bmatrix} \quad (49)$$

$$m(t) = m.\cos(\omega_n.t) \quad (50)$$

The load current can be assumed as:

$$i_v(t) = i_v^0(t)\cos(\omega_n t + \varphi) \quad (51)$$

The voltage can be represented as:

$$N_{topr}(t) = \frac{1-m(t)}{2} \quad \text{and} \quad N_{Lowr}(t) = \frac{1+m(t)}{2} \tag{52}$$

In real time operating conditions, the sum of the upper arm voltages and lower arm voltages should be equal, but in practical those upper and lower arm will not be equal, due to which the circulating current will exist in the system. There are certain control techniques to control the circulating currents. Among them, one is to provide certain offset voltage to maintain the same voltage level for upper and lower arm.

By applying KVL infig.4,

$$\text{Upper } V_{load} = \frac{V_{dc}}{2} - i_{rt}.R - L.\frac{di_{rt}}{dt} - N_{rt}.V_{cirtop}^{\varepsilon} \tag{53}$$

$$\text{Lower } V_{load} = -\frac{V_{dc}}{2} - i_{rl}.R - L.\frac{di_{rn}}{dt} - N_{rl}V_{cirlow}^{\varepsilon} \tag{54}$$

Equation (53) – equation (54) gives:

$$V_{load} = \frac{V_{ctop}-V_{cLower}}{2} - \frac{R}{2}i_r - \frac{L}{2}\frac{d}{dt}(i_r) \tag{55}$$

$$L\frac{d}{dt}(i_{cir}) + R.\, i_{cir} = \frac{V_{dc}}{2} - \frac{V_{clow}+V_{ctop}}{2} \tag{56}$$

- The load voltage depends upon the current i_V, and difference of upper and lower capacitor.
- i_{cir} depends only on the DC link voltage and the sum of the arm voltages.

Therefore, adding some voltage will not affect the load voltage but it will affect the current, then the total circulating current will be controlled and system can maintain steady state condition.

$$\frac{V_{dc}}{2} - \frac{R}{2}i_{load} - R.\, i_{cir} - \frac{L}{2}\frac{d}{dt}(i_{load}) - L.\frac{d}{dt}(i_{cir}) - V_{ct} = V_r \tag{57}$$

$$V_{cu} = \frac{V_s}{2} - V_u - \frac{R}{2}i_{load} - R.\, i_{cir} - \frac{L}{2}\frac{d}{dt}(i_{load}) - L.\frac{d}{dt}(i_{cir}) \tag{58}$$

$$V_r + \frac{R}{2}i_{load} + \frac{L}{2}\frac{d}{dt}(i_{load}) = \frac{V_{cLow}-V_{ctop}}{2} \tag{59}$$

$$\text{Take } \frac{V_{cLow}-V_{ctop}}{2} = \text{ev (error voltage)} \tag{60}$$

$$V_{ctop} = \frac{V_{top}}{2} - \text{ev} - V_{cir} \tag{61}$$

$$\text{and} \qquad V_{cLow} = \frac{V_{dc}}{2} + \text{ev} - V_{cir} \tag{62}$$

$$\text{So, } V_{diff} = R.\, i_{cir} + L.\frac{d}{dt}(i_{cir}) \tag{63}$$

In order to determine the difference voltage between the upper and lower capacitors, one should find the energy stored in the capacitor.

$$E_{rtop}^{\epsilon} = \frac{C^{arm}}{2}(V_{rtop}^{\epsilon})^2 = N.\left[\frac{C}{2}(V_{rtop}^{\epsilon}/N)^2\right] \tag{64}$$

$$E_{rlow}^{\epsilon} = \frac{C^{arm}}{2}(V_{rlow}^{\epsilon})^2 = N.\left[\frac{C}{2}(V_{rlow}^{\epsilon}/N)^2\right] \tag{65}$$

The change in energy stored in the capacitor is:

$$\frac{d}{dt}(E_{cu}^{\epsilon}) = i_{uv}.\, V_{cu}^{\epsilon} = \left(\frac{i_V}{2} + i_{cir}\right)\left(\frac{V_s}{2} - \text{ev} - V_{cir}\right) \tag{66}$$

$$\frac{d}{dt}(E_{cL}^{\epsilon}) = -i_{Lv}.\, V_{cL}^{\epsilon} = \left(-\frac{i_V}{2} + i_{cir}\right)\left(\frac{V_s}{2} + \text{ev} - V_{cir}\right) \tag{67}$$

then the total energy is shown eq(68) and eq(69)

$$E_c^{\in} = E_{rtop}^{\in} + E_{rlow}^{\in} \quad (68)$$

$$E_c^{\Delta} = E_{rtop}^{\in} - E_{rlow}^{\in} \quad (69)$$

Difference is:

$$\frac{d}{dt}(E_c^{\in}) = (V_s - 2V_{cir}).\, i_{cir} - e_V.\, i_V \quad (70)$$

$$\frac{d}{dt}(E_c^{\Delta\in}) = \left(\frac{V_s}{2} - V_{cir}\right).\, i_v - 2e_V.\, i_{cir} \quad (71)$$

Some important conclusions are:

- $i_{cir}.V_s$: this represents the product of power delivered to outside.
- $i_{cir}.V_{cir}$: this represents the losses occurred in the system.
- $i_V.e_V$: this is the power delivered to the load.
- In overall, if we control the i_{cir}, the system capacitor energy can be controlled.
- DC component of i_{cir} has no impact on the difference of capacitor energy as there are no DC components in ev.

The DC component of i_{cir} only can be used to control the total capacitor energy. But the AC component of i_{cir} having the fundamental frequency as the output voltage ev can be employed to control the capacitor energy.

- The product of $e_V.i_{cir}$ will make the energy to change.
- V_{diff}, i_V will give the same effect but this is small for small R and L, thus we need to develop a control strategy for e_V, i_{cir} only.

4. CONCLUSION

The following are the significant contributions and recommendations for further research in MMI.

- MMI is reviewed with different topologies and traced different problems with topologies.
- MMI is reviewed with different modulation techniques and their effects.
- MMI is reviewed with many control techniques and compared with each other.
- It has been given detailed analysis for modulation, control and design.

The important conclusion from the review as below:

- The hybrid topology and control strategy, the dc-link voltage in the IGBT converter and input harmonic currents in the IGCT converter can be regulated.
- It is possible to reduce the sampling frequency further by employing programmed PWM techniques.
- The modular concept allows the application for a wide power range.
- The requirement of equalized power sharing between levels can be resolved using a PWM switching strategy which also compensates the inherent harmonic interaction in the converter system.
- The Modular Multilevel Converter offers superior technical characteristics for HVDC, especially without passive filters at the AC-side and DC-side
- The use of transformer less scheme provides additional flexibility in system configurations and significant reductions in cost and footprint of the converter station.
- The discrete model is used to minimize a defined cost function associated with the internal control objectives of an MMC control.
- Voltage sharing of the devices will be handled automatically by the topology.
- The waveform shape will lead to sinusoidal waveform due to which the THD will be reduced and the harmonics as well.
- The operating voltage of the converters can be increased, instead of connecting the devices in series or in parallel, which makes the system more complex.
- Discrete model do not allow an analytical approach to model the converter and design the control system.
- Numerical solutions of sub-module with higher number of switching require considerable time.

- Under balanced condition, only positive sequence of current will flow in the buffer inductor or arm inductor.
- Under unbalanced condition, all positive, negative and zero sequence of current will flow in the buffer inductor or arm inductor.
- These inductors are necessary to handle the voltage difference between top and bottom side of the converter.
- These inductors can limit the fault current in case of the faults if any arises.

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