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Harmonic Mitigated Front End Three Level Diode Clamped High Frequency Link Inverter by Using MCI Technique

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ABSTRACT

In this paper it proposes a high efficient soft-switching scheme based on zero-voltage-switching (ZVS) and zero-current-switching (ZCS) principle operated with a simple auxiliary circuit extended range for the front-end isolated DC-AC-DC-AC high power converter with an three phase three level diode clamped multi level inverter by using Minority Charge Carrier inspired optimization technique (MCI) with Total Harmonic Distortion (THD), Switching losses, Selective harmonic elimination maintaining with its fundamental as an objective function. Input to the inverter is obtained by the photo voltaic cells and with battery bank. The switching scheme is optimized by MCI technique, analyzed and executed in Matlab and implemented with a digital signal processor (DSP) .Experimental results with different loads have observed and shows its effectives, robustness of the applied technique.

1. INTRODUCTION

Multidimensional scaling is a technique for exploratory analysis of multidimensional data, whose essential part is optimization of a function possessing many adverse properties including multi objectivities, multimodality, and non differentiability etc,. In this paper, global optimization algorithms for multi Objective problems are chosen for different kind of problems especially in the power Industry. MCI is a global optimization algorithm applied to the three phase three level diode clamped multi level Voltage Source Inverter (MLVSI), in which Selective Harmonic Elimination (SHE), THD, Switching losses and maintain with its fundamental is taken as an objective function. Different optimized pulse patterns are obtained by the MCI, these are simulated in MATLAB with their analysis is matched with the experimental results and implemented at practical situations with different loads which shows its effectiveness and robustness of technique. Some of the problems faced by the power electronic industry while converting energy from the sources such as photo voltaic cells, fuel cells, distributed energy systems etc are low power conversion with less efficiency, harmonics, switching losses, THD, bulk size and cost. In order to overcome this, This article presents universal optimized switching technique applied to a inverter to overcome the lower power loss, less total harmonic distortion (THD), less foot print area, higher current density, lower switch stress, operating for various load conditions, operating with sudden changes in load, operating with various power factors, without using of a clamping circuit, it should capable to convert low DC to high power AC applications, it should not have circulating currents, small duty cycle loss and no severe parasitic ringing.

Another requirement is that, the equipment should occupy less foot print and high current density with high efficiency is the primary requirement with isolation. Isolation for power electronic equipment is achieved by using a transformer. Normally line frequency transformers (which is normally operated at low frequency such as 50 or 60 Hz) occupy large space, bulky and lesser current density comparatively with high

frequency transformer. High frequency transformer normally operated above 100 KHz occupies less foot area, high current density and less weight and by this it can attain some of the objectives. In order to achieve this, here implemented a Zero current and zero voltage switching for a front end operated inverter followed by a three phase three level diode clamped inverter with a simple auxiliary circuit.

In order to eliminate the switching losses of a front end inverter, SK Mazumder et.al have implemented a front end isolated converter and done extensive research work in that. It had achieved more than 97% efficiency for a high frequency linked inverter. Another important contribution has done in [18-22]. The concept of Multi Level Inverters (MLI) does not depend on just two levels of voltage to create an AC signal. Instead several voltage levels are added to each other to create a smoother stepped waveform with lower dv/dt and lower harmonic distortions. With more voltage levels in the inverter the waveform it creates becomes smoother, but with many levels the design becomes more complicated, with more components and a more complicated controller for the inverter is needed. The multi-level Voltage Source Converter topologies largely address this issue and permit utilization of the most economically available switch in a converter, which has a voltage rating well beyond that of the switch. Among the multi-level VSC configurations, the multi-level Neutral Point Diode Clamped (NPC) converter has been widely accepted for applications in high power drives and the utility systems. As compared with the other prevalent multi-level converter topologies the NPC converter uses a fewer number of capacitors and switches per phase to synthesize the desired output voltage levels. It is therefore more economical and reliable [11-17]. Hence, it is combining the best possible two techniques and make the system much more efficient than normal.

2. DIODE CLAMPED MULTI LEVEL INVERTER WITH A HIGH FREQUENCY LINK

The numbering order of switches is S1, S2, S3, S4 and S5, S6, S7, S8, S9, S10, S11, S12. The dc bus consists of two capacitors C1, C2. The voltage across each capacitor is Vdc/2. An m –level inverter leg reqires (m-1) capacitors, 2(m-1) switching devices and (m-1)(m-2) clamping diodes. The input supply from any fuel cell can be given to the inverter which consists of a two legs called leading leg and lagging leg. Both leg consists of a MOSFET and IGBT indicated as M1, IG1, M2, IG2 respectively. The output of the inverter from high frequency transformer along with an inductor LSource. The pulsating output is given to the diode bridge rectifier for which the capacitor, inductor will acts as a input filter, blocking capacitor as well. The green dotted line will acts as filter and combination of green dotted and red dotted line indicates as auxiliary ciruit. The main function of this auxiliary circuit is to ensure the ZCS and ZVS for the front end inverter. Lsr is the saturable reactor which is in placed series with the high frequency transformer, ILsr is the current passing through the reactor, IPTrans, IStrans, VPtrans, VStrans is the current and voltage of the transformer primary and secondary respectively. Ilo is the current passing through the filter cum auxiliary inductor, Ida is the current passing through the auxilay diode. The proposed circuit is shown Figure 1.

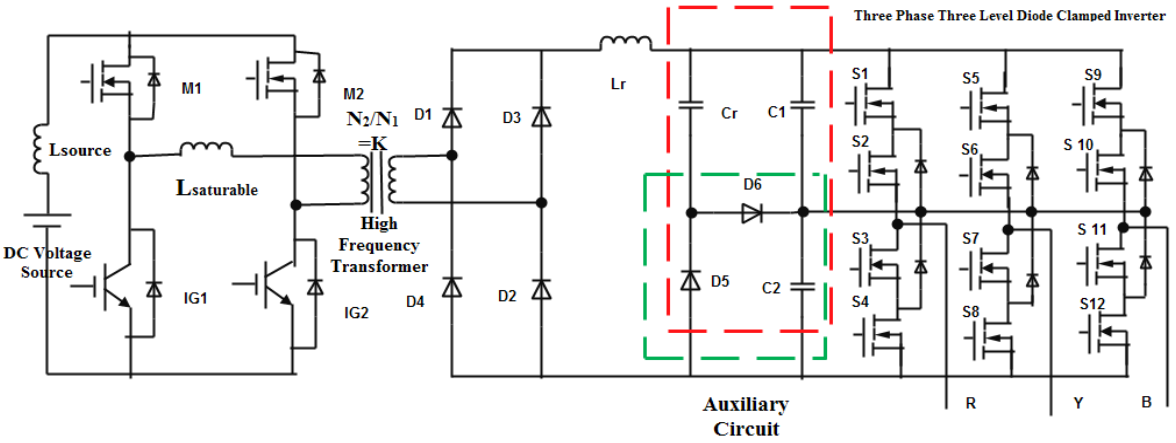


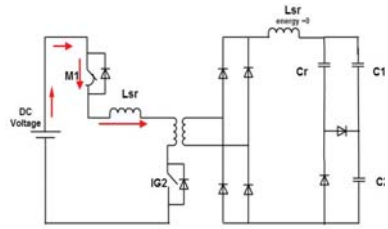
Figure 1. Three Phase Three Level Diode clamped High frequency Link Inverter

3. BASIC PRINCIPLE AND OPERATION

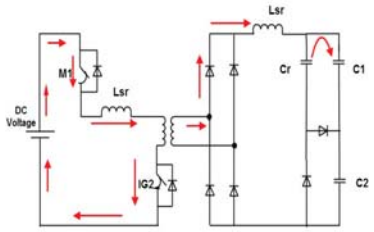
This principle can be explained in two sections. In the first, the basic principle and operation of a front end isolated inverter and three phase three level diode clamped inverter in the second. The basic operation of the proposed ZVCS converter have fourteen operating modes and working on the principle of pulse phase shift modulation technique. Here, it has been considered only six operating modes for the positive half cycle and remaining will be reflected of these modes.

Mode1: (0<t<t1)

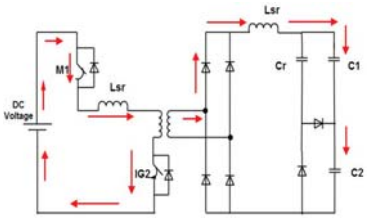
Here assumed that, the inductor is in discharged condition. When the switch M1 is on condition, the total energy that is present in inductor dissipated and current in this condition is zero.



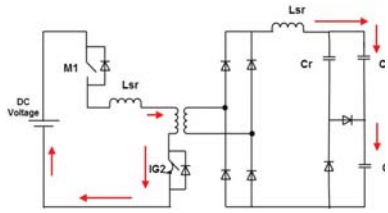
Mode:1



Mode:2



Mode:3



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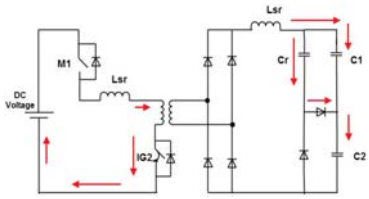
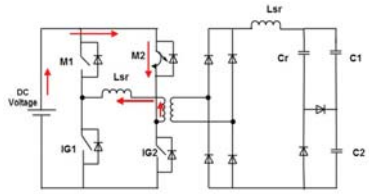


Mode:5



Mode:6

Mode2: (t1<t<t2)

In this mode, both switches M1 and IG2 are in on. The total input power will be transferred through the transformer to output. Here at this time the filter capacitor C is charged along with the filter inductor. The amount of energy that can be stored at this time in inductor is $\frac{1}{2}LI^2$ and in capacitor is $\frac{1}{2}CV^2$.

The current through the transformer is given in equation (1)

$$I_{tr}(t) = N.I_0\big(1 - cos(\omega t)\big) - \frac{V_s - V_0.\frac{1}{N}}{Z}\sin(\omega t) + NI_0 \quad (1)$$

$$I_C(t) = NI_0 - I_{tr}(t) \quad (2)$$

$$V_C(t) = NV_{in}(1 - \cos(\omega t)) - N^2 Z I_0 \sin(\omega t) \quad (3)$$

Mode 3: (t2<t<t3): This mode begins with auxiliary ciruit which is shown in red dotted lines, The capacitor is slowly charging .Since the capacitor voltage Vca is less than the input voltage, current will start flowing through auxiliary circuit which is shown in figure 2. M1 turns on softly as inductor Lr is in series with this switch and limits the rise in current through it. Cr discharges into the auxiliary inductor during this mode. Since voltage Vcs is lesser than the bridge voltage, diode D1 is reversed biased and does not conduct. This mode ends when Cr voltage reaches the voltage across off-state bridge switches.

Mode 4: (t4 < t < t5) : This mode begins when diode D1 becomes forward biased and starts to conduct. The voltage across the bridge switches therefore follows capacitor voltage Vca which is decreasing. This voltage is also equal to the voltage across the transformer. Ideally, if the voltage across the transformer is less than the output. Diodes become reversed biased and power is not transferred to the output, but this power transfer does not in fact stop immediately because of the presence of leakage inductance in the transformer. The transformer current reaches zero at the end of this mode.

$$V_{ab} = \frac{NI_0}{\omega}\left(\frac{1}{\omega^2} - \frac{1}{C_{tot}}\right)\sin(\omega t) - \frac{NI_0}{\omega^2}\,T + 2V_{in} \quad (4)$$

$$I_{tran} = NI\left(1 - \frac{C}{\omega^2}\right)\cos(\omega t) + \frac{C}{\omega^2}NI_0 \quad (5)$$

$$V_C = \frac{I_0}{C_{tot}\omega^2}\sin(\omega t) + \frac{I_0}{C_{tot}\omega^2}\sin(\omega t) - NV_0 \quad (6)$$

Mode 5: (t5 < t < t6): The output capacitances of switches M1 and IG2 and capacitor Cr keep discharging during this mode. The current in the auxiliary circuit branch is equal to the sum of the current from the full-bridge caused by the discharging of the switch output capacitances and Cr, and the input current that flows through Lsr.

$$-V_c(t) + L\frac{di(t)}{dt} + V_{in} = 0 \quad (7)$$

$$V_c = \left(I_{in}\sqrt{\frac{L}{C}} + \frac{V_0}{N} - V_{in}\right)\cos\big(\omega(t - t_0)\big) + V_{in} \quad (8)$$

$$V_c = C\omega\left(I_{in}\sqrt{\frac{L}{C}} + \frac{V_0}{N} - V_{in}\right)\sin(\omega(t - t_0)) \quad (9)$$

Mode 6: (t6 < t < t7): At the beginning of this mode, the DC bus voltage is zero and is clamped to zero as the body-diodes of the converter switches are forward biased and start to conduct. Switches IG2 can be turned on with ZVS sometime during this mode while current is flowing through their body-diodes. Also during this mode, the current that flows through the auxiliary circuit (and thus the current through the full-bridge) begins to decrease because the voltage across the auxiliary inductor is negative as the input voltage is at one end of the circuit and the DC bus voltage is zero. The auxiliary circuit current is equal to the current through Lsa at the end of this mode, which makes the current flowing through the full-bridge to be zero. Different modes of switching operation is shown in figure 2.

In case of three-phase full bridge three level diode-clamped converter in which the dc bus consists of four capacitors, C1, C2,. For a dc bus voltage V dc, the voltage across each capacitor is V dc /2, and each device voltage stress will be limited to one capacitor voltage level i.e. V dc/2, through clamping diodes [7, 9-11].

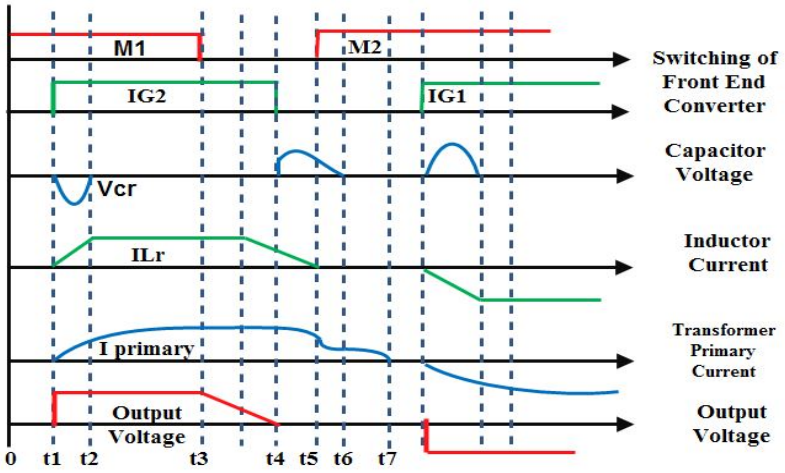


Figure 2. Different modes of operation of a Three Level Diode clamped High frequency Link Inverter

4. PROBLEM FORMULATION

The Harmonic elimination problem is formulated as a set of transcendental equations, that can be solved to determine the angles for turning the switches ON and OFF in a three phase diode clamped inverter. This will generate desired fundamental amplitude and eliminate specified harmonics. In this work the notch angles for a three phase inverter has been determined by using the Accelerated particle swarm optimization technique. The harmonic elimination problem in PWM inverter is treated as an Optimization problem and solved using MCI optimization. The THD of the output voltage of PWM inverter is used as the objective function. The switching angles are calculated by using MCIA and objective function is minimized to obtain

in minimum THD [17]. In Selective harmonic elimination the switching angles for a particular Modulation Index (MI) are calculated and then the pulse sequence and duration for the various gate pulses of the power semiconductor switches of the inverter are generated. In this work all simulations have been carried out for inverter with output frequency of 50Hz and modulation index of 0.9. The number of nonlinear equations in terms of unknown switching angles depends on number of harmonic components to be eliminated. The equations have to be solved for each value of modulation index using numerical minimization approach or artificial intelligence techniques. The fundamental component is assigned a desired output value and other selected orders of harmonics are equated to zero to form the set of transcendental equations.

The fourier series of output voltage can be expressed as

$$\begin{aligned}
&\cos(\alpha_1)+\cos(\alpha_2)+\cos(\alpha_3)+\cos(\alpha_4)=(m-1)*M\\
&\cos(5\alpha_1)+\cos(5\alpha_2)+\cos(5\alpha_3)+\cos(5\alpha_4)=0\\
&\cos(7\alpha_1)+\cos(7\alpha_2)+\cos(7\alpha_3)+\cos(7\alpha_4)=0\\
&\cos(11\alpha_1)+\cos(11\alpha_2)+\cos(11\alpha_3)+\cos(11\alpha_4)=0
\end{aligned} \quad \text{(I)}$$

Along with these equations, the losses that are present in systems can be a combination of turn on losses, turn off losses and conduction losses.

$$P_{TotalIGBT}=P_{CondIGBT}+P_{commIGBT} \tag{10}$$

$$P_{TotalDIODE} = P_{CondDIODE} + P_{commDIODE} \tag{11}$$

$$P_{condDIODE} = I_{Avg}V_{CE} + I^2{}_{rms}R_{diode} \tag{12}$$

$$P_{condIGBT} = I_{Avg}V_{CE} + I^2{}_{rms}R_{IGBT} \tag{13}$$

$$I_{Avg}=\frac{1}{2\pi}\int_0^{2\pi} I_m \sin(t-\alpha)\frac{2}{\sqrt{3}}M\sin(t).dt+\frac{1}{6}\sin(3t)dt \tag{14}$$

$$I_{rms}=\sqrt{\frac{1}{2\pi}\left\{\int_0^{2\pi} I_m \sin^2(t-\alpha)*\frac{2}{\sqrt{3}}M*\sin(t)+\frac{1}{6}\sin(3t)dt\right\}} \tag{15}$$

$$PowerLoss_{Conduction}=\begin{cases}\left(\frac{1}{4}\frac{T_{on}}{T_{off}}\frac{V}{2}t_{rr}I_{rr}{}^2\int_{\alpha 1}^{\alpha 2}\sin^2(t-\phi)dt+\frac{1}{3\pi}\frac{T_{on}}{T}\frac{V}{2}t_{rr}\right.\\ \left.*\int_{\alpha 1}^{\alpha 2}\left[0.8+0.2\frac{I_m}{I_c}\sin(t-\varphi\right]*\left[0.35I_{rr}+\frac{0.15*\sin(t-\varphi)}{I_c}\right]\right.\end{cases} \tag{16}$$

$$\begin{aligned}PowerLoss_{on\&off} &= \left\{\frac{T_{on}}{T}\frac{V}{2}I_m t_{fr}\int_{\alpha 1}^{\alpha 2}\left[\frac{1}{3}\sin(t-\phi)\right]+\frac{1}{6}\sin^2(t-\phi)\frac{I_{cn}}{I_{cf}}dt\right\}\\ &+\frac{1}{16\pi}\frac{T_{on}}{T}\frac{E}{2}I_m t_{fr}\int_{\alpha 1}^{\alpha 2}\left(0.8+0.2\frac{I_{cn}}{I_{cf}}\sin(t-\varphi)\right)\left(0.35I_r+0.15\frac{I_{cm}}{I_{cf}}\sin(t-\phi)+I_{cm}\sin(t-\phi)\right)\end{aligned} \tag{17}$$

The nonlinear transcendental equations are solved by using the MCI techniques as follows.

5. INTRODUCTION TO ALGORITHM

In order to optimize the above specified objective functions. Here it has been used an optimization technique.

Objective function F(X), Where X =(x1, x2, x3, … xn). Initialize the number of electrons that are present in the space x1, x2, x3 … xn with a velocity 'V'. Now we will choose the voltage and resistance range.

Q=I*T=V.T/R As the V, R, T are defined at the starting.

While (T<max iterations)

Generate the new solution by adjusting the resistance and update their resistance values.

If (rand>Ri)

Select a solution among all the best solution. Generate a local solution around and select the best solution
End if
Generate a new solution by going in different paths.
If (rand < Ai & f(xi)<f(xk))
Accept the new solutions
Increase Voli and reduce the Ri.
End if
Rank the all electrons and find the current best xi.
End while

Movement of electrons that are generated by us call as virtual electrons. Here the all the electrons are moving with a constant speed.

Xit=xit-1 + Vit (Vit The voltage at which they are positive)
Rit=Rit-1 + (xit – xk) Vi (Vi Velocity of the electron).
Qit=Wit-1 + β(Rit – Rk)Vi (β belongs to [0,1])
Rx, xk be the global best resistance and global best position respectively. [23, 24]

$$Rit+1 = Rio[1-exp(-rt)] \quad Dit+1 = \alpha - Dit$$

Here, it has been considered, the objective function as shown in set of Eq(I), eq(16) and eq(17)

6. SWITCHING TECHNIQUE

In this section it proposes an optimized switching technique expressed as a combination of sawtooth and sinusoidal signal in quarter wave symmetry. The optimum switching angles are obtained by MCI technique. Figure 2 shows the application of MCI optimization technique to Three phase three level diode clamped high frequency link multi level inverter switching wavefroms and Figure 3 shows the switching wave forms for each switch to Three phase three level diode clamped high frequency link multi level inverter, Switching scheme with MCI optimization technique to obtain forms for each switch to Three phase three level diode clamped high frequency link multi level inverter. In this switching technique, it has been used a two waveforms with a combination of saw-toothed and sinusoidal signal. Depending up on number of harmonics one can select the number of repeated waveform. The switching angles can be selected as follows. The optimum point will start at '0' and will travel through the slope of the line and will repeatedly check as proposed algorithm and finally will found the switching angles. The wave forms are repeated as per the different load conditions. For all figures, it could read as on X-axis, Time in milli sec and on Y-axis Voltage amplitude, unless otherwise specified. In figure 4, It has been specified as function Fc(u),in which MCI technique is incorporated and switching function is derived by using logic gates for DSP processor. In Figure 3, It was shown that the switching angles to be applied for each switch in a MLI. In Figure 4, Output voltage wave form for Three phase three level diode clamped high frequency link multi level inverter showing all lower order harmonics are eliminated.

7. ANALYSIS OF RESULT

The results of the three optimization techniques together with standard version of MCI are summarized. The information available from the summary are i) Minimum THD achieved ii) Number of iterations required to achieve minimum THD.

Figure 4. Experimental setup of proposed inverter

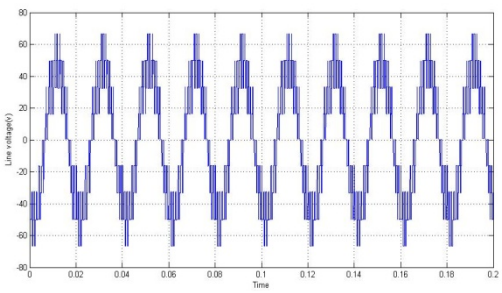


Figure 5. Output Voltage of proposed inverter

Table 1. Comparison between simulation and experimental values of harmonics order using mci

Harmonic order	Simulation in %	Experimental
1	100	100
5	0	0.001
7	0	0.002
11	0	0.004
13	0	0.094
17	0	1.41
19	0	0.150
23	1.1	3.21
29	2.3	3.21
31	0.001	0.907
35	1.5	1.76
37	1.1	1.42
	2.12%	2.97%

It can be observed, that, while running standard MCI, 380 iterations are required to obtain its best fitness value of 2.12%. Thus, for applications where processing power is a constraint, MCI is recommended for fast convergence and acceptable accuracy. In figure 5, It shows the voltage waveform through simulation.
Comparing Simulation and Experimental values of harmonics given in Tables 1 it is observed, that the experimental harmonic profile is close to, but consistently higher than the simulated values. The reason for this is the introduction of blanking time of 3μs to the inverter pulse sequence. The experimental setup shown in Figure 4.

8. CONCLUSION AND FUTURE SCOPE

MCI has been shown to achieve the best results, though requiring more than double the number of iterations required for Accelerated Particle Swarm optimization. Only one variant of optimization technique has been tried. Other variants using various flavors of MCI in combination with other optimization technique can be tried in future. This study was carried out for Selective Harmonic Elimination of four harmonics, which required introduction of five notch angles primaly and can be extended to further. Using higher number of notch angles better theoretical results can be obtained. However experimental results may not be consistent, as there will be very less switching losses. Further work can be carried out to study the divergence of the practical results from the theoretical results, with the increase in notch angles.

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