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Single Stage Single Phase Active Power Factor Corrected Ĉuk Topology Based AC-DC Converter

Md. Ismail Hossain, Mohammad Jahangir Alam
Department of Electrical and Electronic Engineering
Bangladesh University of Engineering and Technology, Bangladesh

Article Info	ABSTRACT
	This paper focuses on the analysis of a power factor correction (PFC) converter using close loop Ĉuk topology. Regardless of the input line voltage and output load variations, input current drawn by the buck or buck-boost converter is always discontinuous. The Boost converter suffers from high voltage stresses across the power electronic devices. The input current in Ĉuk converter is comparable to boost converter's input current. In this paper output voltage is controlled by inner current and outer voltage control loop along with power factor correction (PFC). It shows less input current THD, nearly unity power factor and better output voltage regulation of AC-DC converter under variable input voltage and output load. In this paper the relative performance between normal diode rectifier, open loop Ĉuk rectifier and close loop Ĉuk rectifier is presented. An algorithm for implementing close loop Ĉuk rectifier in digital domain is developed and simulated.

Corresponding Author:

Md. Ismail Hossain
Departement of Electrical and Electronic Engineering,
Bangladesh University of Engineering and Technology,
66 Green Road, Dhaka-1215, Bangladesh.
Email: jewel04eee@yahoo.com

1.   INTRODUCTION

Uses of Computer and telecommunications equipment have become important in our society. Electric vehicle is rapidly increasing in use due to its environment friendly technology. DC power supply is the heart of these devices and most of the case it comes from AC-DC converter. The efficiency, total harmonic distortion of input current, input power factor and regulated output voltage etc are the main concern of these AC-DC converters. Uncontrolled diode rectifier as shown in Figure 1 followed by L-C smoothing filters is widely used as a cheap power supply. Un-controlled charging of DC filter capacitor results in 50Hz pulsed ac current waveform at the input of the rectifier as shown in Figure 2. Several power quality problems arise at the source side, which includes poor power factor high input current total harmonic distortion (THD) as shown in Figure 3 failure of transformers due to overheating and harmonic pollution on grid [1]-[2] etc. Grid disturbances may result in malfunction or damage of electrical devices. Many methods for elimination of harmonic pollution in the power system are in use and new methods are being investigated. Restrictions on current and voltage harmonics are maintained in many countries through IEEE 519-1992 and IEC 61000-3-2/IEC 61000-3-4 [3] standards. The restrictions are associated with the idea of "clean power". The power factor correction (PFC) converter topology using active wave shaping techniques can overcome the problem in line current. The PFC converter forces the line to draw near sinusoidal AC current in phase with its voltage. Most of the single phase AC to DC conversion PFC works are done with Buck, Boost, and buck-boost or fly-back topology between the source and the load. Buck and buck-boost topology suffer from input discontinuous current [4]-[7] and Boost topology needs large value capacitance [8] to minimize the output voltage ripple therefore initial inrush current is higher than Ĉuk converter [9[-[10]. Ĉuk converter

requires low value intermediate capacitance to transfer energy to output capacitance and load [9]-[10]. Open loop Ĉuk converter as shown in Figure 4 suffers from less output voltage regulation, low power factor, low efficiency and high input current THD under input voltage and load variation. In this paper output voltage and input current control variable duty cycle Ĉuk converter has been proposed for minimizing output voltage variation due to line voltage and load variation and obtaining sinusoidal AC mains current. Fixed frequency is chosen due to easier parameter design comparable to hysteresis control.

2. PROPOSED CLOSE LOOP ĈUK REGULATOR BASED AC-DC CONVERTER

Proposed close loop Ĉuk regulator based AC-DC converter is shown in Figure 5. The technique used here is the Average Current Mode control. In Average Current Mode control, the output voltage is controlled by varying the average value of the current signal. The Voltage feed forward compensator controls the input voltage variation in such way that if the input voltage reduces then the output of Voltage feed forward compensator increases and vice versa. The actual output DC voltage is sensed and compared with a reference voltage then the voltage error is processed through the proportional integral controller. The output of the proportional integral controller is multiplied with the rectified input voltage and output of voltage feed forward compensator to make a reference current in phase with rectified input voltage. The real current is forced to track the reference current through current error compensator. The error between the actual current and reference current is processed through the proportional integral controller and then its output is compared with the Saw-tooth wave to generate the required PWM signal.
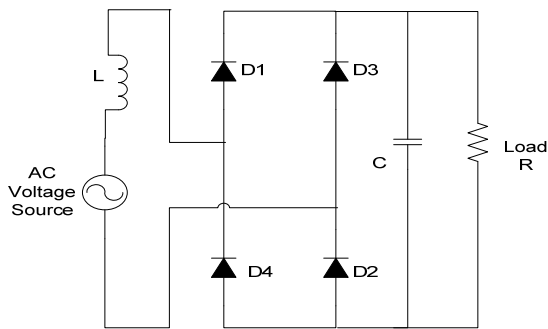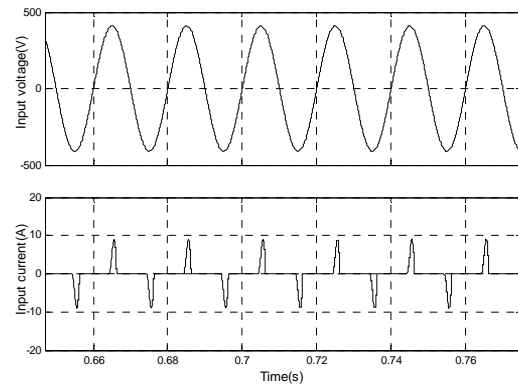

Figure 1. Normal diode rectifier

Figure 2. Input voltage and input current for 400Ω load resistance
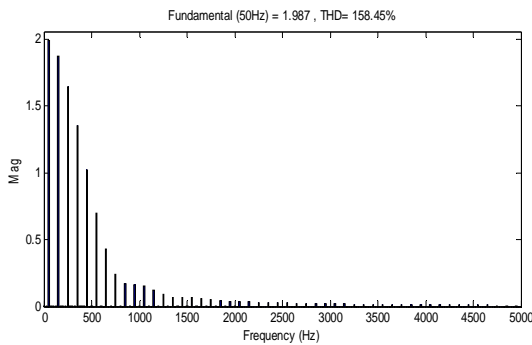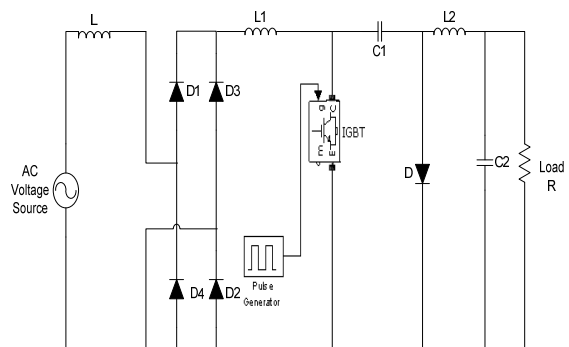

Figure 3. Input current THD for 400Ω load resistance

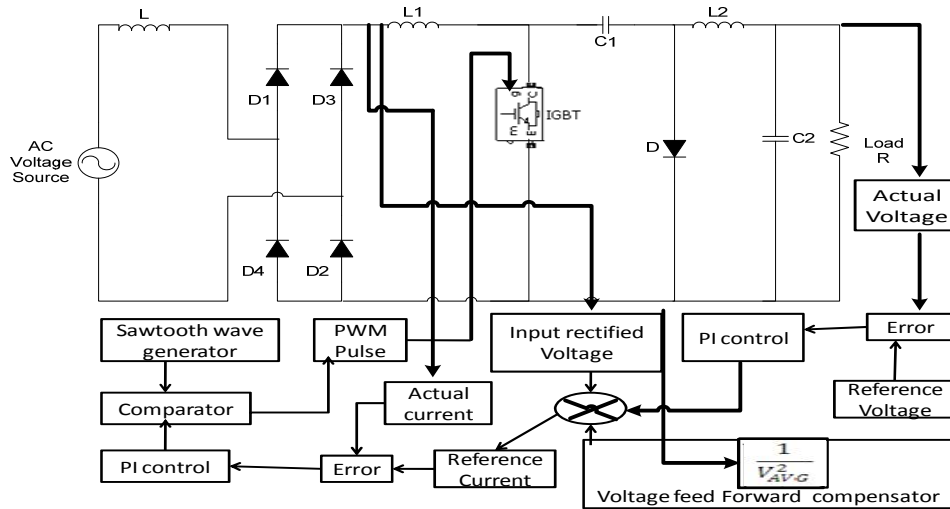
Figure 4. Open loop Ĉuk rectifier

Figure 5. Proposed close loop Ĉuk rectifier

3.   PROPOSED CLOSE LOOP ĈUK REGULATOR IN DIGITAL DOMAIN

Real time hardware circuit as shown in Fig. 6 is used to implement the proposed closed loop Ĉuk based AC-DC converter. The input rectified AC voltage and input rectified current are sensed using simple voltage dividing network and hall type sensor respectively. Negative output DC voltage is sensed through voltage dividing network and inverting network.

3.1. Average Voltage Computation in Digital Domain

In the analog domain, the continuous form of the average Voltage is:

$$V_{AVG} = \frac{1}{T}\int_t^{t+T} V_{ac}.dt \tag{1}$$

Where,
V_{ac} = the instantaneous AC input voltage
T= time period depending on the frequency of the AC input voltage.

In the digital domain the discrete form of this equation is:

$$i = n + \frac{T}{T_s}$$

Therefore,

$$V_{AVG} = \frac{1}{T}\sum_{i=n} V_{AC}(i).T_s \tag{2}$$

$$\text{or } V_{AVG} = \sum_{i=n} V_{AC}(i).\frac{1}{\frac{T}{T_s}} \tag{3}$$

$$\text{or } V_{AVG} = \frac{\sum V_{AC}(i)}{N} \tag{4}$$

Where,
V_{AC} = Input voltage at the ith sample.
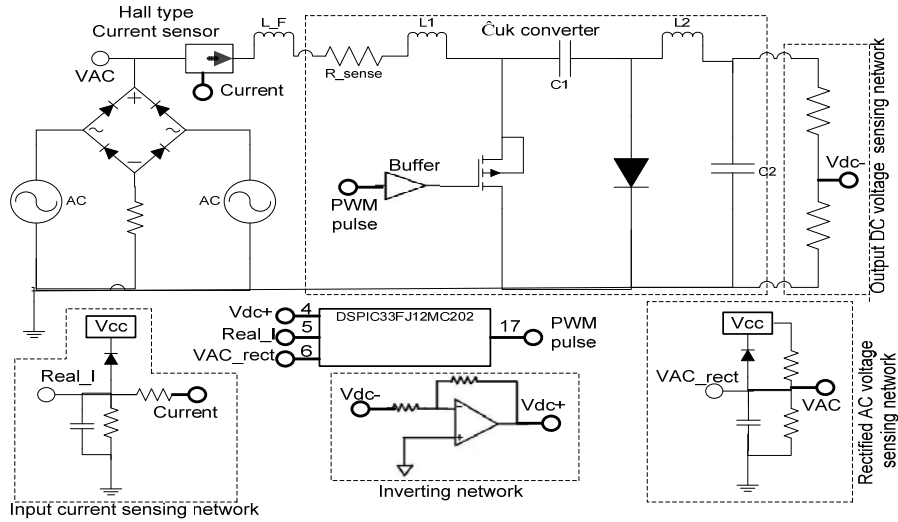N = Number of samples taken

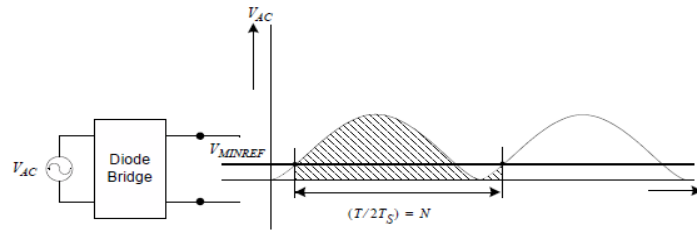Figure 6. Circuit diagram for close loop Ĉuk rectifier

Figure 7. Calculation of average AC voltage

Monitoring of zero crossing point is complecated in analog circuitry. Instead, the method used is to fix a minimum reference point for the input voltage, as shown in Figure 7. A counter starts when the sampled value of input AC voltage from ADC rises above V_{MINREF}, and stops when the voltage falls below V_{MINREF} in the next cycle. Figure 8 shows the program flow chart of average voltage computation in digital domain.
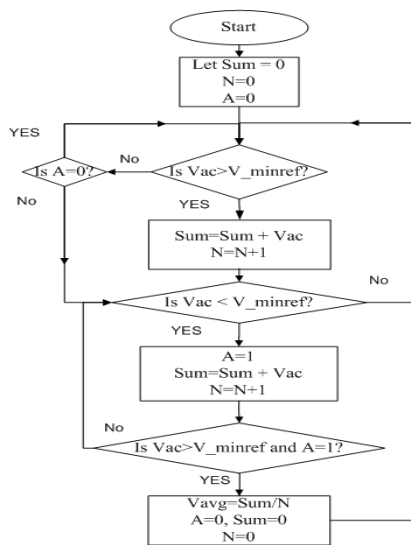

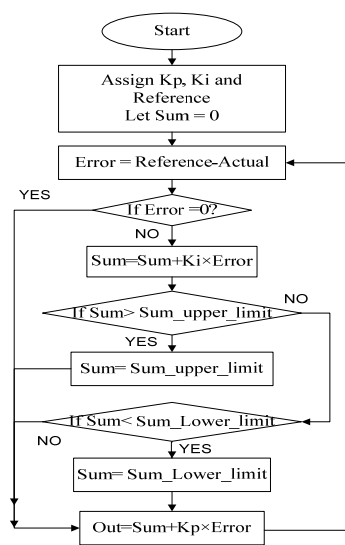Figure 8. Program Flow chart of average voltage computation in digital domain

Figure 9. Program Flow chart of PI control

3.2. Digital Implementation of Proportional Integral Control

The expression of proportional integral control in continuous time domain is defined by the following equation:

$$C(t) = K_P \times E(t) + K_I \int_0^t E(t)dt \tag{5}$$

Where:
C(t) corresponds to the output signal of the PI controller
E(t) =Reference – Actual(t) corresponds to the input error signal of the PI controller
K_P corresponds to the proportional factor
K_I corresponds to the integral constant

And the discrete form of PI expression:

$$C(n) \approx K_P \times E(n) + K_I T_S \sum_0^N E(n) \tag{6}$$

$$C(n) \approx K_P \times E(n) + \frac{T_S}{T_I} \sum_0^N E(n) \tag{7}$$

$$C(n) \approx K \times E(n) + \frac{1}{T_I} \sum_0^N E(n) \tag{8}$$

Where, $K_P = K$ and $K_I = \frac{K}{T_I}$

T_S is the sample time
T_I is the integral time constant
E(n)= Reference-Actual(n) input error at n[th] sample

The program flow chart of PI control is shown in Figure 9.

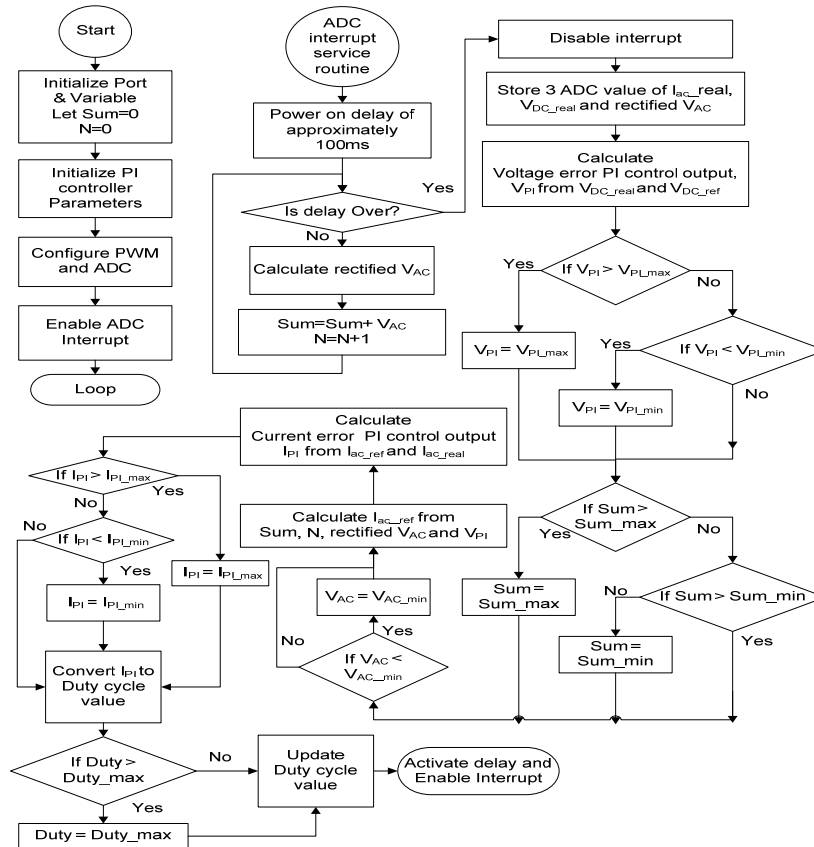## 4. PROGRAM FLOWCHART OF THE PROPOSED SYSTEM

Figure 10. Program Flow chart of the proposed control system

The main program flow chart is shown in Figure 10. After a Reset, when the program is executed, all the variables are initialized and peripherals are configured. The PI parameter values are defined for the control loop compensators. The PWM module is switched ON to operate at a frequency of 80kHz, and all the interrupts are enabled. The ADC module waits for a PWM module special event interrupt. On every period match, the PWM generates a trigger to the ADC to start sampling the signals and converting them. On a timer trigger, the ADC samples and converts the voltages and currents and later generates an ADC interrupt. The power factor correction routines run inside the ADC Interrupt Service Routine (ISR). A power-on delay is allowed for the capacitors to charge to the DC bus voltage.

After the power-on delay time (approximately 100 ms) completion, the control loops begin to execute. During the process of power-on delay, the voltage samples are accumulated and frequency is calculated. This enables the average voltage calculation to be done in the first iteration of the control loop itself, as the average voltage is already available for a period corresponding to one line voltage cycle. The voltage error compensators execute the voltage PI controllers having the measured value of output DC voltage. The average value of input voltage, squaring and dividing routines, execute in sequence from the measured value of input AC voltage thereby giving the voltage feed-forward compensator output. This output is used in conjunction with the voltage error compensator output to calculate the reference value of I_ac_ref. Having I_ac_ref and the measured value of the inductor current, the current error compensator executes the current PI controllers to produce the new duty cycle for the PWM pulse.
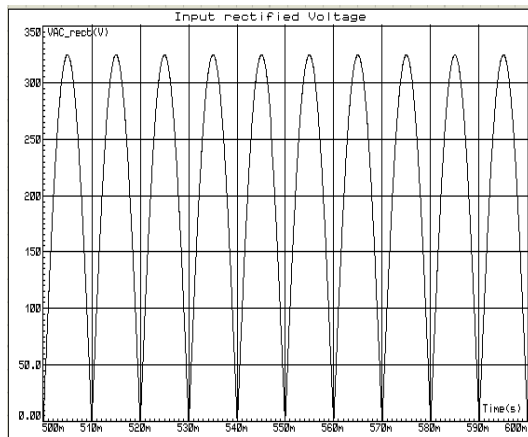
5. SIMULATION RESULT

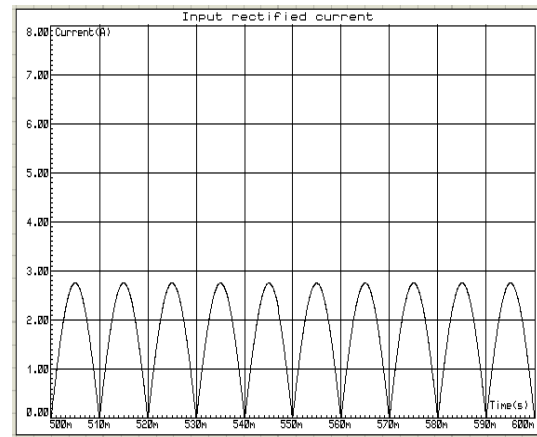Figure 11. 325V (peak) input rectified voltage
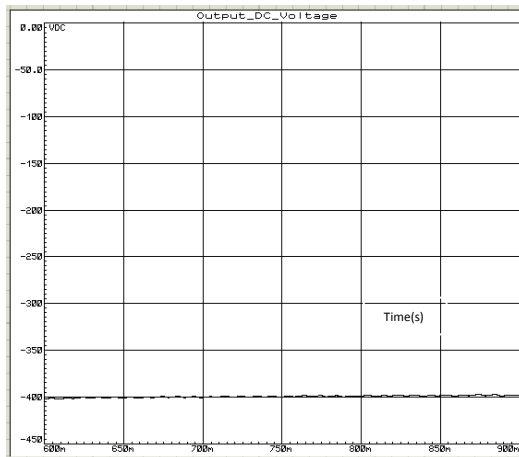

Figure 12. input rectified current for 400Ω load
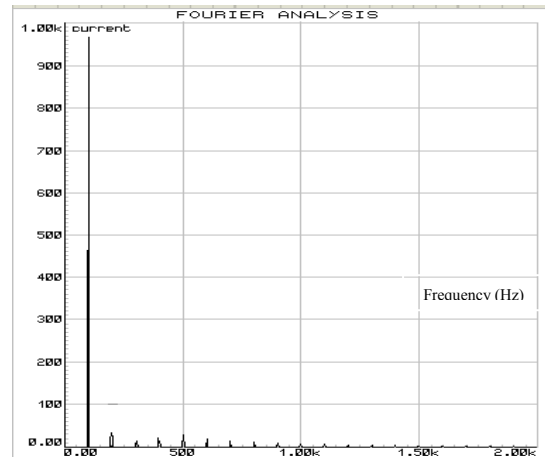

Figure 13. Output voltage for 400Ω load

Figure 14. FFT component of input rectified current for 400Ω load

L_F= 8µH, L1= 10mH, L2=1mH, C1=0.2µF, C2=330µF and switching frequency = 80000Hz are used of proposed close loop Ĉuk topology based AC-DC converter for simulation in proteus software. Normal diode rectifier and open loop Ĉuk rectifier simulation are performed in Matlab Simulink. Figure 11 to Figure 14 show the input rectified voltage, input rectified current, output voltage, FFT component of input current respectively. Figure 15 to Figure 19 show the relative performance of normal diode rectifier, open loop Ĉuk rectifier and close loop Ĉuk rectifier in terms of output voltage regulation, input PF, efficiency, input current THD under load variation and output voltage regulation under input voltage variation. Finally Figure 20 shows the output voltage regulation at different frequency.
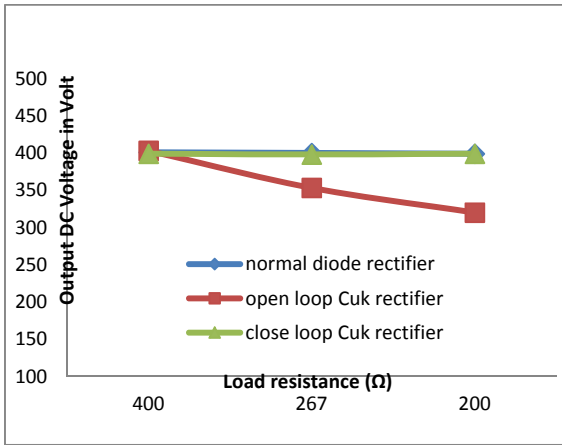

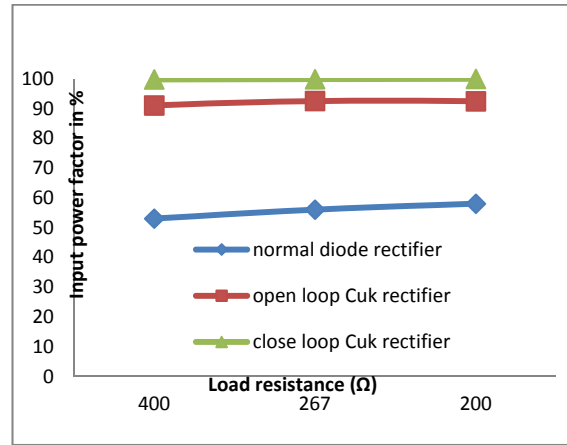Figure 15. Output voltage at different loads and 325V (peak) input voltage

Figure 16. Input PF at different loads and 325V (peak) input voltage
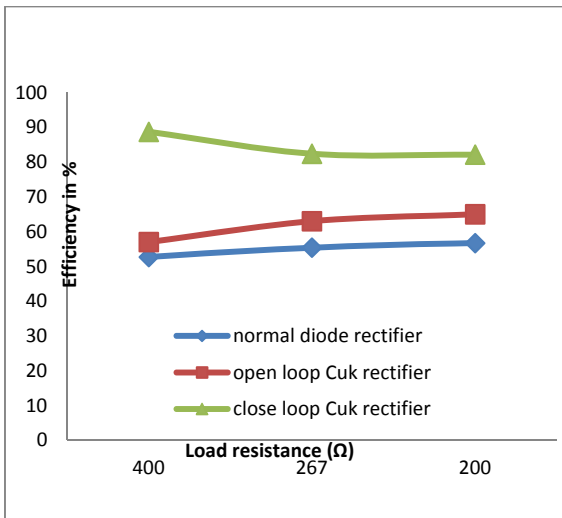

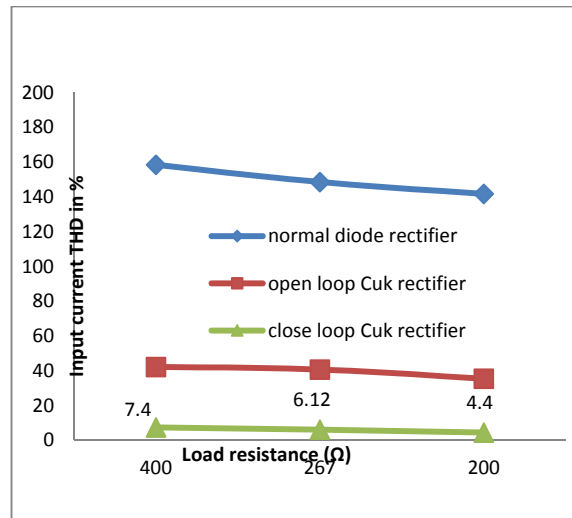Figure 17. Efficiency at different loads and 325V (peak) input voltage

Figure 18. Input current THD at different loads and 325V (peak) input voltage
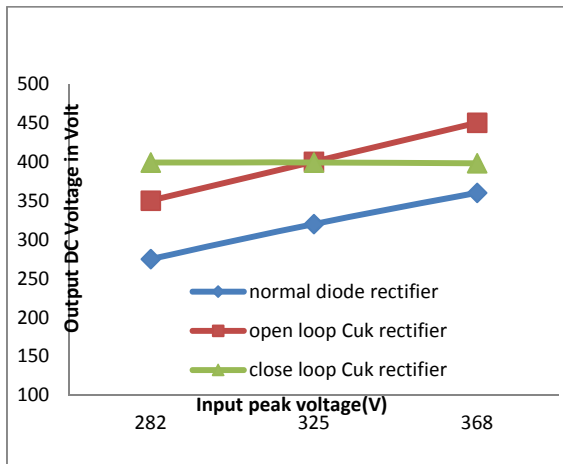
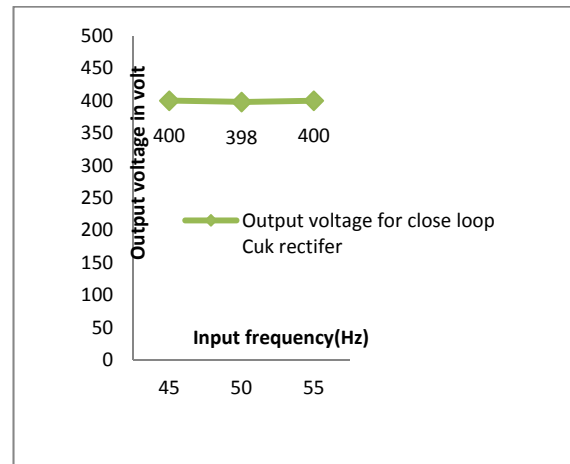Figure 19. Output voltage at different input voltages with 400Ω load resistance

Figure 20. Output voltage at different input frequency and 400Ω load resistance

6. CONCLUSION

In this paper the proposed close loop Ĉuk topology based AC-DC converter has analyzed and implemented in digital domain with intelligent program algorithms. The results of proposed controller show the improvement of input current THD, input power factor and output voltage regulation under the variable load and input voltage disturbance. The comparative performances of different AC-DC converters have presented and hence the effectiveness of the proposed close Ĉuk topology based AC-DC converter has verified.

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BIOGRAPHIES OF AUTHORS

Md Ismail Hossain received his M.Sc degree in Electrical & Electronic Engineering from Bangladesh University of Engineering and technology. He is working as an assistant professor in Electrical & Electronic Engineering Department at International Islamic University Chittagong. His research interests are Power Electronics, Industrial motor drive and automation, Hybrid electric vehicle, Microcontroller and Embedded Systems, Electrical Machine, Renewable energy and Smart Grid etc

Dr. Mohammad Jahangir Alam is working as a professor in Electrical & Electronic Engineering department at Bangladesh University of Engineering and technology. He received his B.Sc and M.Sc degree in Electrical & Electronic Engineering from Bangladesh University of Engineering and technology. He did his PhD in Electrical Engineering from Dublin City University, Ireland. His research interests are Electrical and optical characterization of thin films. Structural characterization of thin films (Infrared, X-ray diffraction and X-ray photoelectron spectroscopy techniques). Dielectric materials and power electronics etc.