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A Single-Phase Multilevel Current-Source Converter using H-Bridge and DC Current Modules

Suroso*, Toshihiko Noguchi**
* Departement of Electrical Engineering, Jenderal Soedirman University, Indonesia
** Departement of Electrical and Electronics Engineering, Shizuoka University, Japan

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ABSTRACT

This paper presents a different topology of H-bridge based multilevel current-source inverter (CSI). In this new inverter configuration, an H-bridge CSI is connected with a single or more current modules to generate a multilevel output current waveform with lower di/dt, and less distortion. Using the proposed multilevel CSI, the number of the power switching devices, and isolated gate drive circuits can be reduced. Moreover, chopper based DC current sources are presented to reduce the inductor size effectively to be in micro-Henry order, and to ensure the balance of the intermediate current levels. The proposed topology is inherently able to reduce the inductor conduction losses if compared with the conventional multilevel CSIs and the H-bridge CSI. Seven-level PWM inverter configurations with non-isolated DC current sources and with a single DC power source are verified through computer simulations. Furthermore, laboratory prototypes of seven-level CSI is setup and tested. The results show that the inverter circuit works properly to generate the multilevel output current waveform with low harmonics currents, small inductors and with less conduction losses which proves feasibility of the proposed multilevel CSI.

Corresponding Author:

Suroso,
Departement of Electrical Engineering,
Jenderal Soedirman University,
Jl. Mayjen Sungkono km. 5, Kalimanah, Purbalingga, Jawa Tengah, Indonesia.
Email: suroso.te.unsoed@gmail.com

1. INTRODUCTION

Some circuit configurations of multilevel current-source inverters (CSI) have been presented in some research papers. A traditional way to produce a multilevel current waveform is by connecting some H-Bridge CSIs in parallel [1], [2]. This inverter circuit is the dual of cascade H-bridge multilevel voltage source inverter (VSI). Unfortunately, the need of isolated DC current sources, power devices count and their gating circuits are some problems of this inverter circuit. Reference [3] presented the multilevel CSI topology using H-bridge and inductor-cell. This topology simplifies the requirement of isolated DC current sources in the parallel H-bridge multilevel CSI. Another circuit configuration of multilevel CSI is created by utilizing multi-cell configuration of multilevel CSI [1], [4], [8], which is the dual of flying capacitor multilevel VSI. Balancing control complexity of the intermediate level currents is a problem of this inverter [8]. Several control techniques have been presented to control the balance of the intermediate level currents in [5] and [6], however the inverter still requires very large in size of the intermediate inductors (>100 mH). Reference [7] presented another circuit configuration of multilevel CSI which is a modified configuration of parallel H-bridge multilevel CSI. However, even 400 mH bulky inductors have been used, large ripples of the smoothing inductor currents are still exist. These ripples will distort the output current waveform of the inverter. Moreover, the cumbersome inductors will be costly and limit the application of the inverter. Reference [9] presented the configuration of single-rating inductor cell multilevel CSI which is the dual

circuit of improved diode-clamped multilevel VSI. The multi-cell and single-rating inductor cell topologies use very large intermediate inductors added in the inverter circuit to obtain the intermediate current levels, instead of the smoothing inductors used for DC current generation. These inductors will cause more losses to the inverter circuits aside from losses caused by the smoothing inductors and inverter's power devices. The inverter circuits with more intermediate inductors will have lower efficiency.

In this paper, a new circuit configuration of multilevel CSI, applying an H-bridge CSI topology and current modules with capabilities of reducing isolated gate drive circuits, reducing inductor size, and with lower inductor conduction losses are presented. The chopper based DC current sources are also presented to control the intermediate level currents using small size of inductors. The operation performance of the proposed multilevel CSI is examined and is validated through some computer simulations. Furthermore, laboratory experimental prototypes of seven-level CSIs were set up to verify the proper operation of the new topology, using the power MOSFETs in series with blocking diodes.

2. CIRCUIT CONFIGURATION AND PRINCIPLE OPERATION

2.1. Operation Principle of Inverter Circuit

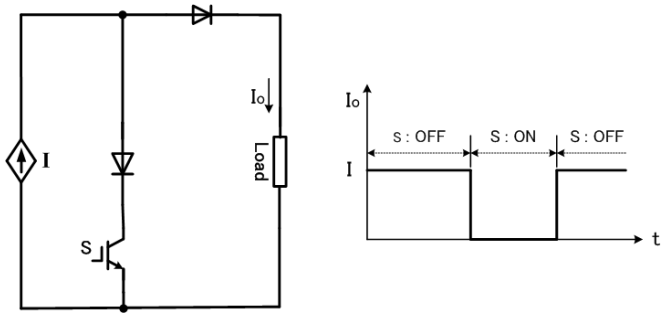

Figure 1. The current-module circuit, and its basic operation [8]

Figure 1 shows the circuit configuration of the current-module, and its basic operation. The current module is constructed by a DC current source with a unidirectional power switch S, and a diode [8]. The novel circuit configuration of the multilevel CSI is derived by connecting a single or more modules with the H-bridge CSI as shown in the schematic diagram of the proposed multilevel CSI in Figure 2 and Figure 3. The current modules work for multilevel output current waveform generation. A five-level current waveform is generated by adding a single current-module, a seven-level current waveform is achieved by connecting two current-modules with the three-level H-Bridge CSI, and so on. The level number of the output current waveform and the count of the current-modules can be obtained from the equation:

$$V = 3 + 2U\,, \tag{1}$$

Where V is the level number of the output current and U is the count of current-modules.

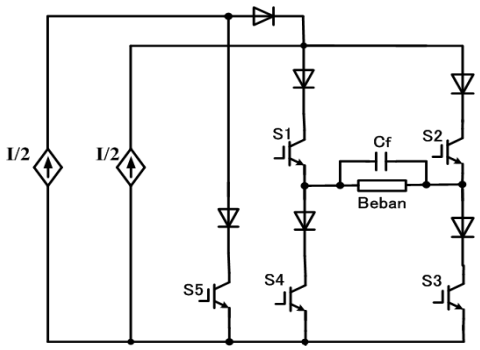

Figure 2. Proposed five-level CSI

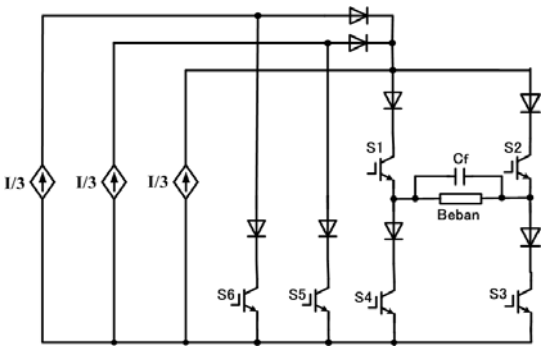

Figure 3. Proposed seven-level CSI

The number of the DC current sources, also representing the number of the smoothing inductors in the real power circuits. For the same amplitude of the output current, the amplitudes of the DC current sources in the proposed multilevel CSI are smaller than the amplitude of the DC current source in the three-level H-Bridge CSI. Moreover, all DC current sources are connected at the same point, hence the isolated DC current sources used in the conventional parallel H-Bridge multilevel CSI are not necessary in this inverter circuit configuration.

As shown in Figure 2 and Figure 3, the power switches S3, S4, S5 and S6 are connected at a common-emitter line or at the same potential point. As a result, even the number of the current-modules increases, the circuit needs only three isolated gate drive circuits. Two isolated gating circuits are used to drive the power switches S1 and S2, and one more to gating the power switches S3, S4, S5 and S6. This feature leads to the reduction in the number of isolated gate drive circuits used in multilevel CSI circuits [8]. The output current levels of the five-level CSI are +I, +I/2, 0, -I/2, and -I current levels. For seven-level CSI, the output current levels are +I, +2I/3, +I/3, 0, -I/3, -2I/3, and -I current levels.

Table 1. Switch states of proposed seven-level CSI

S1	S2	S3	S4	S5	S6	Output current
1	0	1	0	0	0	+I
1	0	1	0	0	1	+2I/3
1	0	1	0	1	1	+I/3
1	0	0	1	1	1	0
0	1	0	1	1	1	-I/3
0	1	0	1	0	1	-2I/3
0	1	0	1	0	0	-I

The switching state combinations required to generate a seven-level current waveform are listed in TABLE 1. The seven-level output current (+I, +2I/3, +I/3, +0, -I/3, -2I/3 and -I current-levels) are generated as follows:

a) Current level +I: S2, S4, S5 and S6 are turned-off, while S1 and S3 are turned-on, making the current +I flow to the load.
b) Current level +2I/3: S2, S4 and S5 are turned-off, while S1, S3 and S6 are turned-on, making the current +2I/3 flows to the load.
c) Current level +I/3: S2 and S4 are turned-off, while S1, S3, S5 and S6 are turned-on, making the current +I/3 flows to the load.
d) Current level 0: S1, S4, S5 and S6 are turned-on, and S2, S3 are turned-off making the current loops for every DC current sources. No current flows to the load.
e) Current level –I/3: S1 and S3 are turned-off, while S2, S4, S5 and S6 are turned-on, making the current –I/3 flows to the load.
f) Current level -2I/3: S1, S3 and S5 are turned-off, while S2, S4 and S6 are turned-on, making the current -2I/3 flows to the load.
g) Current level -I: S1, S3, S5 and S6 are turned-off, while S2 and S4 are turned-on, making the currents –I flows to the load.

Table 2. Comparison between four types of five-level CSIs [8]

Multilevel CSI Types	Multi-cell Type	Paralleled H-bridge Type	Single-rating inductor cell Type	H-bridge with inductor cell type	Proposed Topology
Power switches	8	8	8	8	5
Diodes	8	8	8	8	6
Inductors	3	2	5	2	2
Isolated gate drive circuits	4	4	4	4	3

The count reduction of circuit components attained by using the proposed multilevel CSI is presented in Table 2. This table presents the components count involved to construct a five-level CSI circuits using the proposed five-level inverter circuits, and three other inverter circuits. The total of the inductors includes the smoothing inductors, and the intermediate inductors. The smoothing inductors are the inductors connected to the DC power source to generate the DC current sources. The intermediate inductors are used for the intermediate level currents generation. The reduction in component numbers will be more significant

for higher level CSI. As an example, for seven-level CSI, the paralleled H-Bridge configuration needs twelve power switches, but the proposed seven-level CSI needs only six power switches, 50% reduced, with the same number of inductors. The number of the inductors is fewer if compared with the multi-cell multilevel CSI, and single-rating inductor cell multilevel CSI topologies. A five-level single-rating inductor cell CSI needs five inductors, the proposed five-level CSI needs only two inductors, 60% reduced.

2.2. DC Current Source Generation

The DC current sources are absolutely required in the current-source inverter type. In this paper, the DC current-sources are acquired by using buck-chopper circuits connected with a DC power source [8], [10], [11]. The DC power source (V_{in}) can be a photovoltaic system, fuel-cell, battery or rectifier circuits. The chopper works to provide a constant DC current source for the H-Bridge CSI and current-module circuits. The chopper circuit is composed by a power switch, an inductor (choke) and a power diode. The controlled power switch works to controll the smoothing inductor's current, and to reduce the smoothing inductor size. The power diode (D_F) is applied to keep continuous current path of the smoothing inductor's current. Figure 5 and Figure 6 show the configurations of five-level and seven-level CSIs with DC current generation circuits. It should be noted that only a single DC power source (V_{in}) is connected to circuits to obtain multiple non-isolated DC current-sources. The proposed multilevel CSI does not need isolated DC current sources.

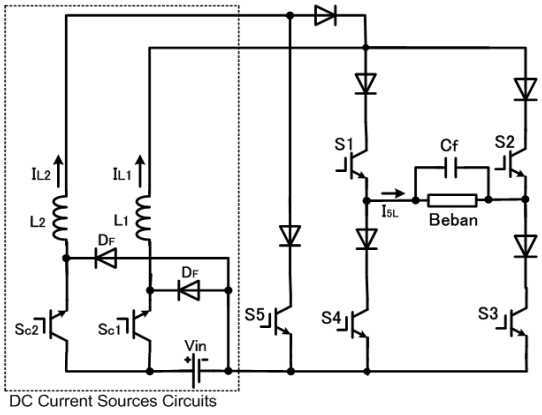

Figure 5. Five-level CSI with DC current-sources circuits [8]

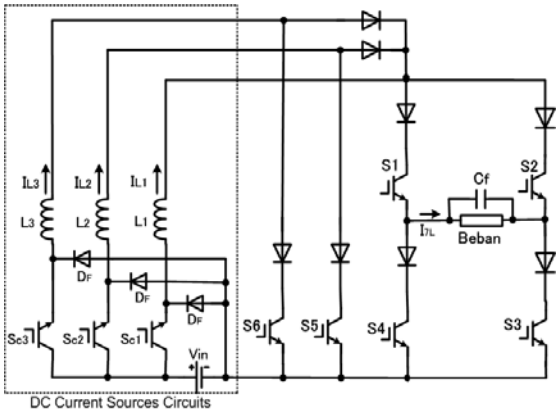

Figure 6. Seven-level CSI with DC current sources circuits [8]

2.3. Conduction Losses of Inductors

This section discusses the inductor's conduction losses in multilevel CSIs. From author's literature search result, the size of the inductors used in the conventional multilevel CSI topologies is very large, more than 100 mH [1]-[7], [9]. These bulky inductors will be the main cause of losses which cause the efficiency of the multilevel CSI much lower than the multilevel VSI. In the proposed topology, if the amplitude of the *V*-level output current is I, and the number of the current-module is *U*, the current flowing through the smoothing inductor I_{LN} is expressed as:

$$I_{LN} = \frac{I}{(U+1)}, \tag{2}$$

If the smoothing inductor has resistance R_L, the inductor's conduction losses (P_{Lc}) caused by this current is expressed as:

$$P_{Lc} = \left(\frac{I}{U+1}\right)^2 R_L \tag{3}$$

The total conduction losses due to the inductors in a *V*-level CSI ($P_{Lc\text{-}V}$) can be calculated as:

$$P_{Lc-V} = (U+1)\left(\frac{I}{U+1}\right)^2 R_L = \frac{I^2 R_L}{U+1} \quad (4)$$

In the five-level CSI, the current flowing through the smoothing inductors is half the amplitude of the five-level output current. In the seven-level CSI configuration, the amplitude of the smoothing inductor currents is one third of the seven-level output current, and so forth. The higher the level-number of the output current leads to smaller currents flowing through the smoothing inductors as expressed in (2). Therefore, it reduces the total conduction loss (P_{Lc-V}) of the inductors as shown in Figure 7. The total inductor's conduction loss of the five-level CSI (P_{Lc-5}) is half the inductor's conduction loss of the three-level H-Bridge CSI (P_{Lc-3}). The total inductor's conduction loss of seven-level CSI (P_{Lc-7}) is one third of the inductor's conduction loss of the H-Bridge CSI, and so forth [8].

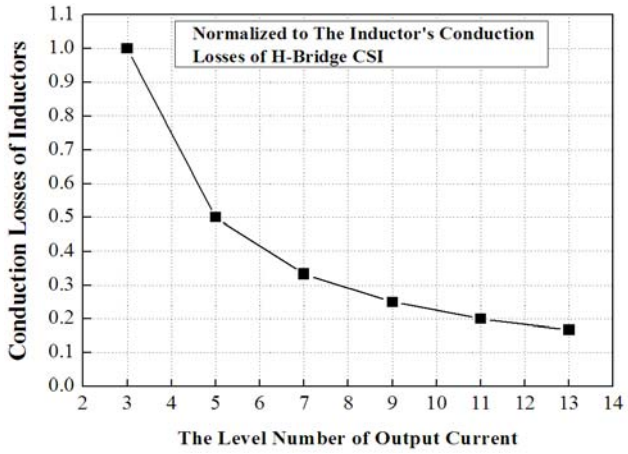

Figure 7. Characteristics of conduction loss of the smoothing inductors [8]

2.4. Current Regulator and Pulse Width Modulation (PWM) Tecnique

Proportional integral (PI) current regulators are separately employed to regulate the smoothing inductors's current (I_L). The switching signals of the chopper's power switches are produced by comparing the error of the measured smoothing inductor's currents, and a sawtooth carrier waveform using comparator circuits. The ouput signals will determine the operation of the chopper's controlled power switches to attain stable DC current-sources of the inverter circuits [8]-[11].

For the modulation technique, a multi-carrier with level-shifted based sinusoidal pulse width modulation (PWM) strategy is applied to control the inverter's power switches. Some triangular carrier waveforms with the same phase and frequency are utilized in this technique. The fundamental output current frequency of the inverter is determined by the frequency of the modulated signal (a reference sinusoidal waveform). The switching frequency of the inverter's power switches is defined by the frequency of triangular carrier waveforms. A total, *(V-1)* of triangular carrier waveforms are required in the *V*-level output current waveform generation of the inverter circuits [8]-[14].

Table 3. Test parameters of inverter circuits

Smoothing inductors	600 □H
DC power source voltage	160 V
Switching frequency of inverter	22 kHz
Filter capacitor	5 □F
Load	R = 6.5 Ω , L =1.2 mH
Output current frequency	60 Hz

3. Computer Simulation and Experimental Test Results

The operation of the proposed topology is tested through computer simulation and experimental prototype in laboratory. The seven-level CSI configuration as shown in Figure 6 was tested by using computer simulation with PSIM software. The parameters of tested the inverter circuits are listed in Table 3. Figure 8 shows the computer simulation results of the seven-level CSI. The seven-level and the load current waveforms are presented in this figure. Figure 9 shows the DC current waveforms flowing through the 600-µH smoothing inductors L_1, L_2 and L_3. The amplitudes of the smoothing inductor currents are well balanced for all smoothing inductors I_{L1}, I_{L2} and I_{L3} [8].

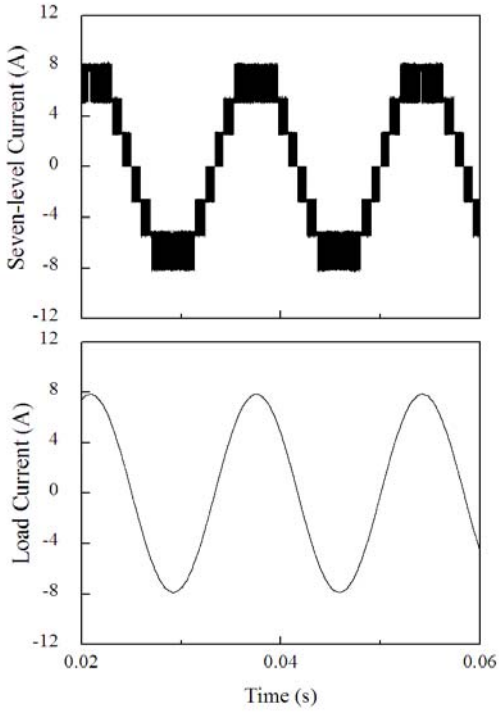

Figure 8. Seven-level PWM current and load current waveforms

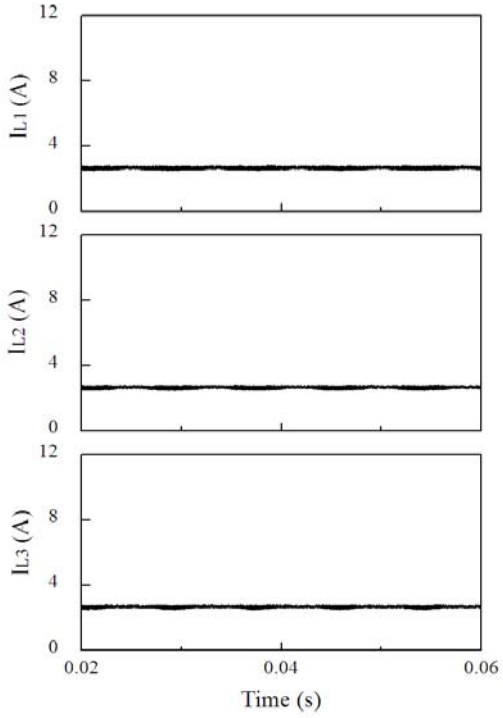

Figure 9. DC current waveforms of smoothing inductors

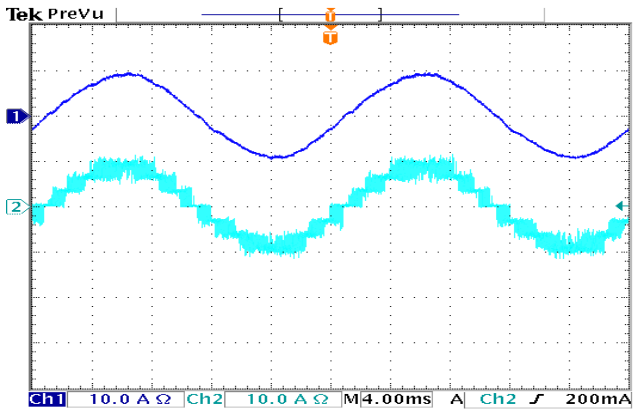

Figure 10. Experimental test results of load current and seven level PWM current waveforms

Furthermore, in order to verify the proposed seven-level CSI configurations experimentally, laboratory prototypes seven-level CSI was constructed with IXFK90N30 power MOSFETs in series with DSEI120-06A fast recovery diodes. The low on-resistance (R_{DSon}) of the power MOSFETs, and low forward

voltage drop (V_F) of diodes are chosen in order to minimize the conduction losses. The on-resistance of the power MOSFETs and the forward-voltage drop of the diodes are 33 mΩ and 1.3 V(max), respectively. The implemented circuit specifications are identical with the computer simulation parameters in Table 3. The DC resistance of the 0.6 mH smoothing inductors is 26.5 mΩ obtained from measurement. The control circuits were built using analog circuits. The opto-isolator based gate driver circuits are used in the prototypes.

Figure 10 shows the experimental waveforms of the seven-level CSI, i.e., showing the load current and PWM seven-level current waveforms at modulation index of 0.95. As can be seen in the figure, a low distorted sinusoidal load current waveform is obtained after filtering by a small 5-μF filter capacitor.

4. CONCLUSION

In this paper, a novel circuit configuration of multilevel current-source inverter has been presented and verified. In this new topology, a three-level H-bridge CSI is connected with a single or more current-modules to generate the multilevel output current waveform. In order to control the intermediate current levels and to reduce the size of the inductors used in the multilevel CSI, chopper circuits with proportional integral (PI) current regulator are implemented to generate the DC current-sources of the inverter. Using the presented topology and from test results of the seven-level CSI, a sinusoidal load current waveforms with less distortion, less components of inverter, smaller size of smoothing inductors and with lower inductor's conduction losses can be achieved.

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BIOGRAPHIES OF AUTHORS

Suroso received the B. Eng. degree in electrical engineering, from Gadjah Mada University, Indonesia in 2001, and the M. Eng. degree in electrical and electronics engineering from Nagaoka University of Technology, Japan in 2008. He was a research student at electrical engineering department, Tokyo University, Japan from 2005 to 2006. He earned the Ph.D degree in energy and environment engineering department, Nagaoka University of Technology, Japan in 2011.He was a visiting researcher at electrical and electronics engineering department, Shizuoka University, Japan from 2009 to 2011. Currently, He is an assistant professor at department of electrical engineering, Jenderal Soedirman University, Purwokerto, Central Java, Indonesia.His research interest includes power converters, and its application in renewable energy conversion.

Toshihiko Noguchi was born in 1959. He received the B. Eng. degree in electrical engineering from Nagoya Institute of Technology, Nagoya, Japan, and the M. Eng. and D. Eng. degrees in electrical and electronics systems engineering from Nagaoka University of Technology, Nagaoka, Japan, in 1982, 1986, 1996, respectively. In 1982, he joined Toshiba Corporation, Tokyo, Japan. He was a Lecturer at Gifu National College of Technology, Gifu, Japan, from 1991 to 1993 and a Research Associate in electrical and electronics systems engineering at Nagaoka University of Technology from 1994 to 1995. He was an Associate Professor at Nagaoka University of Technology from 1996 to 2009. He has been a Professor at Shizuoka University since 2009. His research interests are static power converters and motor drives.