

## A Novel Hybrid Negative Half Cycle Biased Modulation Scheme for Cascaded Multilevel Inverter

R. Hemanthakumar, V. RaghavendraRajan, C.S. Ajin Sekhar, M. Sasikumar

Jeppiaar Engineering College, Anna University, Chennai – 600 119, India

---

### Article Info

#### Article history:

Received Jan 29, 2014

Revised Mar 10, 2014

Accepted Mar 25, 2014

---

#### Keyword:

Hybrid Negative Half Cycle Biased Modulation Scheme (HNHCBM)

5-level Cascaded Multilevel Inverter

Circulating pulses

Circulating pulse width modulation

Low harmonics

Switching loss

---

### ABSTRACT

This paper proposes a new Modified hybrid modulation scheme for cascaded multilevel inverter. The proposed method employs novel single carrier sinusoidal pulse width modulation with its negative cycle biased (HNHCBM) for reducing switching losses when compared to other sinusoidal modulation methods using a hybrid scheme. This scheme is a derivative of various single carrier sinusoidal pulse width modulation scheme and main advantages are reduced harmonics, enhanced output voltage, reduced power loss in the series cells and ease of implementation. The simulation results are analysed with matlab/simulink and compared with experimental results obtained using 5-level inverter and the results are summarized.

Copyright © 2014 Institute of Advanced Engineering and Science.

All rights reserved.

---

### Corresponding Author:

R.Hemanthakumar

Department of Electrical and Electronics Engineering,

Jeppiaar Engineering College,

Rajiv Gandhi salai,

Chennai – 600 119, India

Email: hemanthakumar18@gmail.com

---

## 1. INTRODUCTION

Multilevel inverters are gaining importance mainly due to reduced harmonics content in its output. Traditional voltage source inverters (VSI) fed systems suffer from high harmonics, electromagnetic interference in the output. This led to the development of concept of multilevel inverter which offers less harmonic output voltage. The major challenges in the development of multilevel inverter are reducing the increase in number of switches for each level increase of output, less harmonics, low electromagnetic interference, low switching losses and high efficiency. The basic types of multilevel inverters are diode clamped, flying capacitor and cascaded multilevel inverter [1]-[4]. Apart from these are also other topologies like reverse voltage topology [5], sublevel inverter [6], etc. Various control techniques [7] for multilevel inverters have been proposed. Among the above, due to the advantage of ease in increase of level, no capacitor balancing problem and reliable (cell like) structure, cascaded multilevel inverter is applied to medium and high power applications as well as renewable energy fed applications [8]-[10].

Several sinusoidal modulation techniques like Alternative Phase Opposition Disposition (APOD), Phase Shift Carrier (PSC), multilevel sinusoidal-modulation (MSPWM), Phase shifted carrier PWM (PSC PWM), and Single Carrier Sinusoidal (SCSPWM) [11] etc have been proposed already. Here a new hybrid modulation technique for harmonic reduction and reduced switching losses is proposed. This paper first discusses about the basic principle behind the technique, then hybrid switching scheme for reducing stress

on switches as well as its losses using 5-level cascaded multilevel inverter, and extension to N-level systems is discussed. At last the same is simulated and verified with experimentation results.

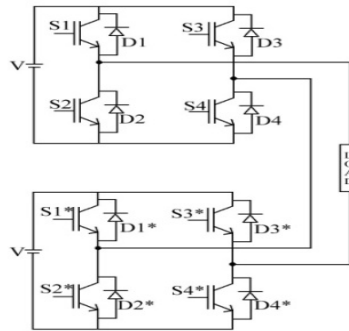


Figure 1. 5-level Cascaded multilevel inverter circuit

## 2. BASIC PRINCIPLE OF MODULATION TECHNIQUE

The basic principle behind the proposed Negative Half Cycle Biased Modulation Scheme (NHCBM) is explained using the 5-level cascaded multilevel inverter Figure 1. The modulating signal is generated with respect to the carrier signal of amplitude  $A_{tr}$ . If the amplitude of the modulating sinusoidal signal is  $A_m$ , then the modulating signal is generated using the following formulas,

$$U_{m\_p1} = A_m \sin \omega t \quad (1)$$

$$U_{m\_n1} = A_m \sin \omega t + A_{tr} \quad (2)$$

$$U_{m\_p2} = A_m \sin \omega t - A_{tr} \quad (3)$$

$$U_{m\_n2} = A_m \sin \omega t + 3A_{tr} \quad (4)$$

Equations 1-4 represent the positive cycle and negative cycle of two modulating signal. The resulting modulating and carrier waveforms for 5-level inverter are shown in Figure 2.

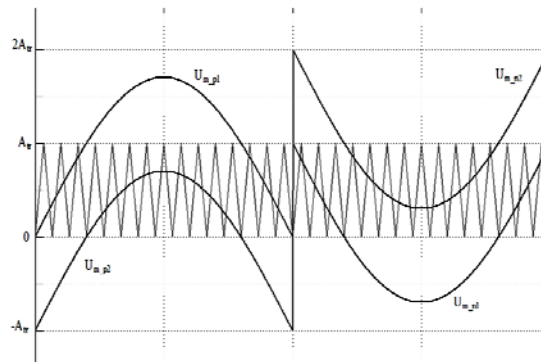


Figure 2. Proposed Negative Half Cycle Biased Modulation (NHCBM) Scheme

Therefore in case of N-level inverter, the positive and negative cycle of the modulating signal is given by:

$$U_{m\_pN} = A_m \sin \omega t - ((N-3)/2)A_{tr} \quad (5)$$

$$U_{m\_nN} = A_m \sin \omega t + (N-2)A_{tr} \quad (6)$$

The modulation index (M) is given by:

$$A_m = (N-1)MA_{tr}/2 \tag{7}$$

Figure 2 is due to modulation index of  $M=8$ . It is noted that the proposed modulation signal has negative cycle biased based on the level of operation and can be easily applied to N-level system

### 3. HYBRID SWITCHING SCHEME

The block diagram of hybrid modulation switching scheme is shown in Figure 3 for 5-level inverter. This scheme is based on the main aim of circulating the switching pulses between the cascaded multilevel inverter cells. Four kinds of signals A-D is generator in the base modulation generator and the pulses for switches are generated in hybrid modulation controller for the each cell separately. Base PWM circulation block is used to modulate the signal C and D which are the signal generated using the proposed modulation scheme.

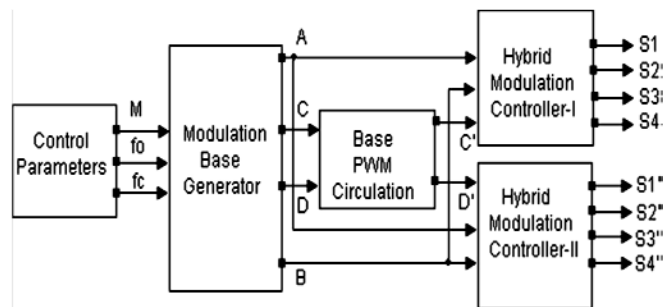


Figure 3. Block diagram of Hybrid switching scheme

#### 3.1. Base Modulation Signal Generator

The block diagram of base modulation signal generator is given in Figure 4. Base modulation generator generates four signals A-D based on the control parameters like modulation index ( $M$ ), output voltage frequency ( $f_o$ ) and carrier frequency ( $f_c$ ).

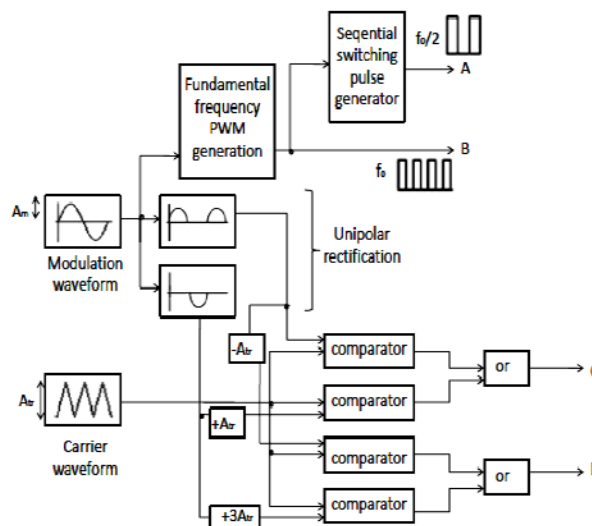


Figure 4. Block diagram of Base modulation signal generator

The signal A and B is independent of the number of level of inverter as it is based on the output frequency ( $f_o$ ). The signal A and B is a square wave generated with 50 percent pulse width and frequency ( $f_o$ ) and ( $f_o/2$ ) respectively and is independent of the number of levels.

The signal C and D are modulated signals from the proposed modulation scheme as already discussed in case of 5 level inverter in previous section.

### 3.2. Base PWM Circulation and Hybrid Modulation Controller

With the aim of reducing switching losses base PWM circulation can be implemented using multiplexer as shown in Figure 5. The signals C and D are circulated at the rate of frequency  $f_o/4$  to produce signals C' and D' as output for 5-level inverter.

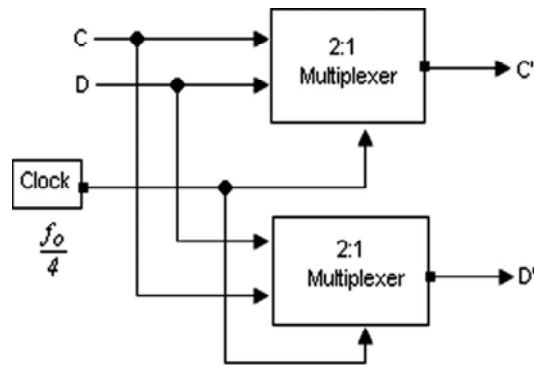


Figure 5. Base PWM circulation schemes for 5-level inverter

This scheme can be implemented to N-level by circulating each signal at the rate of  $f_o/(N-1)$ . The output signals C' and D' are combined logically with A and B in the hybrid controller to generate switching pulses for the inverter. The logics used for 5-level inverter is shown below:

$$\begin{array}{ll}
 S1 = ABC' + \bar{A}B & S1' = ABD' + \bar{A}B \\
 S2 = \bar{A}BC' + \bar{A}\bar{B} & S2' = \bar{A}BD' + \bar{A}\bar{B} \\
 S3 = \bar{A}\bar{B}C' + \bar{A}\bar{B} & S3' = \bar{A}\bar{B}D' + \bar{A}\bar{B} \\
 S4 = \bar{A}BC' + AB & S4' = \bar{A}BD' + AB
 \end{array}
 \quad \text{and}$$

From the above logics it can be observed that these logics can be extended to N-level inverter easily by just replacing the modulated signal generated in each set of equations.

## 4. SIMULATION RESULTS

The proposed technique is simulated using Matlab software and the results are studied below at switching frequency of 100 KHz. The simulink circuit diagram of the 5-level inverter is shown below in Figure 6.

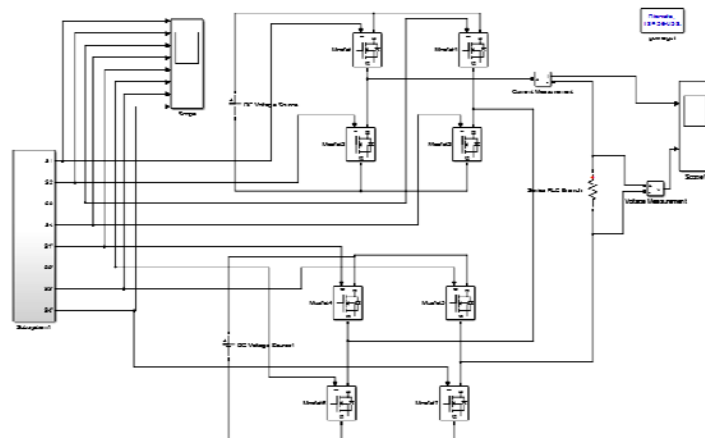


Figure 6. Simulink construction cascaded 5-level inverter

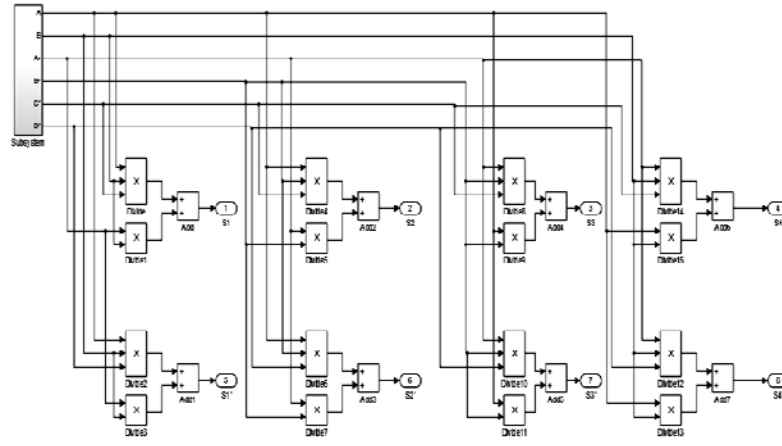


Figure 7. Hybrid controller logics implementation

The hybrid modulation controller logics are implementation in simulink is shown in Figure 7.

The switching pulses S1 to S4 and S1' to S4' generated from the logics are shown in Figure 8. From the figure it is observed that the pulses contain both fixed pulse width modulation (FPWM) and Negative Half Cycle Biased Modulation (NHCBM) signals forming a hybrid combination. The output voltage is applied to load resistance of 10ohms and each of cascaded cells has input voltage of 200V. The output voltage and current waveforms of the inverter with modulation index (M=0.8) are shown in Figure 9.

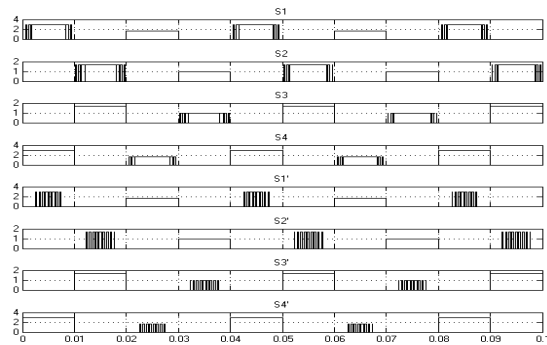


Figure 8. Hybrid modulated switching pulses

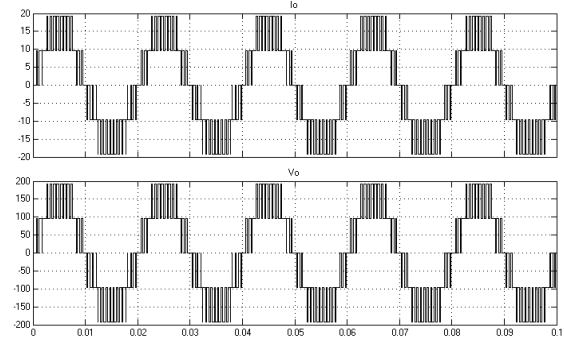


Figure 9. Output current (Io) and output voltage (Vo) waveforms

The Total Harmonic Distortion analysis (THD) of the proposed scheme reveals that the harmonics is reduced to nearly half from the results of THD shown in Figure 10 and 11.

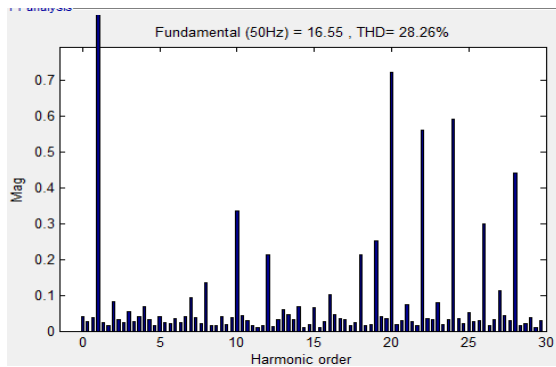


Figure 10. THD in output voltage due to proposed

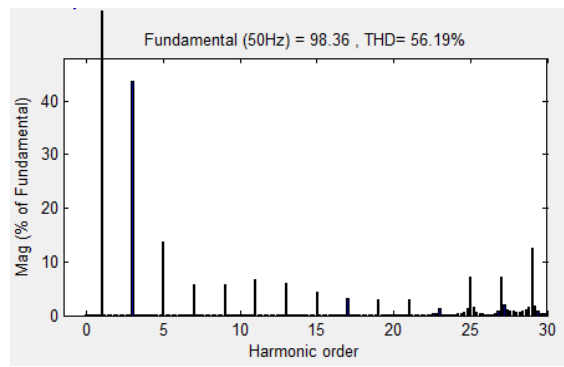


Figure 11. THD in output voltage without Hybrid

hybrid scheme (HNHCBM) scheme ((NHCBM)  
 The variation of Total Harmonic Distortion (THD) with the modulation index (M) is plotted and is shown in Figure 12.

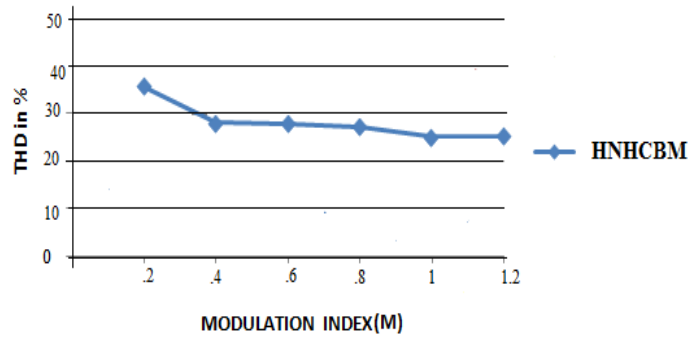


Figure 12. Modulation index (Vs) THD

From the graph and THD analysis, it is clear that the proposed hybrid method is most efficient SPWM method.

**5. HARDWARE IMPLEMENTATION**

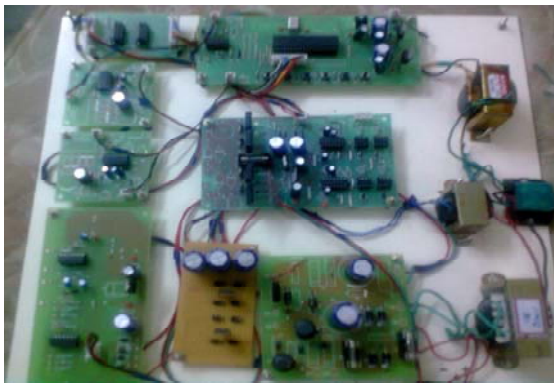


Figure 13. Hardware setup of cascaded five level inverter

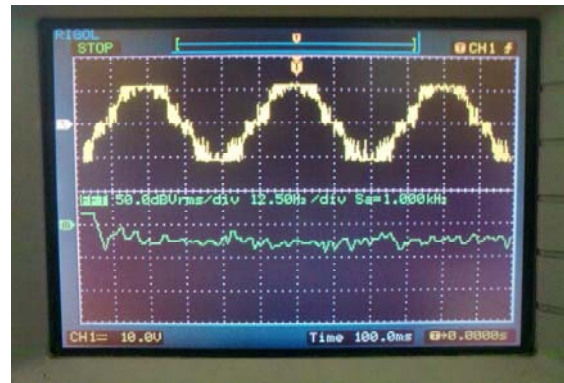


Figure 14. DSO measured five level output voltage



Figure 15. Harmonic spectrum of output voltage

The Proposed Hybrid Negative Half Cycle Biased Modulation Scheme (HNHCBM) is implemented in hardware using FGA25N120 IGBT for the full bridge inverter and CSD100060 diode as the switching devices and the gate pulses are generated using the TMS320F2407 controller. The experimental setup is

shown in Figure 13 and the output voltage waveform obtained across the load resistance 10ohm is shown in Figure 14. From Figure 13 and 14 it is evident that the output voltage waveform obtained during experimental analysis is similar to simulation and the harmonic spectrum of the output obtained is shown in Figure 15. From the practical results it is evident that this method is efficient than normal SPWM methods.

## 6. CONCLUSION

In this paper, Negative Half Cycle Biased Modulation Scheme (NHCBM) is proposed and implemented using hybrid modulation (HNHCBM) technique. The harmonics spectrum of the output voltage for R load is analysed and the output obtained during NHCBM and HNHCBM is compared. From the above comparison it is evident that output voltage harmonics is improved using the hybrid technique. The Harmonic performance of this proposed scheme is plotted against modulation index and it seems to be efficient. PWM circulation in hybrid scheme leads to balanced power dissipation in the switches within the cell as well as series connected cells. This scheme can be easily extended to higher voltage levels and to 3 phase systems.

## REFERENCES

- [1] E Babaei. A cascade multilevel converter topology with reduced number of switches. *IEEE Trans. Power Electron.*, 2008; 23(6): 2657–2664.
- [2] Nabae, I Takahashi, H Akagi. A new neutralpoint-clamped PWM inverter. *IEEE Trans. Ind. Appl.*, 1981; IA-17(5): 518-523.
- [3] TA Meynard, H Foch. *Multi-level choppers for high voltage applications*. Proc. Eur. Conf. Power Electron. Appl., 1992; 2: 45–50.
- [4] C Govindaraju, K Baskaran. Efficient hybrid carrier based space vector modulation for cascaded multilevel inverter. *Journal of Power Electronics*. 2010; 10(3): 277–284.
- [5] K Srinivas, K Rameshbabu, CH Rambabu. A New Multilevel Topology for Induction Motor Drive. *in ijetae*. 2012; 2(12).
- [6] R Kalaiarasi, T Manokaran. A Novel Topology of Reduced Components by using Sub Multilevel Converter for DC Motor. *Journal of Advanced Technology in Engineering*. 2012; 1(1): 54-56.
- [7] R Seyezhai, Banuparvathy Kalpana. Design and Development of Hybrid Multilevel Inverter employing Dual Reference Modulation Technique for Fuel Cell Applications. *International Journal of Power Electronics and Drive Systems*. 2011; 1(2): 104-112.
- [8] G Nageswara Rao, P Sangameswara Raju, K Chandra sekhar. Multilevel Inverter Based Active Power Filter for harmonic Elimination. *International Journal of Power Electronics and Drive Systems*. 2013; 3(3): 271-278.
- [9] Sasikumar M, ChenthurPandian S. Modeling and Analysis of Cascaded H-Bridge Inverter for Wind Driven Isolated Self – Excited Induction Generators. *International Journal on Electrical Engineering and Informatics (IJEI)*. 2011; 3(2): 132-145.
- [10] Muhammad Jamil. Comparison of Multilevel Inverters for the Reduction of Common Mode Voltage. *International Journal of Power Electronics and Drive System (IJPEDS)*. 2013; 3(2): 170~178.
- [11] BP McGrath, DG Holmes. Multicarrier PWM strategies for multilevel inverters. *IEEE Trans. Ind. Electron.*, 2002; 49(4): 858-867.

## BIOGRAPHIES OF AUTHORS



Mr. R. Hemantha Kumar has received the Bachelor degree in Electrical and Electronics Engineering from Thangavelu Engineering College, Anna University, India in 2011. He is pursuing Master of Engineering in Power Electronics and Drives from Jeppiaar Engineering College, Anna University, India. His area for interest includes in the field of Power Converters for Renewable energy, PWM techniques and multilevel converters.



V. RaghavendraRajan has received the Bachelor degree in Electrical and Electronics Engineering from Aurora's Seethaiah engineering college, Jawaharlal Nehru University, Hyderabad, India in 2011. He is pursuing Master of Engineering in Power Electronics and Drives from Jeppiaar Engineering College, Anna University, India. His area for interest includes in the field of Wind Energy and PWM techniques in converters.



Mr.C.S.Ajin Sekhar received the B.E degree in electrical and electronics engineering from SRR engineering College, Anna University, Chennai 2012, India, He is pursuing Master of Engineering in Power Electronics and Drives from Jeppiaar Engineering College, Anna University, India. His area for interest includes in the field of Renewable Energy, Power Converters, AC-AC Converters and PWM techniques.



Dr.M.Sasikumar has received the Bachelor degree in Electrical and Electronics Engineering from K.S.Rangasamy College of Technology, Madras University, India in 1999, and the M.Tech degree in power electronics from VIT University, in 2006. He has obtained his Ph.D. degree from Sathyabama University, Chennai in 2011. Currently he is working as a Professor and Head in Jeppiaar Engineering College, Chennai Tamilnadu, India. His area of interest includes in the fields of wind energy systems, Hybrid systems and power converter and soft-switching techniques. He is a life member of ISTE.