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A Low Cost Single-Switch Bridgeless Boost PFC Converter

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ABSTRACT

This paper proposes the single-switch bridgeless boost power factor correction (PFC) converter to achieve high efficiency in low cost. The proposed converter utilizes only one active switching device forPFC operation as well as expecting higher efficiency than typical boost PFC converters. On the other hand, the implementation cost is less than traditional bridgeless boost PFC converters, in where two active switching deivces are necessary. The operational principle, the modeling, and the control scheme of the proposed converter arediscussed in detail. In order to verify the operation of the proposed converter, a 500W switching model is built in PSIM software package. The simulation results show that the proposed converter perfectly achieves PFC operation with only a single active switch.

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1. INTRODUCTION

A power factor correction (PFC) converters have been employed in many applications such as power supplies, battery chargers, motor drive applications, and so on [1]-[9]. Traditional PFC converters usually employs a diode bridge and an active switching device such as IGBTs and MOSFETs. Recently, bridgeless PFC converters which do not requirehaving a diode bridge have been studied, because the converter efficiency can be improved by eliminating the diode bridge. However, typical bridgeless PFC converters require two active switches to conduct an input current according to the polarity of the input voltage.This increases the implementatin cost including the gate driver circuitries and snubbers. Moreover, increasing the number of active switching devices also decreases the reliability of the entire power stage. In terms of electromagnetic inteference (EMI), it has been known that bridgeless topologies are worse than traditional boost PFC topologies with a diode bridge. In order to overcome this disadvantage, semi-bridgeless PFC converters have been proposed [10], [11]. These semi-bridgeless PFC converters have equivalent EMI characteristics with traditional boost PFC converter with a diode bridge, but still they employ two active switches.

In this paper, a low cost single-switch bridgeless PFC converter is proposed. The proposed converter utilizes a single active switch, and it operates in entire electrical cycle. So, the implementation cost can be reduced, and the utilization of the switch can be increased. Compared to the traditional semi-boost PFC converter, the proposed converter employs two more diodes to avoid a short ciruit condition, but reduce the number of the active switch whose realization cost is higher than several passive switching components such as a diode. So the total cost saving can be achieved. The EMI characteristics of the proposed converter are basically identical to traditional semi-bridgeless PFC topologies. This paper consists of following sections. In section 2, the single-switch bridgeless PFC topology is proposed, and its operation mode and the inductor current equation are analyzed in detail. In section 3, the control model of the proposed converter is discussed,

and its derivation procedure is explained. The control strategy is also introduced in this section. The numerical transfer function and the simulation model of an example case are discussed in section 4. Also the loop-gain analysis with the designed controllers are performed. The simulation results are also shown in the section to verify the performance of the proposed converter. Finally, the conclusion is made in the last section.

2. PROPOSED SINGLE-SWITCH BRIDGELESS BOOST PFC CONVERTER

Figure 1 shows the topology of the proposed single-switch bridgeless boost PFC converter. For the front-end stage, only one active switching device $Q_1$is employed, and it conducts in full electrical cycle. Since Q_1 operates in the entire cycle, the blocking diodes D_3 and D_4 are necessary to avoid confliction of positive and negative half cycles.

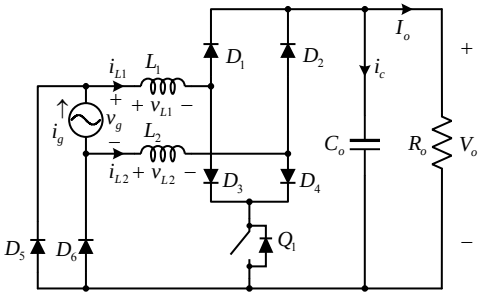
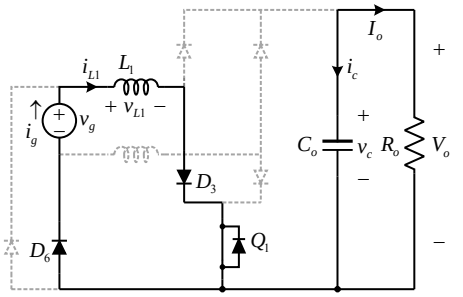
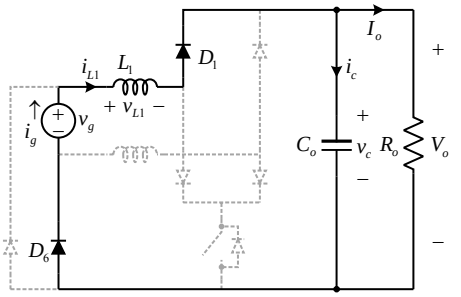


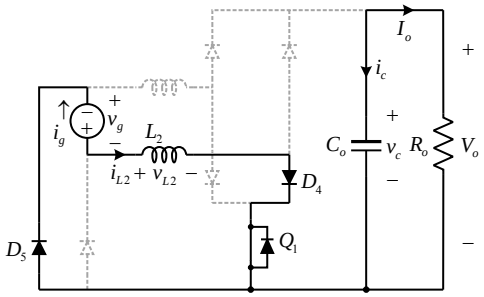
Figure 1. Proposed single-switch bridgeless boost PFC converter



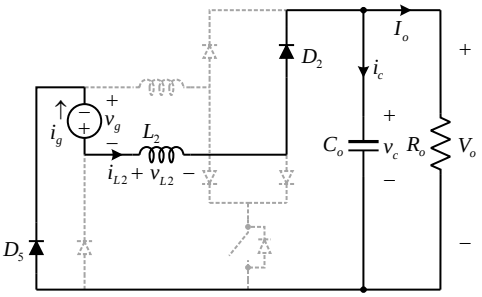
(a) whenv_g is positive, and Q_1 is turned on



(b) whenv_g is positive, and Q_1 is turned off



(c) whenv_g is negative, and Q_1 is turned on



(d) whenv_g is negative, and Q_1 is turned off

Figure 2. Operation of the proposed converter

Figure 2 illustrates the operation modes of the proposed converter according to the polarity of the input voltage $v_g$and the status of Q_1. In figure 2(a), v_g is positive, and Q_1 is turned on. In this case, the input current i_g flows through L_1, D_3, Q_1, and D_6, and D_1, D_2, D_4, D_5 are blocked. The input energy is stored in L_1 while the load R_o is supplied from the energy charged in the dc-link capacitor C_o. By ignoring the voltage drops induced by D_3, D_6, and Q_1, the voltage across L_1 is written as follows:

$$v_{L1} = L_1 \frac{di_{L1}}{dt} \tag{1}$$

For the switch off-stage in positive v_g, the equivalent circuit is shown in Figure 2(b). Here, $i_g$flows via L_1, D_1, C_o, R_o, and D_6. The active switch Q_1 and other diodes do not conduct.In this stage, the energies stored in L_1 and from the source v_g are simultaneously transferred to the dc-link and the load. This operation is exactly same to typical boost converters. As similar to the previous one, the inductor voltage is represented as (2).

$$v_{L1} = v_g - V_o = L_1 \frac{di_{L1}}{dt} \tag{2}$$

Note that the inductor current i_{L1} is the same to i_g for the positive half cycle. For the negative half cycle, D_4 or D_2 is turned on according to the status of Q_1. Unlike the previous two cases, D_5 and L_2 are conducting as in Figures 2(c) and 2(d). In these modes, the magnitude of i_{L2} is identical to i_g, but its direction is opposite according to the definition in Figure 2. The expressions of i_{L2} are represented in (3) and (4).

$$v_{L2} = -v_g = L_2 \frac{di_{L2}}{dt} \tag{3}$$

$$v_{L2} = -v_g - V_o = L_2 \frac{di_{L2}}{dt} \tag{4}$$

For the capacitor voltage, only the status of Q_1 is considered without referring the polarity of the input voltage. When Q_1 is turned on, the capacitor current is written as (5).

$$i_c = C_o \frac{dv_c}{dt} = -I_o = -\frac{v_c}{R} \tag{5}$$

The capacitor current in the off stage of Q_1 is represented as below:

$$i_c = C_o \frac{dv_c}{dt} = \left(i_{L1} \text{ or } i_{L2}\right) - I_o = i_g - \frac{v_c}{R} \tag{6}$$

3. MODELING AND CONTROL OF THE PROPOSED CONVERTER

3.1. Modeling of the Duty-to-input Current

For PFC converter control, usually two control loops, the input current and the dc-link voltage, are necessary. For the input current control loop design, the duty-to-inductor current model should be evaluated. In order to simplify the model, let's assume that L_1 and L_2 have the same values as L_g. Then, Equation (1) and (3) are the same as well as Equations (2) and (4) are identical. Then, the well-known state-space averaging technique can be applied to obtain the control models [12]. By using Equations (1) and (5), the state equation when Q_1 is turned on can be written as follows:

$$\begin{bmatrix} \frac{di_g}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = A_0 \begin{bmatrix} i_g \\ v_c \end{bmatrix} + B_0 v_g, \qquad A_0 \equiv \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{R_o C_o} \end{bmatrix}, \qquad B_0 \equiv \begin{bmatrix} \frac{1}{L_g} \\ 0 \end{bmatrix} \tag{7}$$

On the other hand, the state equation when Q_1 is turned off is also derived as (8) by using (2) and (6).

$$\begin{bmatrix} \frac{di_g}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = A_1 \begin{bmatrix} i_g \\ v_c \end{bmatrix} + B_1 v_g, \qquad A_1 \equiv \begin{bmatrix} 0 & -\frac{1}{R_o} \\ \frac{1}{C_o} & -\frac{1}{R_o C_o} \end{bmatrix}, \qquad B_1 \equiv \begin{bmatrix} \frac{1}{L_g} \\ 0 \end{bmatrix} \tag{8}$$

Let's define constant matrices *A* and *B* for state-space analysis as:

$$A \equiv A_0 d + A_1 (1-d), \qquad B \equiv B_0 d + B_1 (1-d) \tag{9}$$

Where *d* represents the duty reference. After that the dc components of the states i_g and v_c can be derived as follows by utilizing the matrices *A* and *B*.

$$X = -A^{-1} B V_g \tag{10}$$

Where *X* is the dc component vector, and V_g is the peak value of v_g. By applying Laplace transform, (11) is obtained as follows:

$$\begin{bmatrix} \frac{i_g(s)}{d(s)} \\ \frac{v_c(s)}{d(s)} \end{bmatrix} = (sI - A)^{-1} \left[(A_0 - A_1) X + (B_0 - B_1) V_g \right], \qquad I \equiv \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \tag{11}$$

By solving (11), the duty-to-inductor current and the duty-to-capacitor voltage models are derived as follows:

$$\frac{i_g(s)}{d(s)} = \frac{V_g \left(R_o C_o s + 2 \right)}{L (1-d) \left(R_o C_o s^2 + s + (1-d)^2 \right)} \tag{12}$$

$$\frac{v_c(s)}{d(s)} = \frac{R_o V_g \left((1-d)^2 - s \right)}{L (1-d)^2 \left(R_o C_o s^2 + s + (1-d)^2 \right)} \tag{13}$$

3.2. Control Strategy

As described before, the voltage and the current control loops as in Figure 3 are necessary for the PFC converter. Two proportional-integral (PI) controllers are employed for each control loop. In order to improve the current control performance, the duty feed-forward term is applied. Thanks to the feed-forward term, the integral portion in the PI current controller is reduced, so that the dynamic property can be improved. For the voltage controller, a 120Hz bandstop filter is employed to filter out 120Hz periodic voltage ripple caused by the single-phase power fluctuation phenomenon [13]. By doing so, the dynamic property of the voltage control loop can be improved without introducing unnecessary 120Hz component in the current reference.

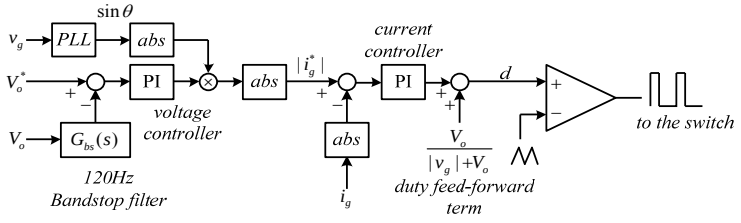


Figure 3. The control scheme of the proposed converter

4. SIMULATION STUDY

4.1. Power Circuit Switching Model

Figure 4 shows the developed switching model in PSIM. In the switching model, both the 15 percent and 85 percent of the rated load are configured. In order to see the dynamic performance of the entire control system, the 85 percent load can be connected or disconnected in step. The parameters of the power circuit is summarized in Table 1. All active and passive switching devices are assumed as ideal elements, so their voltage drops are ignored. The time step for the simulation is selected as 250nsec.

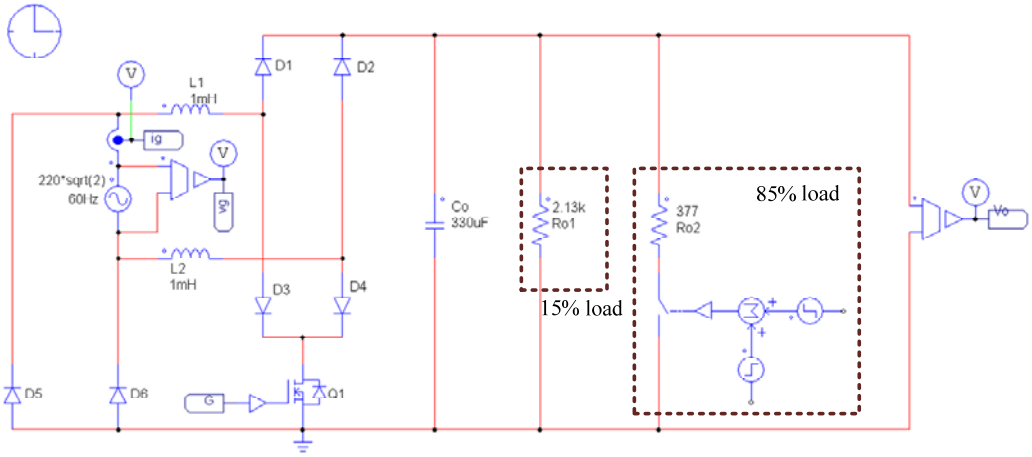


Figure 4. Developed power circuit in PSIM

Table 1. The Parameters for the Simulation

Contents	Values
Input inductance L_g	1 mH
Output capacitance C_o	330 μF
Input root-mean-square (RMS) voltage V_{rms}	220 V
Rated output power P_o	500 W
Output voltage reference	400 V
Operating frequency	60 Hz
Switching frequency	200 kHz

4.2. Controller Design and Implementation

For the current controller design, the transfer function in (12) is utilized. By substituting the parameters into the transfer function, the numerical model in (14) is obtained.

$$\frac{i_g(s)}{d(s)} = \frac{27.38s + 622.3}{6.842 \times 10^{-5} s^2 + 0.0007775s + 0.00047} \tag{14}$$

In (14), the duty reference *d*was selected as 0.2225 which corresponds the required duty reference to produce 400V output at the peak of the input voltage. By using the MATLAB SISOTOOL, the proportional and the integral gains of the PI current controller are designed as 0.1556 and 2103, respectively. These values give 78 deg of phase margin at 10kHz, and it may be an enough controller design specification for the PFC current control.

In order to design the voltage controller, the plant model is derived as (15) rather than using (13), because of the consideration of the current control loop.

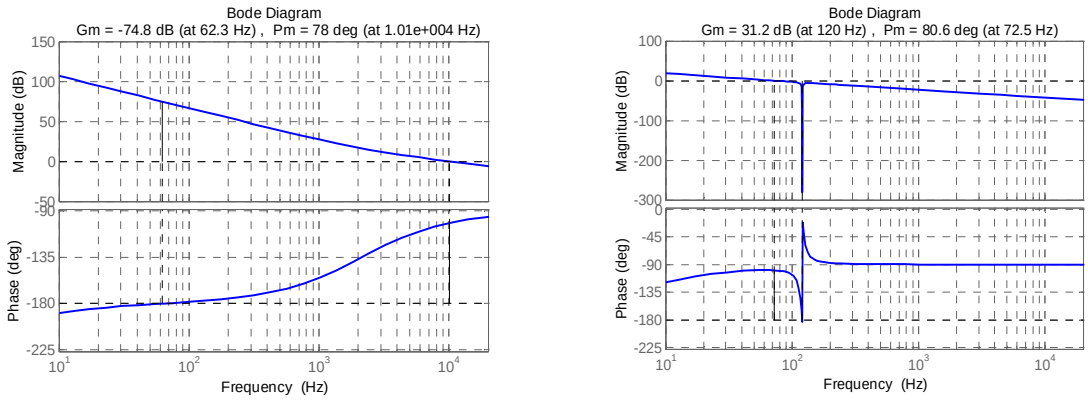
$$\frac{v_c(s)}{i_g(s)} = \frac{R_o}{R_o C_o s + 1} \tag{15}$$

The 120Hz bandstop filter is implemented as follows:

$$G_{bs}(s) = \frac{s^2 + (2\pi \times f_c)^2}{s^2 + 2\pi \times f_b s + (2\pi \times f_c)^2} \tag{16}$$

Where f_c and f_b represent the cut-off frequency and the passband of the bandstop filter. In the simulation, f_c and f_b are selected as 120Hz and 10Hz. Again, the MATLAB SISOTOOL is utilized to determine the

proportional and the integral gains of the PI voltage controller as 0.1 and 5. With the gains, the entire voltage loop has 80.6 deg of phase margin at 72.5Hz. Figure 5 shows the open-loop gain of the current and the voltage control loops. From the figure, it is confirmed that the open-loop gain results with the designed controllers satisfy the design specifications.



(a) the duty-to-inductor current model (b) the duty-to-capacitor voltage model

Figure 5. The open-loop gains

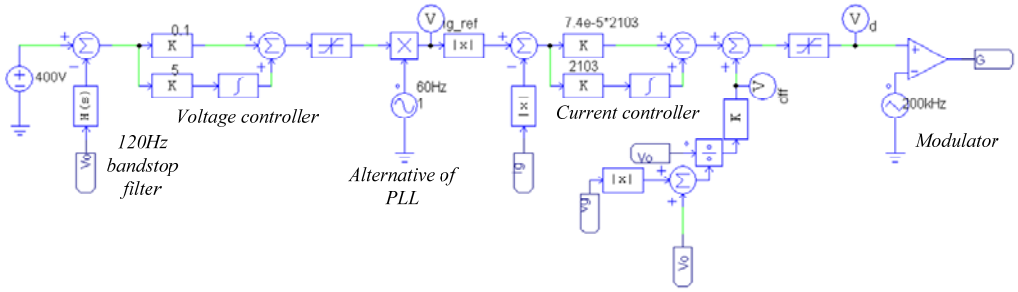
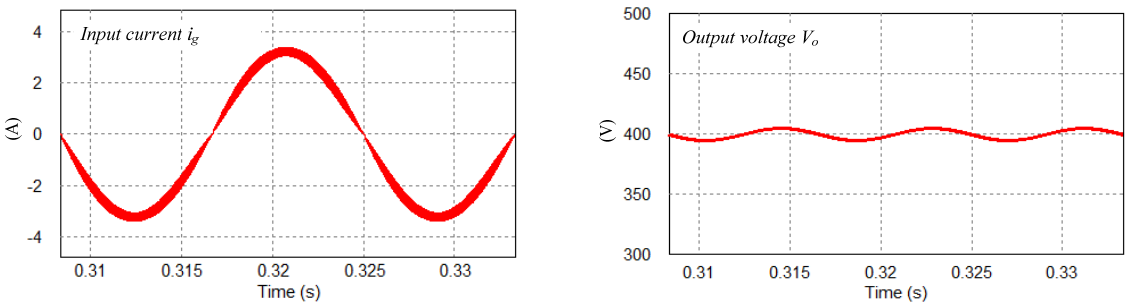


Figure 6. The implemented controller in PSIM

4.3. Simulation Results

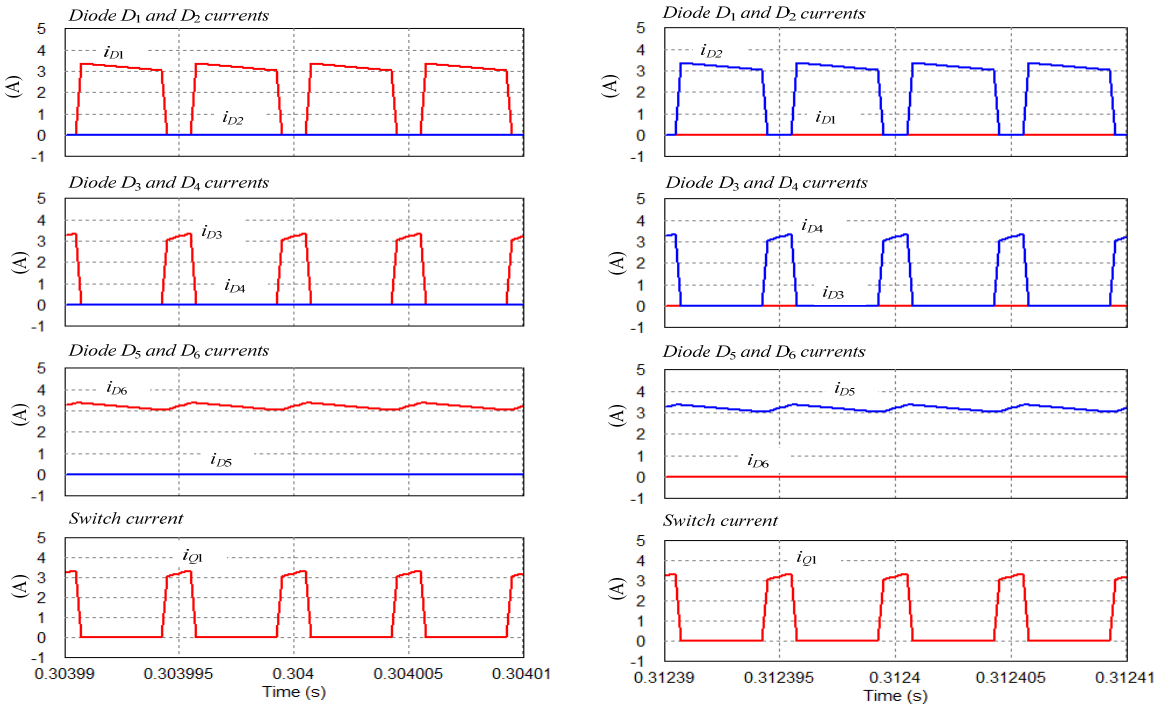
The simulation result using the developed switching model at the full load steady-state condition is shown in Figure 7. As shown in the figure, the input current is regulated sinusoidally, and the output voltage is controlled to 400V. In the output voltage, the well-known double frequency ripple, here 120Hz, appears.



(a) Input current (b) Output voltage

Figure 7. The simulation result at the full load steady-state condition

Figure 8 shows the simulated waveforms of the devices for positive and negative half cycles. The waveforms corresponds the analysis taken in the previous section. Note that the switch current i_{Q1} flows both in the positive and the negative cycles whereas other devices conducts in each half cycle as analyzed before.



(a) For positive half cycle (b) For negative halfcycle

Figure 8. The waveforms of devices

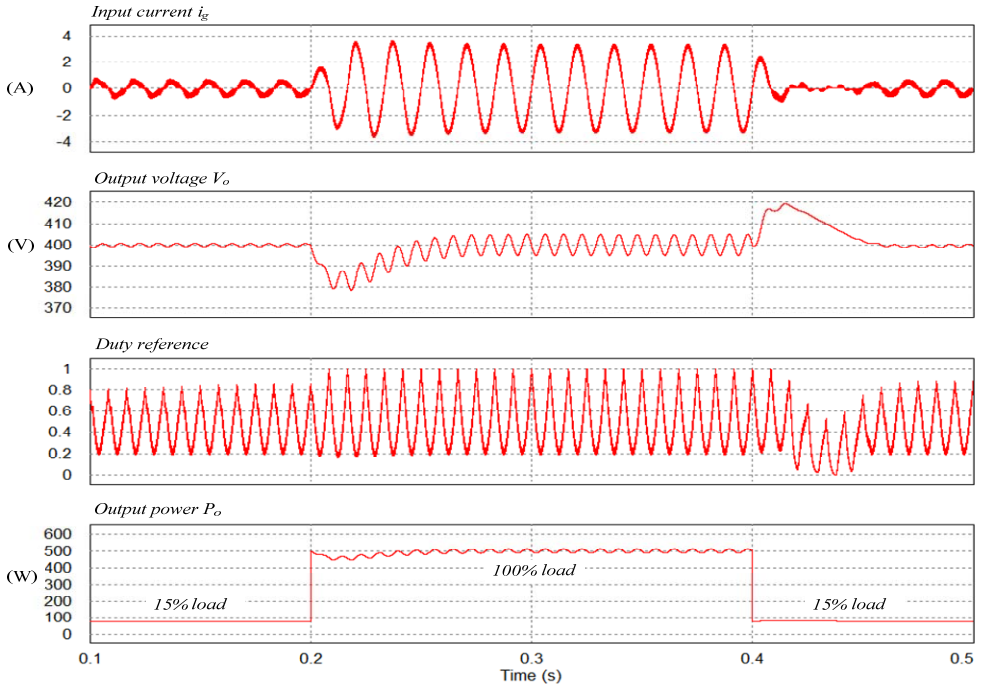


Figure 9. The transient response of the developed switching simulation model

The transient response of the developsed simulation model is shown in Figure 9. In the simulation, the load is changed at $t = 0.2s$ from 15 percent to 100 percent in step. As shown in the figure, the current and the voltage controls are stable, and the current is very well regulated. At t=0.4s, the load is changed to 15 percent. Even in that condition, there is no significant transient problem, and the overshoot of the dc-link voltage is less than 20V. At 15 percent load, the current is slightly distorted, because the converter operates in discontinuous conduction mode in such a small output power [14]-[15]. However, the effect of the current distortion is so little, that it is not a big problem in the entire system performance.

In sum, through the simulations, the operation of the single-switch bridgeless PFC converter has been verified.

5. CONCLUSION

The single-switch bridgeless PFC converter has been proposed in this paper. For the proposed converter, the topology, the operation modes, the modeling and controls have been dealt in detail. The numerical transfer function of the proposed converter has been evaluated using the state-space averaging technique, and the simulation model matched with the numerical function have been tested. In order to see the performance of the proposed converter, a 500W switching model was built in PSIM software package. By using the developted simulation model, both the transient and the steady-state operations have been evaluated. Through the simulations, it has been confirmed that the operation of the proposed converter is very well matching the theoretical analyses. Since the proposed converter employs only one single active switch, it is expeted that the implementation cost can be reduced, and the reliability of the entire power stage can be improved.

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Younghoon Cho was born in Seoul, Korea, in 1980. He received the B.S. degree in electrical engineering from Konkuk University, Seoul, in 2002, the M.S. degree in electrical engineering from Seoul National University, Seoul, in 2004, and the Ph.D. degree from Virginia Polytechnic Institute and State University, Blacksburg, VA, USA, in 2012. From 2004 to 2009, he was an Assistant Research Engineer with the Hyundai MOBIS R&D Center, Yongin, Korea. Since 2013, He is now an Assistant Professor in the Department of Electrical Engineering, Konkuk University, in Seoul. His current research interests include digital control techniques for power electronic converters in vehicle and grid applications, multilevel converters, and high-performance motor drives.