

Multilevel DC Link Inverter with Reduced Switches and Batteries

Y. R. Manjunatha*, B.A. Anand**

* Department of Electrical Engineering, U.V.C.E, K.R. Circle, Bengaluru-1

** Electrical Engineering, Department of Agricultural Engineering, UAS-B, GKV Campus, Bangalore-65

Article Info

Article history:

Received Oct 3, 2013

Revised Mar 1, 2014

Accepted Mar 18, 2014

Keyword:

Cascaded H-bridge inverter

DC link

MLDCLI

Multilevel inverter

Power electronic drives

ABSTRACT

Multilevel inverters are the best solution for medium and high voltage power electronic drives. Because of its unique characteristic of synthesizing sinusoidal voltage with less harmonic contents using several DC sources. In a three phase multilevel inverter, each phase of a cascaded H-bridge inverter requires ' n ' DC sources to obtain $2n + 1$ output voltage levels. One particular disadvantage is that, it increases number of power semiconductor switches. To overcome this disadvantage a multilevel DC link inverter (MLDCLI) with reduced number of switches and batteries is proposed.

Copyright © 2014 Institute of Advanced Engineering and Science.
All rights reserved.

Corresponding Author:

B.A. Anand

Assistant Professor,

Department of Agricultural Engineering,

UAS-B, G.K.V.K, Bangalore-560065

Email: lovanand1586@gmail.com

1. INTRODUCTION

Multilevel converters have received more and more attention because of their capability of high voltage operation, high efficiency, and low electromagnetic interference (EMI). The desired output of a multilevel converter is synthesized by several sources of dc voltages. With an increasing number of dc voltage sources, the converter voltage output waveform approaches a nearly sinusoidal waveform while using a fundamental frequency switching scheme. These results in low switching losses, and because of several dc sources, the switches experience a lower voltage stress. As a result, multilevel converter technology is promising for high power electric devices such as utility applications [1]. There are three major multilevel topologies: cascaded, diode clamped, and capacitor clamped. For the number of levels (M) greater than three or some applications such as reactive and harmonic compensation in power systems, these multilevel converters do not require a separate dc power source to maintain each voltage level. Instead, each voltage level can be supported by a capacitor with proper control. However, for $M > 3$ and applications involved in active power transfer, such as motor drives, these multilevel converters all require either isolated dc power sources or a complicated voltage balancing circuit and control scheme to support and maintain each voltage level. In this aspect, the three existing multilevel converters are neither operable nor complete for real (active) power conversion because they all depend on outside circuits for voltage balancing [2]. Multilevel inverters produce a stepped output phase voltage with a refined harmonic profile when compared to a two-level inverter-fed drive system. However, these configurations are also complex for higher number of levels. The three-level inverter is realized by connecting two 2-level inverters in cascade. This three-level inverter structure does not show the voltage fluctuations of the neutral point, as isolated power supplies are employed to power the individual inverters. [3].

For many applications, to get many separate DC sources is difficult, and too many DC sources will require many long cables and could lead to voltage unbalance among the DC sources [4]. To reduce the number of DC sources and semiconductor switches required, when the cascaded multilevel converter is applied to a motor drive, a scheme is proposed in this paper, that allows the use of *two* unequal voltage DC sources and *eight* switches to generate 7 level equal step multilevel inverter output. Whereas the conventional cascaded multilevel inverter requires *three* equal voltage DC sources and *twelve* switches to generate 7 levels. This scheme provides the capability to produce higher voltages at higher speeds (where they are needed) with a low switching frequency, which has inherent low switching losses and high conversion efficiency. For electric/hybrid electric vehicle motor drive applications, one H-bridges and four switches for cascading the batteries for each phase is a good tradeoff between performance, cost and reliability.

2. MULTILEVEL CASCADED H-BRIDGES INVERTER STRUCTURE

To operate a cascaded multilevel inverter using two unequal DC source, [5] proposed to use the first DC sources (i.e., the battery connected to first H-bridge, H_1) as V_{dc} and the magnitude of voltage of second battery as $2V_{dc}$. To understand the concept, consider a cascaded multilevel inverter with two H-bridges as shown in Figure 1. The DC source for the first H-bridge (H_1) is a battery or fuel cell V_1 with an output voltage of V_{dc} , and the DC source for the second H-bridge (H_2) is V_2 with an output voltage of $V_{dc}/2$. The output voltage of the cascaded multilevel inverter is:

$$V(t) = V_1(t) + V_2(t) \quad (1)$$

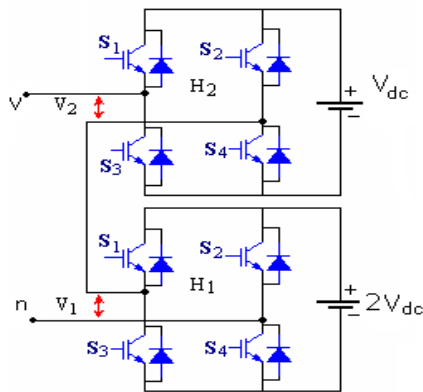


Figure 1. Single phase structure of a Multilevel cascaded H-bridges inverter

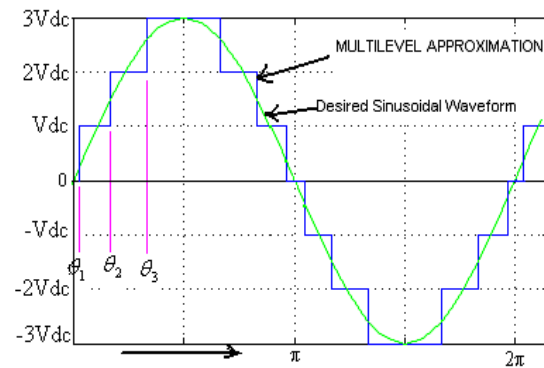


Figure 2. Multilevel converter output with two unequal batteries

By giving the triggering pulses to the switches of H_1 appropriately, the output voltage V_1 can be made equal to V_{dc} , 0, or $-V_{dc}$. while the output voltage of H_2 i.e., V_2 can be made equal to $2V_{dc}$, 0, or $-2V_{dc}$ by giving the triggering pulses to the switches of H_2 appropriately. Therefore, the output voltage of the converter can have the values, $(2V_{dc}+V_{dc})$, $2V_{dc}$, V_{dc} , 0, $-V_{dc}$, $-2V_{dc}$ and $-3V_{dc}(-V_{dc}-2V_{dc})$ which are 7 possible output levels. Figure 2 shows the 7 level equal step output voltage waveform [5].

The significant advantages of multilevel configuration are, voltage sharing both statically and dynamically and it produces better voltage waveforms with less harmonic contents. One particular disadvantage of cascaded H-bridges multilevel inverter is that, it increases greater number of power semiconductor switches. The work proposed in [6] reduces the number of switches, their gate drivers, compared with the existing multilevel inverter counterparts with harmonic profile improvement.

3. CASCADED HALF-BRIDGE-BASED MULTI LEVEL DC LINK INVERTER STRUCTURE WITH UNEQUAL VOLTAGE SOURCES

The work proposed in [6] utilizes three batteries and ten switches to generate seven voltage levels per phase. This paper proposes a scheme in which only two batteries and eight switches are utilized to generate same number of voltage levels per phase and it is shown in Figure 3.

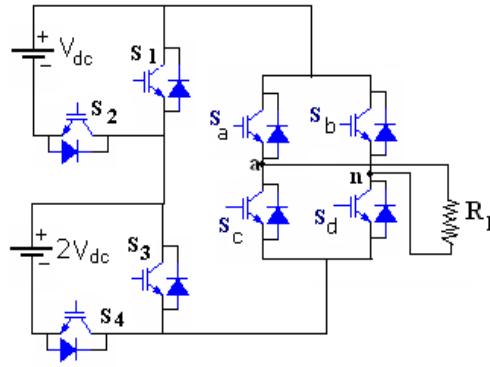


Figure 3. 7-level Cascaded multilevel DC link inverter with unequal source

The cascaded Multi Level DC Link (MLDCL) inverter with unequal voltage batteries consists of half bridge cells and one full bridge cell. Each half-bridge cell has two switches S_1 and S_2 . They operate in a toggle fashion. The cell source is bypassed when S_1 is on and S_2 is off. The cell source adds to the DC link voltage when S_1 is off and S_2 is on. The half bridge cell produces DC bus voltage waveform in the shape of staircase and the full bridge inverter cell alternates the voltage polarity to produce an AC voltage of staircase waveform. Single-phase bridge inverter contains four switches from S_a , S_b , S_c and S_d .

Table 1. Switching Pattern For Cascaded H-Bridge Mldci With Unequal Voltage Sources—Seven Level

Levels	S_1	S_2	S_3	S_4	S_a	S_b	S_c	S_d	V_{R_L}
1	on	off	off	on	on	off	off	on	V_{dc}
2	off	on	on	off	on	off	off	on	$2V_{dc}$
3	off	on	off	on	on	off	off	on	$3V_{dc}$
4	off	off	off	off	off	off	off	off	0V
5	on	off	off	on	off	on	on	off	$-V_{dc}$
6	off	on	on	off	off	on	on	off	$-2V_{dc}$
7	off	on	off	on	off	on	on	off	$-3V_{dc}$

Table 1 shows switching pattern for cascaded H-bridge MLDC inverter with unequal voltage sources. Specifically, the MLDCL formed by the 2 half-bridge cells provides a staircase-waveform in the dc-bus voltage of 3 steps to the full bridge inverter, which in turn alternates the voltage polarity to produce an ac voltage V_{an} of a staircase shape with 7 levels.

4. COMPARISON OF MLDCL INVERTER WITH UNEQUAL SOURCES AND EXISTING COUNTERPARTS

The multilevel dc-link inverter effectively reduces the number of switches and their gate drivers. Cascaded multilevel inverter requires $2 * (m-1)$ number of switches and the cascaded MLDCL require only $(m+3)$ number of switches. Whereas the proposed MLDCL inverter with unequal voltage sources requires just $(m+8)$ switches, Where m takes the values 0, 2, 4, 6, 8,..., for 7, 15, 31, 63,..., switching levels respectively. In addition, the new multilevel dc-link inverter saves the cost of the inverter circuit by having an additional module of single-phase full bridge inverter. With higher voltage levels, only two switches are enough for fabricating each bridge in multilevel dc-link (MLDCL) with four switches in single phase full bridge inverter.

Table 2. Component Count Comparison—Seven Levels

Types of Inverter	No. of Levels	No. of Batteries	No. of Switches
Conventional Multi Level Inverter with equal source voltages	7	3	12
	15	7	28
	31	15	60
	63	31	122
MLDCL Inverter with equal source voltages	7	3	10
	15	7	18
	31	15	34
	63	31	65
MLDCL Inverter with unequal voltage sources	7	2	8
	15	3	10
	31	4	12
	63	5	14

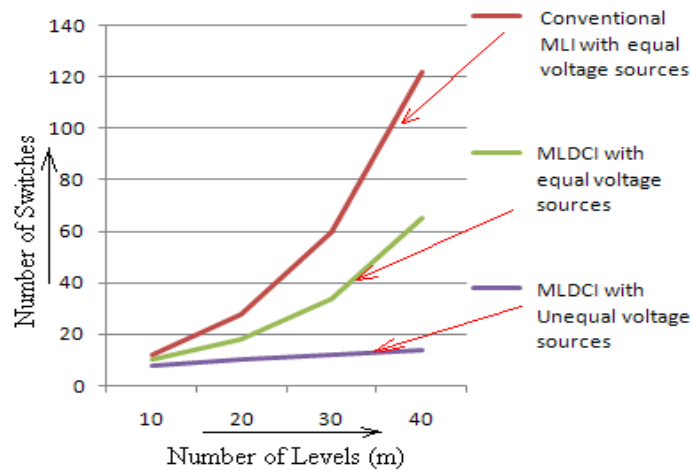


Figure 4. Comparison of required number of Switches

Figure 4 shows the reduction in number of switches in the MLDCL inverter with unequal voltage sources. The number of levels as compared to the Conventional Multi Level Inverter with equal source voltages and MLDCL Inverter with equal source voltages the MLDCL inverter with unequal voltage sources scheme considerably reduces the number of switches.

Figure 5 shows the reduction in number of batteries in the MLDCL inverter with unequal voltage sources. The number of batteries as compared to the Conventional Multi Level Inverter with equal source voltages and MLDCL Inverter with equal source voltages the MLDCL inverter with unequal voltage sources scheme considerably reduces the number of batteries.

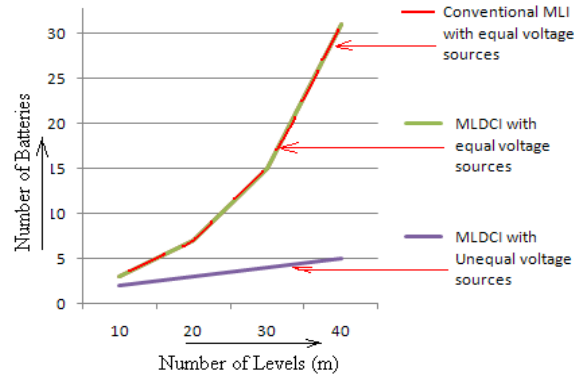


Figure 5. Comparison of required number of Batteries

5. MODULATION AND SWITCHING CONTROL

Generally, traditional PWM control methods and space vector PWM methods are applied to multilevel inverter modulation control. The disadvantage of the traditional PWM methods is the power loss in the switches due to the high switching frequency [7]-[9]. For these reasons, low switching frequency control methods, such as a fundamental frequency method [10], and the active harmonic elimination method [11] has been proposed for motor drive applications. This is the simplest switching control method for the proposed multilevel motor drive. It also is an effective modulation control method for the proposed Multilevel DC link inverter with unequal voltage sources motor drive.

The Fourier series expansion of the 7-level equal step output voltage waveform is:

$$V(\omega) = \sum_{n=1,3,5,\dots}^{\infty} \frac{4V_{dc}}{n\pi} \{ (\cos n\theta_1) + (\cos n\theta_2) + (\cos n\theta_3) \} \sin(n\omega t) \quad (2)$$

Where 'n' is the order of harmonic in the output voltage of multilevel inverter. Given a desired fundamental voltage V_1 , one wants to determine the switching angles θ_1 , θ_2 , θ_3 so that $V(\omega) = V_1 \sin(\omega t)$, and specific higher harmonics of $V(n\omega t)$ are eliminated [6]-[8]. For three-phase motor drive applications, the triplen harmonics in each phase need not be considered as they automatically cancel in the line-to-line voltages. The lower order harmonics can be eliminated by choosing proper values for θ_1 , θ_2 and θ_3 in the following equations:

$$\left. \begin{aligned} \cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) &= m \\ \cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) &= 0 \\ \cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) &= 0 \end{aligned} \right\} \quad (3)$$

This is a system of three transcendental equations in the three unknowns θ_1 , θ_2 , and θ_3 . There are many ways one can solve for the angles [10], [12]-[14]. Here the resultant method [11], [15] was used to find the switching angles. The modulation index m is defined as:

$$m = \frac{\pi V_1}{2V_{dc}} \quad (4)$$

And the total harmonic distortion (THD) up to the 50th harmonic (odd, non-triplen) is computed as:

$$THD = \frac{\sqrt{V_5^2 + V_7^2 + \dots + V_{49}^2}}{V_1} \quad (5)$$

6. SIMULATION AND EXPERIMENTAL RESULTS

To validate the proposed MLDCL inverter with unequal voltage sources, a motor drive control scheme has been developed. The switches used for this inverter are the IGBTs GT60M303 (Toshiba Make). The gating pulses are generated by microcontroller board. A 3-phase induction motor is selected with the specifications shown in the Table 3 below. Also motor model is developed using MATLAB Simulink.

Table 3. Specification of motor

S. No.	Type of the motor	3- ϕ Induction motor
1	Rated Output Power	3700 watts (5 HP)
2	Rated line to line voltage	415 volts
3	Rated Current	8.4 amps
4	Number of Poles	4
5	Frequency	50 Hz
6	Rated Speed	1485 rpm
7	Type of winding	Y- connected

The parameters of this motor are calculated by conducting No-load test, Blocked Rotor test and Retardation test. This motor model is simulated using MATLAB and the simulated results are compared with that of practical results. It is found that these two results are very close to each other. Then the motor model is simulated with the proposed cascaded multilevel inverter.

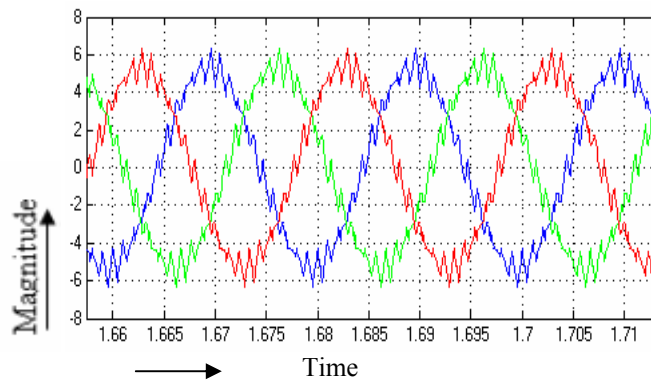


Figure 6. Stator current, motor fed from SPWM Inverter

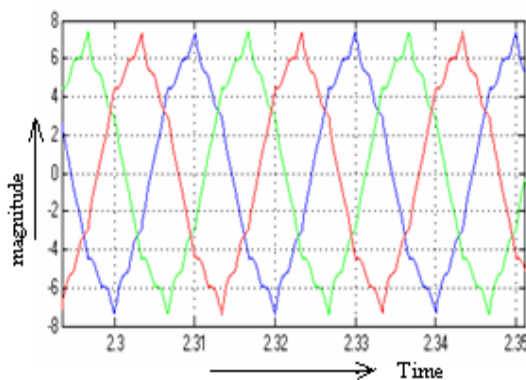


Figure 7. Stator current, motor fed from ML Inverter

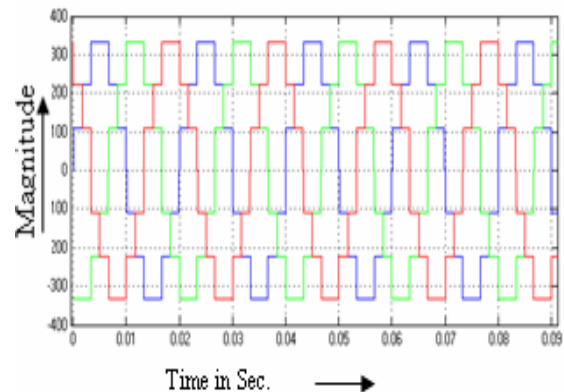


Figure 8. Output voltage waveform of MLI (3 phase)

Figure 6 shows the stator currents of three phase induction motor on no-load fed from 2 level inverter. In this figure even though the waveform looks close to sinusoidal, it has distortion. Figure 7 is the stator currents of the same motor fed with 7 level inverter. It is observed that the distortion is almost reduced. Hence the motor runs smoothly and safely. Fig. 8 is the three phase output voltage of multilevel (7 Level) inverter with two unequal voltages.

7. EXPERIMENTAL VALIDATION

To experimentally validate the proposed multilevel inverter, a prototype MLDCL inverter with two unequal batteries per phase and 8 IGBTs as switching devices. The fundamental frequency of the inverter output is 50Hz. Figure 9 shows the block diagram of the experimental setup.

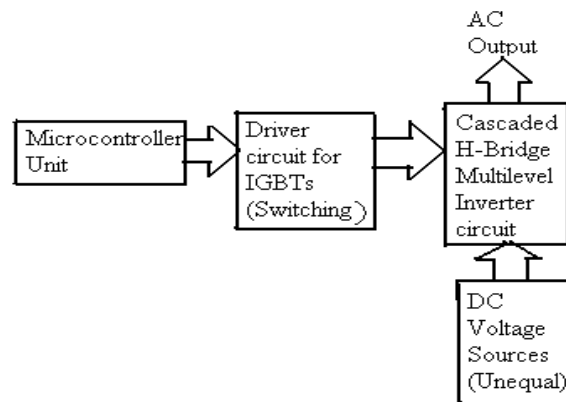


Figure 9. Block diagram of the experimental setup

The microcontroller unit is a PIC 18F8722 microcontroller. It is an 80 pin TQFP package needs +12V DC supply for its working and operates at a frequency of 40MHz. This microcontroller has 128KB of program memory, 3936 bytes of data memory and 1024 bytes of data EPROM memory. It also has 9 I/O ports and 5 timers. This microcontroller is used to implement the control algorithm (i.e. to generate the gating pulses) for switching devices in the MLDCL inverter with unequal voltage sources. The gating pulses generated by microcontroller cannot be connected directly to the power semiconductor switching devices. Hence the driver circuit is introduced between microcontroller and MLDCL inverter with unequal voltage sources. The detailed circuit diagram of this driver unit is shown in Figure 10.

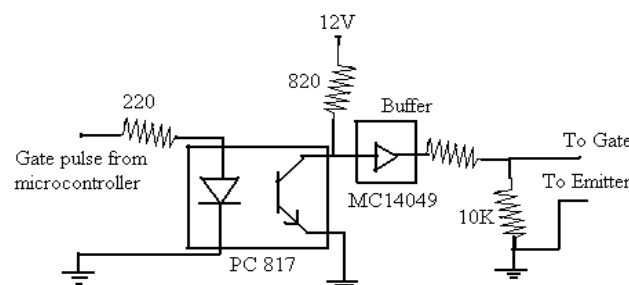


Figure 10. Gate drive circuit for IGBT

The driver circuit consists of an optocoupler (PC 817) to which the gating pulse generated by microcontroller is given. This optocoupler is used for isolation purpose. Output of optocoupler is passed through a buffer to improve the output drive capacity of the driver circuit so that the switching device can turn on quickly without delay. The driver circuit is for only one switching device. MLDCL inverter with unequal voltage sources was shown in Figure 3. This inverter circuit has been built using 900V, 60A IGBTs

(i.e. CT60AM-18F of Mitsubishi make) as switching devices. These devices have a maximum turn ON time of 0.75 μ s and turn off time of 0.7 μ s.

8. CONCLUSION

This paper developed a Multilevel DC Link Inverter with unequal voltage sources motor drive control scheme that required only two-battery source for each phase. A 7-level equal step output voltage switching control method has been applied to the motor drive. Multilevel DC Link Inverter with unequal voltage sources is simulated using MATLAB Simulink. The hardware prototype is implemented using Microcontroller. A seven level-cascaded multilevel DC-link inverter with unequal voltage sources is successfully fabricated and tested. The new MLDCL inverter with unequal voltage sources needs least number of components than the other counterpart existing multilevel inverters for the same level of output waveform. By increasing the number of levels of the Multilevel DC Link Inverter with unequal voltage sources switches, gate driver and battery are reduced with better output waveform.

REFERENCES

- [1] Z Du, L Tolbert, J Chiasson. Active Harmonic Elimination on Multilevel power converters. *IEEE Trans. Power Electron.*, 2006; 21(2): 459–469.
- [2] Fang Zheng Peng, Senior Member, IEEE. A Generalized Multilevel Inverter Topology with Self Voltage Balancing. *IEEE Transactions on industry applications*. 2001; 37(2): 611-618
- [3] VT Somasekhar, K Gopakumar, Senior Member, IEEE, M. R. Baiju, Krishna K. Mohapatra, Student Member, IEEE, L Umanand. A Multilevel Inverter System for an Induction Motor with Open-End Windings. *IEEE Transactions on industrial electronics*. 2005; 52(3).
- [4] Zhong Du, Leon M Tolbert, John N Chiasson, Burak Ozpineci Hui Li, Alex Q Huang. Hybrid Cascaded H-bridges Multilevel Motor Drive Control for Electric Vehicles.
- [5] Manjunatha YR, Dr MY Sanavullah. Generation of Equal Step Multilevel Inverter Output Using Two Unequal Batteries. *International Journal of Electrical and power engineering*. 2007; 1(2): 206-209.
- [6] R Kavitha, P Dhanalakshmi Rani Thottungal. Implementation of Novel Low Cost Multilevel DC-Link Inverter with Harmonic Profile Improvement. *Asian Power Electronics Journal*. 2008; 2(3): 158-162.
- [7] HS Patel, RG Hoft. Generalized harmonic elimination and voltage control in thyristor inverters: Part I -harmonic elimination. *IEEE Trans. Industry Applications*. 1973; 9: 310-317.
- [8] HS Patel, RG Hoft. Generalized harmonic elimination and voltage control in thyristor inverters: Part II -voltage control technique. *IEEE Trans. Ind. Applications*. 1974; 10: 666-673.
- [9] PN Enjeti, PD Ziogas, JF Lindsay. Programmed PWM techniques to eliminate harmonics: A critical evaluation. *IEEE Transactions on Industry Applications*. 1990; 26(2): 302-316.
- [10] Z Du, LM Tolbert, JN Chiasson. Harmonic elimination for multilevel converter with programmed PWM method. *IEEE Industry Applications Society Annual Meeting*. Seattle, Washington. 2004: 2210-2215.
- [11] PN Enjeti, PD Ziogas, JF Lindsay. Programmed PWM techniques to eliminate harmonics: A critical evaluation. *IEEE Transactions on Industry Applications*. 1990; 26(2): 302 - 316.
- [12] T Kato. Sequential homotopy-based computation of multiple solutions for selected harmonic elimination in PWM inverters. *IEEE Trans. Circuits and Systems I*. 1999; 46(5): 586-593.
- [13] JN Chiasson, LM Tolbert, KJ McKenzie, Z Du. A new approach to solving the harmonic elimination equations for a multilevel converter. *IEEE Industry Applications Society Annual Meeting*. Salt Lake City, Utah. 2003: 640-645.
- [14] Z Du, LM Tolbert, JN Chiasson. *Modulation extension control for multilevel converters using triplen harmonic injection with low switching frequency*. IEEE Applied Power Electronics Conference. Austin, Texas. 2005: 419-423.
- [15] S Sirisukprasert, JS Lai, TH Liu. Optimum harmonic reduction with a wide range of modulation indexes for multilevel converters. *IEEE Trans. Ind. Electronics*. 2002; 49(4): 875-881.
- [16] Zhong Du, Leon M Tolbert, John N Chiasson2, Burak Özpineci. A Cascade Multilevel Inverter Using a Single DC Source. 426-430.

BIOGRAPHIES OF AUTHORS

Y.R. Manjunatha did his BE from Mysore University in Electrical And Electronics Engineering from J.N.N College of Engineering, Shimoga. He has completed his Master of Technology in Power Electronics Engineering at B.M.S College of Engineering under Visvesvaraya Technological University Belgaum. Dr. Manjuntha has obtained his Doctoral Degree from V.M.U, Salem in Electrical Engineering. His area of interests in power electronics modeling, power engineering in the field of energy conversion, Distribution System Automation and Designing of Power Electronics Converters. He is currently Chairman and Head of the Department in Department of Electrical Engineering at U.V.C.E, Bangalore University.



B.A. Anand did his BE from Visvesvaraya Technological University during 2004-08 in Electrical and Electronics Engineering from Sri Krishna Institute of Technology, Chikkabanavara, Bangalore. He has completed his Master of Engineering in Power and Energy Systems at University Visvesvaraya College of Engineering [U.V..C.E] during 2010-2011. Mr. B.A. Anand is obtaining his Doctoral Degree from Visveswaraya Technological University in Department of Electrical Engineering. He is currently working as Assistant Professor of Electrical Engineering in Department of Agricultural Engineering at University of Agricultural Sciences-Bangalore, G.K.V.K Campus, Bangalore-560065. His interests are in the area of power system operation and control, Substation automation and Power distributions system studies.