International Journal of Power Electronics and Drive System (IJPEDS)
Vol. 4, No. 3, September 2014, pp. 337~342
ISSN: 2088-8694

Closed Loop Analysis of Multilevel Inverter Fed Drives

V.S. Bharath*, Gopinath Mani**
* Research scholar, Bharath University, chennai, India
** Professor, dr.n.g.p. Institute of technology, Coimbatore, tamilnadu, India

Article Info

Article history:

Received Feb 18, 2014
Revised Apr 3, 2014
Accepted Apr 19, 2014

Keyword:

Multilevel Inverter
switching angles
Total harmonic distortion
Selective Harmonics Elimination

ABSTRACT

This paper deals with the simulation and implementation of multilevel inverter for drives application. Here the focuses will be onimproving the efficiency of the multilevel inverter and quality of output voltage waveform. The circuit is developed towards high efficiency, high performance, and low cost, simple control scheme. Harmonics Elimination was implemented to reduce the Total Harmonics Distortion (THD) value which is achieved by selecting appropriate switching angles. In this paper to determine the performance of rectifier, steady state analysis is done. Furthermore, the merits of multilevel inverter topology are inherited.Closed loop control is done to analysis the stability of the system.

Corresponding Author:

V.S.Bharath
Research Scholar
Departement of Electrical and Electronics Engineering,,
Bharath University, Chennai-72.
Email: bharathpg2002@gmail.com

1. INTRODUCTION

Nowadays researchers all over the world spending their great efforts to improve the performance of multilevel inverters system by control simplification and optimized algorithms in order to decrease Total Harmonic Distortion (THD) and torque ripple of the motor. Today in all industries Variable speed drives are most commonly used. AC drives such as Induction Motors (IM) and recently Permanent Magnet Synchronous Motors (PMSM) are offered. The widely used applications are pumps, fans, elevators, electrical vehicles, heating, ventilation and airconditioning, robotics, wind generation systems, ship propulsion, etc. In the present industrial world there is a very great need to control the speed of the drives for better production and quality output where rotating machines are used. Nowadays PMSM gives very fast and accurate speed response, insensitivity to parameter variations with quick recovery of speed from the disturbance.The Inverter output waveforms are usually rectilinear in nature which contain harmonics, it may lead to reduced load efficiency and performance. In many industrial applications it is very essiential to control the output voltage of inverters.There are mainly three types of multilevel inverters; they are 01) diode- clamped, 02) flying capacitor and 03) cascade multilevel inverter (CMLI). Out of which CMLI has wide range of application. [1]-[2]. In [3]-[4], iterative numerical analysis have been implemented to solve the SHE equations. By using the proposed topology the number of switches will reduced and hence the efficiency will improve as in [5]. In high power applications, the harmonic content of the output waveforms has to be reduced as much as possible inorder to avoid distortion in the grid and to reach the maximum energy efficiency [6].The phase shifted technique is best suitable for CMLI and it is used in this paper for generation of triggering pulses to CMLI [7]-[9]. Multilevel sinusoidal PWM can be classified as in [10]. In this paper five level diode clamped multilevel inverters fed drive is used and a closed loop Control system is designed using PI controller in order to maintain load voltage constant during under voltage and Over voltage conditions.

2. MULTILEVEL INVERTER

According to research, the first multilevel inverter wasdesigned in the year 1975 and it was a cascade inverter with diodes blocking the source of the circuit. This inverter was later derived into theDiode Clamped Multilevel Inverter, also called Neutral-PointClamped Inverter. In the NPCMLI topology the voltage clamping diodes is used which is an essential one.

The main aim of the modulation strategy of multilevel inverters is to synthesize the output voltage as close aspossible to the sinusoidal based waveform. In research work lot of modulation techniques are interduced for harmonic reduction and switching loss minimization. This modulation method which is used in multilevel inverters can be classified according to switching frequency of the system. The methods that work with high switching frequency have more commutations for the power semiconductors in one period of the fundamental outputvoltage of inverter. A very popular method in industrial applications is the classic carrier-based sinusoidal PWM (SPWM) that uses the phase-shifting technique to reduce the harmonics in the load voltage. Another interesting alternative is the SVM strategy which is used in three-level inverters. A common DC-bus is divided by an even value, depending on the number of voltage evels in the inverter circuit, of bulk capacitors in series with a neutral point in the middle of the line. The diode-clamped mulilevel inverter uses capacitors in series to divide equally the dcbus voltage into anequal set of voltage levels of the system. To generate m levels ofthe phase voltage, an m-level diode-clamp inverter needs m-1level capacitors on the dc bus system. A Multilevel inverter is shown in Figure 1. The dc bus consists of four capacitors. They are listed as C1, C2, C3, and C4. For a dc bus voltage Vdc, the voltage across each capacitor is Vdc/4, and each device voltage stress will be limited to one capacitor voltage level, Vdc/4, through clamping diodes. In the inverter system DCMI output voltage synthesis is relatively consider as straight forward. In general to explain how the staircasevoltage is synthesized, point O is considered as the outputphase voltage, this is considered as the reference point. The multilevel inverter is shown in Figure 1 which have five switch combinations to generatefive level voltages across A and O. Table 1 shows that the phase voltage level and their corresponding switch states. From Table 1, state 1 represents that the switch is on and state 0 representsthe switch is off. Therefore in each phase a set of four adjacentswitches is on at any given time. Thefour complimentaryswitch pairs exist in each phase, they are listed as Sa1 to Sa'1, Sa2 to Sa'2, Sa3 to Sa'3and finally Sa4 to Sa' 4.

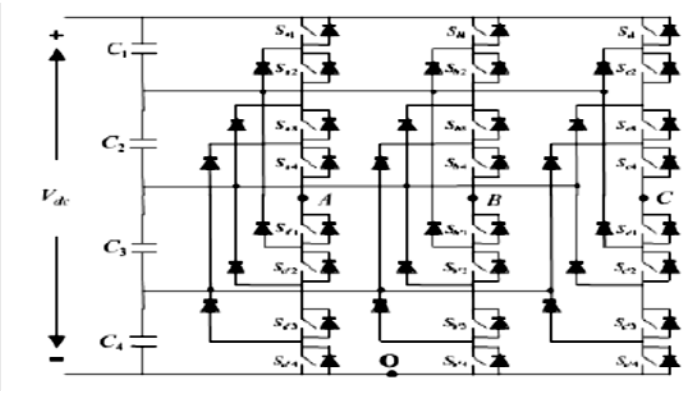

Figure 1. Multilevel Inverter

Table 1. Switching stage

O/P Vo	Switch State							
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	$S_{a'1}$	$S_{a'2}$	$S_{a'3}$	$S_{a'4}$
$V_5=V_{dc}$	1	1	1	1	0	0	0	0
$V_4=3V_{dc}/4$	0	1	1	1	1	0	0	0
$V_3=V_{dc}/2$	0	0	1	1	1	1	0	0
$V_2=V_{dc}/4$	0	0	0	1	1	1	1	0
$V_1=0$	0	0	0	0	1	1	1	1

Selective Harmonic Elimination (SHE) technique for one phase inverters is one of the options for inverters to reduce some harmonics and set the cut frequency of a low- pass filter with a higher value to reduce the size of inductances and capacitances of the filter. Even some harmonics can be eliminated, the total harmonic distortion could increase. Multilevel inverters provide a less THD than other inverters and it can improve with more levels added. One of the drawbacks is the calculation of the switching angles since the more levels are needed, more angles must be calculated and more time is spent in calculation. The RMS voltage for (2p+1) levels is,

$$V_{o,RMS} = \sqrt{P^2 - \frac{2}{\pi}\sum_{t=0}^{p-1}(2i+1)\alpha_{t+1}} \quad (1)$$

Where p is the number of switching angles in half cycle.

The Fourier coefficients are:

$$b_n = \sum_{i=1}^{p}\frac{2}{\pi}\int_{\alpha}^{\pi-\alpha} Esin(n\theta)d\theta \quad (2)$$

$$b_n = \frac{4E}{n\pi}\sum_{i=1,3,5}^{p}\cos(n\alpha) \quad (3)$$

One of the most used techniques for finding the switching angles is to use the Fourier coefficients to eliminate some harmonics. The number of harmonics to be eliminated is equal to the number of switching angles to be calculated minus one, with this technique.

3. SIMULATION ANALYSIS OF MULTILEVEL INVERTER

In this paper, Figure 2 shows the simulation of new cascaded five level H bridge multilevel inverter. The proper switching control of the auxiliary switch can generate half level of dc supply voltage which has five output voltage levels. The levelsare V, V/2, 0, -V/2, -V. For getting the better output voltage, the switches need to be turned on. The switching combinations are shown in Table 1. The output voltage and current waveforms are shown in Figure 3. It measures 200volt and 01amp current. The Schematic is shown below.

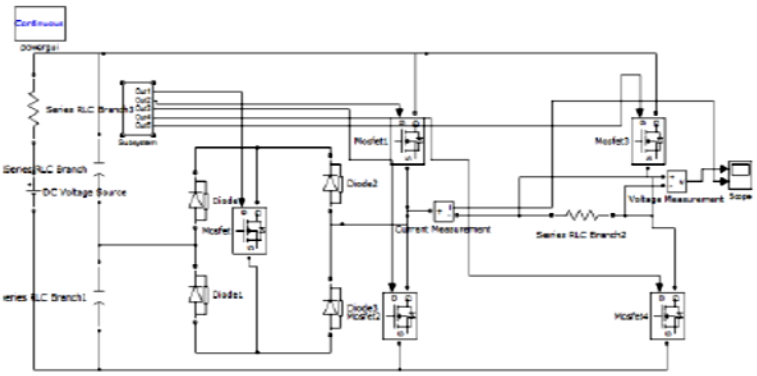

Figure 2. Simulation of Multilevel Inverter

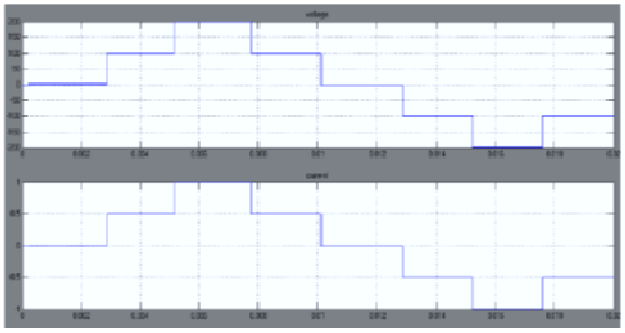

Figure 3. Its shows the voltage and current waveform

The simulated result for phase voltage and its THD spectrum is shown in Figure 4. The simulated values of THD are in close agreement hence validating results. It is to be noted that the modulation index for CMLIs have been chosen randomly. The THD in output voltage increase with increase in number of levels. Nextsimulation analysis of closed loop PI control of multilevel inverter fed drive has done. Mathematical model of PMSM is simulated drive model. The closed loop PI controller is done using field oriented control to control the speed & torque of the drive.The torque speed characteristics of the drive strongly correlates with the employed modulation strategies.The entire work is simulated using MATLAB/SIMULINK software. The closed loop PI control of multilevel inverter fed drive is shown in Figure 5. Generally the PI controllers are used widely in motion control of systems. It consist of a proportional gain that produces an output directly proportional to the input error and an integration to make thesteady state error zero for a step change in the input.

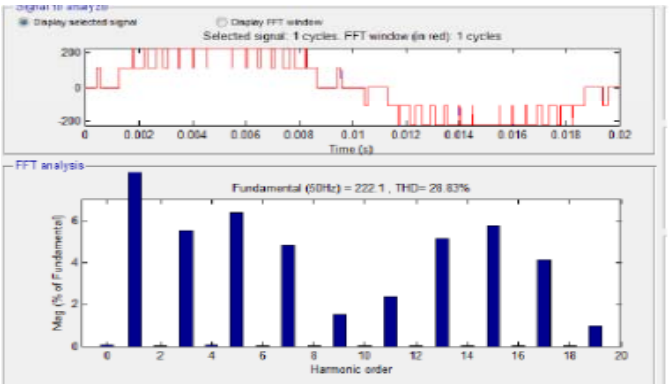

Figure 4. THD value of phase voltgage

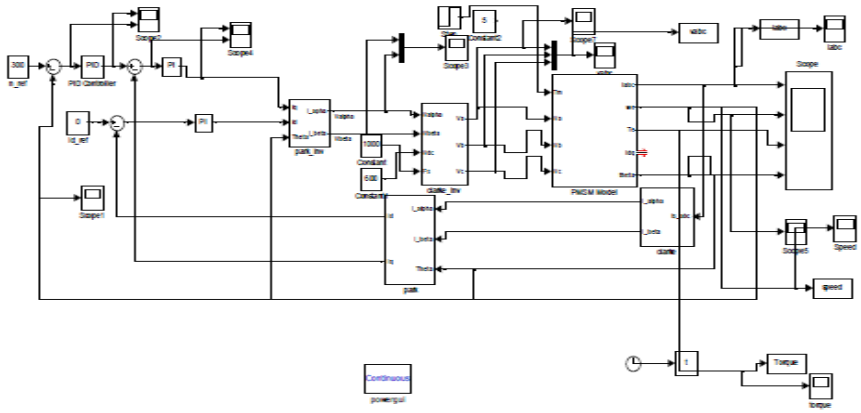

Figure 5. Closed loop analysis of multilevel Inverter

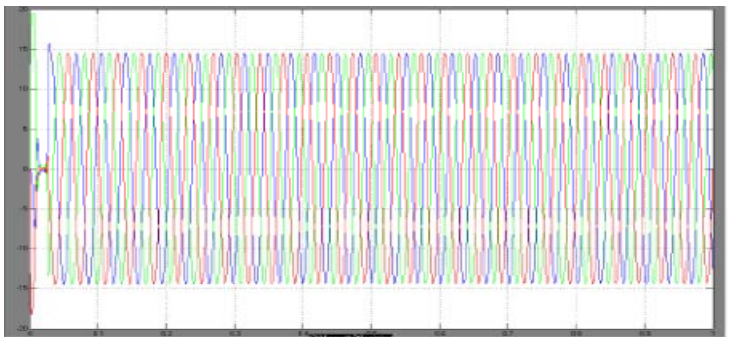

Figure 6. Output voltage waveform

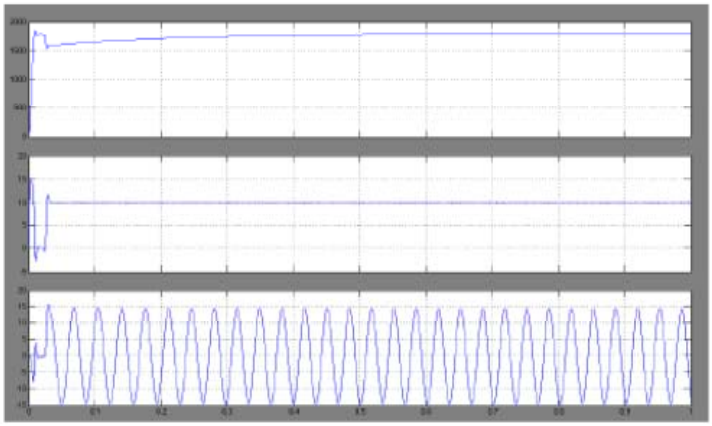

Figure 7. Output Speed, Torque and Current waveform

The output voltage of the closed loop system is shown in Figure 6 which reaches the set value, the corresponding speed, torque and current waveform of the drive system is shown in Figure 7. From the above results it implies that the speed torque characteristics of drive are having very good transient and steady state characteristics. A speed controller has been successfully designed for a drive system, so that the motor runs at the reference speed. In the above simulation the measurement of currents and voltages in each part of the system is possible, thus permitting the calculation of instantaneousor average losses, and efficiency.

4. CONCLUSION

This work has covered the simulation of multilevel inverter and closed loop multilevel inverter fed drives using MATLAB/SIMULINK software. Closed loop models are developed and they are used successfully for simulation. The simulation studies indicate that a simple way to get the desired output voltage with minimum THD. The simulation results are in line with the predictions. The closed loop PI controllers control the speed & torque of the drive which is seen from the result. From the results, the author can conclude that the speed torque characteristics of drive are having very good transient and steady state characteristics. The hardware implementation will be done in future.

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BIOGRAPHIES OF AUTHORS

V.S.Bharath, has obtained his B.E degree from Madras University, Chennai. He obtained his M.E degree from Annamallai University, Chidambram. He is presently aresearch scholar of Bharath University, Chennai. His area of interest is Inverter fed AC drives. He has a vast experience in teaching. At present he is working as Associate professor in an engineering college Bengalure.

Gopinath Mani has obtained his B.E degree from Bharathiar University, Coimbatore in the year 2002. He obtained his M-Tech degree from Vellore Institute of Technology; Vellore in the year 2004.He obtained is Doctorate from Bharath University, Chennai. He is working as a Professor/EEE, at Dr.N.G.P Institute of Technology, Coimbatore, India. His Area of interest is Power Electronics. He is professional member of IEEE, ISTE, IETE, IAENG, and IACSIT. He has received best performer award in the year 2010.