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A Survey and Experimental Verification of Modular Multilevel Converters

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ABSTRACT

This article primarily brings to limelight the Multi-level converters review and specifically the form and function of modular multilevel converter (MMC) with their modulation, design considerations, balancing issues, control schemes, and applications. This article intends to make a detailed analysis of MMC with their controller related issues in comprehensive manner. It is an approach for MMC design and modulation schemes in easy manner. Furthermore, a five level MMC have been designed with optimal controller and verified by its experimental results and explored. In addition to that, this approach draws strategic conclusions on MMC towards making the system more robust in operation, less complex in design and control.

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1. INTRODUCTION

Many investigations in the field of modular multi-level inverters have led to successful operation in HVDC systems. In recent times, in the power transmission era, for very long distances, high voltage DC (HVDC) transmission lines based on current source inverters (CSI) and voltage source inverters (VSI) are found to be offering more economic and cost effective power transmission. But, recently HVDC transmission systems based on VSI have received increasing attention due to many opportunities like the grid access of weak AC networks, independent control of active and reactive power, supply of passive networks and black start capability, high dynamic performance and small space requirements [1]-[3].

In particular, the novel power converter topology for MMC has been intensively researched, developed, and valuated against many features like high modularity, simple scalability, low expense of filters, robust control, simple in design and redundancy. This converter is composed by identical power cells connected in series, each one built up with standard components, enabling the connection to high voltage poles. Although the MMC and derived topologies offer several advantages, simultaneously they also introduce a more complex design of the power circuit and control goals, which have been the main reason for the recent and ongoing research. Furthermore, Medium Voltage Converters are an interesting area for the application of MMCs. This paper is organized in four sections. Section-1 introduces the MMC. Section -2 discusses the different topologies and modulation techniques. Section-3 should discuss the different control techniques, fault tolerant operation and its experimental verification and finally conclusion with recommendations are provided.

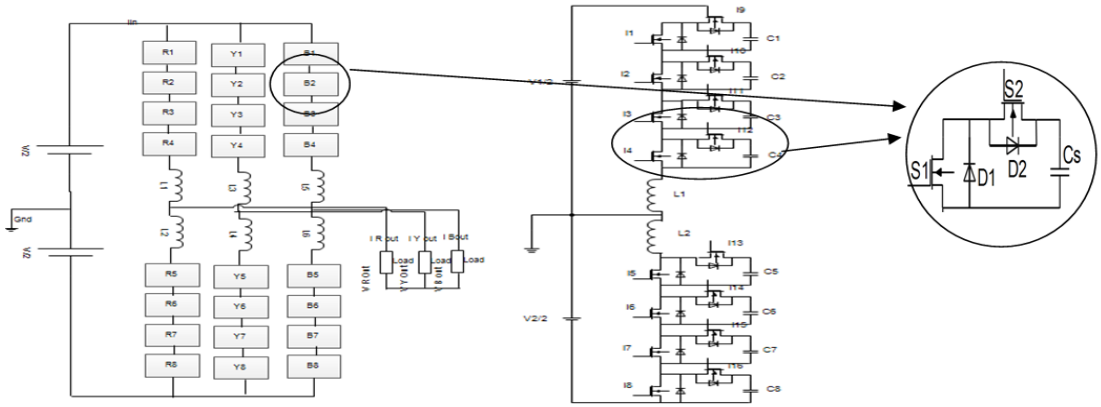

Figure 1. Five level three phase single star chopper cell based Modular Multi Level converter and its sub-module configuration

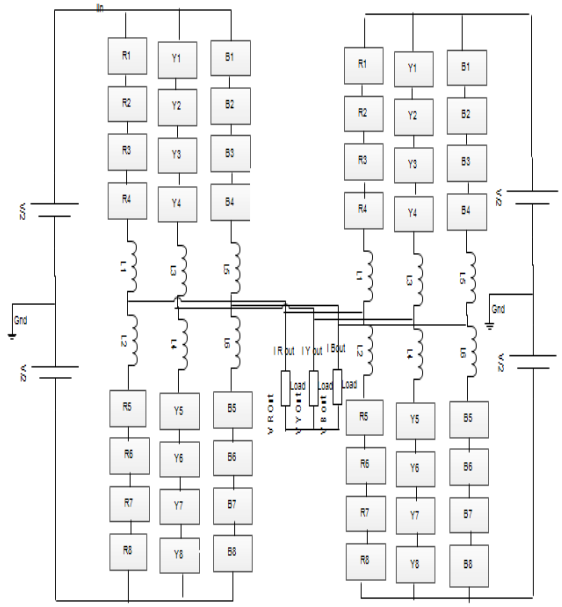

Figure 2. Double star three phase five level Modular Multi Level converter

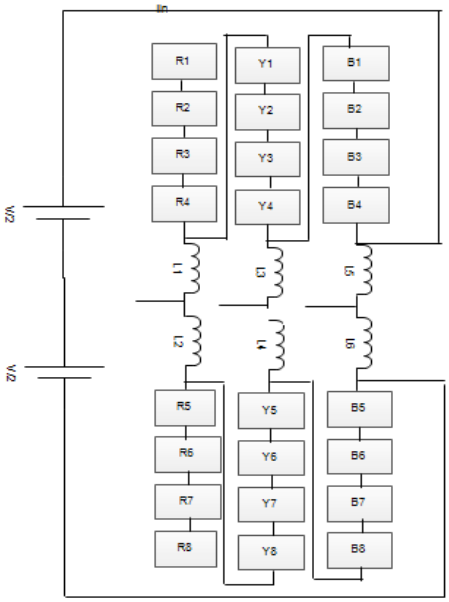

Figure 3. Single delta three phase five level Modular Multi Level converter

2. MODULAR MULTI-LEVEL CONVERTER TOPOLOGIES AND MODULATION TECHNIQUES

There are many topologies are existing in literature, after careful review, based on function and its applicability, it has been divided as follows:

a) Single star bridge cells (SSBC)
b) Single delta bridge cells (SDBC)
c) Double star chopper cells(DSCC)
d) Double star bridge cells(DSBC)

The vital difference between the chopper and bridge cells are the switches in place of capacitors as presented in below sub-module configuration, Figure 1 [4]-[10], [37].

Single star, Double star chopper cells are shown in Figure 1. The current flowing through the R phase top limb, bottom limb, circulating current and R phase currents are represented by 'it_r', 'i_{lr}', 'i_{cir}', 'i_r' respectively. By virtue of KCL on Figure 1;

$$it_r = i_{cir} + \frac{i_r}{2} \quad (1)$$

$$i_{lr} = i_{cir} - \frac{i_r}{2} \quad (2)$$

$$i_{cir} = \frac{1}{2}\,(i_{tr} + i_{lr}) \quad (3)$$

The circulating current consists of both alternating currents (ac) components and direct current (dc) components as follows:

$$i_{cir} = \overline{i_{cir}} + \widetilde{i_{cir}} \quad (4)$$

This circulating current is the unique feature of this topology. This current consists of both DC & AC component, where the DC component is:

$$\overline{i_{cir}} = \frac{i_0}{3} \quad (5)$$

Where 'i_o' is the total output current

In order to find out voltage for the 'R' phase, KVL is applied to Figure 1. Then the voltage across the R phase top limb, 'Vt_r'and resistance, R_{top}, for bottom limb, 'V_{lr}' and resistance, R_{low}, circulating currents, 'i_{cir}', with supply voltage, 'V_{dc}', 'Vnt_r' represents the voltage of limb 'n', and 'N' represents the number of modules.

$$V_{tr} = \frac{Vdc}{2} - \sum_{n=1}^{N} Vnt_r - L_{top}.\frac{d_{itr}}{dt} - R_{top}\,.\,i_{tr} \quad (6)$$

$$V_{lr} = -\frac{Vdc}{2} + \sum_{n=N+1}^{2N} Vnl_r + L_{low}.\frac{d_{ilr}}{dt} + R_{low}\,.\,i_{lr} \quad (7)$$

Applying (1) & (2) in Equation (6) and (7), we have:

The total 'R' phase ac output voltage 'V_{acout}' is equation (6) + (7),

$$V_{acout} = \tfrac{1}{2}\left[\sum_{n=N+1}^{2N} Vntr - \sum_{n=1}^{N} Vlnr\right] - L_{top+low}.\frac{d_{ir}}{dt} - R_{top+low}\,.\,i_r \quad (8)$$

In verdict, the output voltage depends upon the current 'i_r' and the difference of voltage in the modules. From Equation (8), as long as the $L_{top+low}$ will be present in the circuit; losses will occur; the output voltage will vary.

This circulating current can be expressed as:

$$L_{tot}\,.\,\frac{d_{icir}}{dt} + R_{tot}\,.\,i_{cir} = \frac{V_{dc}}{2} - \frac{\left[\sum_{n=N+1}^{2N} Vntr - \sum_{n=1}^{N} Vlnr\right]}{2} = \frac{V_{cir}}{2} \quad (9)$$

As shown in the Equation (9) , '$L_{tot}\,.\,\frac{d_{icir}}{dt} + R_{tot}\,.\,i_{cir}$' is the voltage drop in one limb that can also be referred as the difference between lower and upper arm voltages. The outcomes of the above equation are:

a) The arm voltage drop is equal to the difference of source voltage and sum of voltages of upper and lower modules.
b) The 'i_{cir}' depends upon the source voltage 'V_{dc}' and sum of cell voltages.
c) Consequently, by adding or subtracting the same amount of voltage from both arms will not result in any substantial change the AC side output voltage, but it affects circulating current.

The upper and lower arm voltages inclusive of sub modules are shown in Equation (10) and (11):

$$V_{tr} = \sum_{n=1}^{N} Vntr = \frac{V_{dc}}{2} - V_{tr} + \sum \frac{V_{tr}}{2} \quad (10)$$

$$V_{lr} = \sum_{n=N+1}^{2N} Vnlr = \frac{V_{dc}}{2} + V_{lr} + \sum \frac{V_{tr}}{2} \quad (11)$$

2.1. Modulation Strategies

From the exhaustive survey of literature, it classifies primarily two methods of modulation strategies depending upon the operation of MMC [11]-[21].

a) Zero voltage applied to the arm inductors.
b) Voltage applied to the arm inductors.

1) With this strategy, the voltage provided by the upper and lower inductors are zero i.e. $V_{tr} = V_{lr}$. Hence the voltage levels provided by them are 0 or $\frac{V_{DC}}{N}$, hence the number of levels obtained from them is N+1 and the numbers of inserted cells are constant.

2) In this case, upper and lower cells have different voltage levels V_{tr} and V_{lr}, so as to generate different voltage across the limbs. This leads to higher number of voltage levels in the output voltage which is equal to 2N+1. Here the numbers of inserted cells are not constant, which may be equal to N+1, N, N-1. In this method, the circulating current can be controlled, but due to the presence of circulating currents; higher ripples will come in to the picture. However, to reduce the ripple content, a large number of inductors are required.

Considering the five levels MMC as represented in Figure 1, the switching operations are shown in table below. For understanding purpose the top four switches S_1,S_2,S_3,S_4 are shown as I_1,I_2,I_3,I_4 and the bottom four switches as I_6,I_7,I_8,I_9 for a leg. In the other hand, the auxiliary switches are in opposite manner of the main switches with a delay; this is explained in Table 2 and 3. In the Table 1, the switching states for a MMI are shown. The state of, '1' indicates the switch is in ON condition and OFF for '0'.Primarily it consists of 'one' state of 'V/2'output voltage and '16' states of 'V/4' output voltage and '16' states of '0' voltage. The Table 2 shows the basic operations of redundancies switch state condition of one upper limb. Finally the Table 3 shows the capacitor charging status of upper limb. Table 2 and Table 3 indicates the redundant switching and capacitor status in one sub module .Upward arrow indicates the capacitor charging and else discharging.

Table 1. Basic Switching Operation of a Five Level MMC

State	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	State
$+v/2$	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	$-v/2$
	1	1	1	0	1	0	0	0	0	0	0	1	0	1	1	1	
	1	1	1	0	0	1	0	0	0	0	0	1	1	1	0	1	
	1	1	1	0	0	0	0	1	0	0	0	1	1	1	1	0	
	0	1	1	1	1	0	0	0	1	0	0	0	0	1	1	1	
	0	1	1	1	0	1	0	0	1	0	0	0	1	0	1	1	
	0	1	1	1	0	0	1	0	1	0	0	0	1	1	0	1	
	0	1	1	1	0	0	0	1	1	0	0	0	1	1	1	0	$-v/4$
	1	0	1	1	1	0	0	0	0	1	0	0	0	1	1	1	
	1	0	1	1	0	1	0	0	0	1	0	0	1	0	1	1	
	1	0	1	1	0	0	1	0	0	1	0	0	1	1	0	1	
$v/4$	1	0	1	1	0	0	0	1	0	1	0	0	1	1	1	0	
	1	1	0	1	1	0	0	0	0	0	1	0	0	1	1	1	
	1	1	0	1	0	1	0	0	0	0	1	0	1	0	1	1	
	1	1	0	1	0	0	1	0	0	0	1	0	1	1	0	1	
	1	1	0	1	0	0	0	1	0	0	1	0	1	1	1	0	
	1	1	1	0	1	0	0	0	0	0	0	1	0	1	1	1	
	1	1	1	0	0	1	0	0	0	0	0	1	0	1	1	1	
	1	1	1	0	0	1	0	0	0	0	0	1	1	0	1	1	
	1	1	1	0	0	0	1	0	0	0	0	1	1	1	0	1	
	1	1	1	0	0	0	0	1	0	0	0	1	1	1	1	0	
	1	1	0	0	1	1	0	0	1	0	1	0	1	1	0	0	
	1	1	0	0	0	1	1	0	1	0	1	0	0	1	1	0	
	1	1	0	0	0	0	1	1	1	0	1	0	0	0	1	1	
	1	1	0	0	1	0	0	1	1	0	1	0	1	0	0	1	
	1	1	0	0	1	0	1	0	1	0	1	0	1	0	1	0	
0	1	1	0	0	0	1	0	1	1	0	1	0	0	1	0	1	0
	0	1	1	0	1	1	0	0	0	1	0	1	1	1	0	0	
	0	1	1	0	0	1	1	0	0	1	0	1	0	1	1	0	
	0	1	1	0	0	0	1	1	0	1	0	1	0	0	1	1	
	0	1	1	0	1	0	0	1	0	1	0	1	1	0	0	1	
	0	0	1	1	1	1	0	0	1	0	0	1	0	1	1	0	
	0	0	1	1	0	1	1	0	1	0	0	1	0	0	1	1	
	0	0	1	1	0	0	1	1	1	0	0	1	1	0	0	1	
	0	0	1	1	1	0	0	1	1	0	0	1	1	0	1	0	
	0	0	1	1	1	0	1	0	1	0	0	1	0	1	0	1	
	0	0	1	1	0	1	0	1	0	1	0	1	1	0	1	0	
	1	0	0	1	1	1	0	0	0	1	0	1	0	1	0	1	

Table 2. Basic Switching Operation of a Redundance Switching State in MMC

State	Current	Switching	Capacitor	Capacitor
1010	$i_a > 0$	S_1 D_2 S_4 D_3	$Cs_2\uparrow$	$Cs_4\downarrow$
1010	$i_a < 0$	S_2 D_1 S_3 D_4	$Cs_4\uparrow$	$Cs_2\downarrow$
0110	$i_a > 0$	S_2 D_1 S_4 D_3	$Cs_1\uparrow$	$Cs_4\downarrow$
0110	$i_a < 0$	S_2 D_1 S_4 D_3	$Cs_4\uparrow$	$Cs_1\downarrow$
0101	$i_a > 0$	S_2 D_1 S_3 D_4	$Cs_1\uparrow$	$Cs_3\downarrow$
0101	$i_a < 0$	S_1 D_2 S_4 D_3	$Cs_3\uparrow$	$Cs_1\downarrow$
1001	$i_a > 0$	S_1 D_2 S_3 D_4	$Cs_1\uparrow$	$Cs_3\downarrow$
1001	$i_a < 0$	S_2 D_1 S_4 D_3	$Cs_3\uparrow$	$Cs_2\downarrow$

Table 3. Basic Capacitor Switching Operation of a Redundance Switching State in MMI

S_1	S_2	V_{out}	Current	Power	Capacitor
On	Off	0	$i_{out} > 0$	S_1	Undefined
On	Off	0	$i_{out} < 0$	D_1	Undefined
Off	On	V_{dc}	$i_{out} > 0$	D_2	Charge
Off	On	V_{dc}	$i_{out} < 0$	S_2	Discharge

Due to the uneven voltage distribution in the legs of a phase, circulating currents will flow through the system. It consists of current harmonics which deteriorates the system performance. Here, an attempt is made to derive the current harmonics present in circulating currents and its necessary controller to suppress the same. The instantaneous voltage across the capacitors are denoted as V_{c1}, V_{c2}, V_{c3}, V_{c4}…. V_{cN} Also the voltage distribution across the capacitors is considered to be the same.

$$V_{c1} = V_{c2} = V_{c3} = V_{c4}\ldots. = V_{cN}. \tag{12}$$

Under any switching conditions, the average voltage across the upper arm switches are shown as:

$$\frac{V_{C_u}}{N} = \frac{V_{Dc} + \Delta V_{cu}}{N} \tag{13}$$

The total capacitor voltage of the capacitor is shown in Equation (3) and the deferential capacitor voltage is shown in the Equation (4), in the same way Equation (16), (17) and(18) for the lower limb.

$$V_{C_u} = V_{c1} + V_{c2} + V_{c3} \ldots. V_{cN}. \tag{14}$$

$$\Delta V_{C_u} = \Delta V_{c1} + \Delta V_{c2} + \Delta V_{c3} \ldots. \Delta V_{cN}. \tag{15}$$

$$\frac{V_{C_l}}{N} = \frac{V_{Dc} + \Delta V_{CL}}{N} \tag{16}$$

$$V_{CL} = V_{c(N+1)} + V_{c(N+2)} + \ldots. V_{c2N} \tag{17}$$

$$\Delta V_{CL} = \Delta V_{c(N+1)} + \Delta V_{c(N+2)} + \ldots. \Delta V_{c2N} \tag{18}$$

The circulating currents in the arm inductors consists of both DC and AC components. These AC components are called as the harmonics, since those are rotating with the higher frequencies in the system.

$$i_{cir} = \frac{\mathrm{i_{dc}}}{3} + \sum_{n=1}^{\infty}(\mathrm{i_{acn}}) \tag{19}$$

$$i_{cir} = \frac{\mathrm{i_{dc}}}{3} + \mathrm{i_{ac1}} + \mathrm{i_{ac2}} + \mathrm{i_{ac3}} + \ldots. i_{acn} \tag{20}$$

In order to derive the circulating voltage and current, we need the output voltage of a single phase from the three phase:

$$V_R = \frac{V_{dc}.m.\sin(\omega_o t)}{2} \quad (21)$$

$$I_R = I_o.\sin(\omega_o t - \varphi) \quad (22)$$

'm' is the modulation index of a signal. Yet again, the actual voltages are shown below:

$$V_{acu} = N.\frac{V_{dc}}{2}(1 - m.\sin(\omega_o t))\ (V_{ac} + \Delta V_{cu}) \quad (23)$$

$$V_{acl} = N.\frac{V_{dc}}{2}(1 + m.\sin(\omega_o t)(V_{ac} + \Delta V_{cl}) \quad (24)$$

Therefore, the total voltage is;

$$V_{ac} = V_{au} + V_{aL} \quad (25)$$

$$= \frac{V_{dc}}{2}\ (1 - m.\sin(\omega_o t))(\Delta V_{cu} + V_{ac}) + \frac{V_{dc}}{2}(1 + m.\sin(\omega_o t)(V_{ac} + \Delta V_{cl})) \quad (26)$$

$$V_{au} + V_{aL} = V_{dc} + \frac{\Delta V_{cu} + \Delta V_{cl}}{2} + \frac{m.\sin\omega_o t.(\Delta V_{au} - \Delta V_{cl})}{2} \quad (27)$$

In order to derive the disturbance voltage for the upper and lower cell capacitors of a leg i.e. $\Delta V_{cv}\ and\ \Delta V_{CL}$;

$$V_{c1} = \frac{1}{C_1}\int i_1(t).dt \quad (28)$$

$$V_{cu} = \frac{1}{C_v}\int i_u(t).N_u.dt \quad (29)$$

At this instance,

$$i_u = \sum_{n=0}^{\infty} i_{un} \quad (30)$$

$$i_L = \sum_{n=0}^{\infty} i_{Ln} \quad (31)$$

$$N_u = \frac{1 - m.\cos\omega t}{2} \quad (32)$$

$$N_L = \frac{1 + m.\cos\omega t}{2} \quad (33)$$

$$V_{cu} = \frac{1}{C_u}\int \sum_{n=0}^{\infty} i_{un}.\frac{1 - m.\cos\omega t}{2} \quad (34)$$

$$V_{cL} = \frac{1}{C_L}\int \sum_{n=0}^{\infty} i_{Ln}.\frac{1 - m.\cos\omega t}{2} \quad (35)$$

$$C_V = C_1 + C_2 \ldots . C_n \quad (36)$$

$$C_L = C_{n+1} + C_{n+2} \ldots . C_{2n} \quad (37)$$

Now, let's consider about the current

$$i_{au} = i_{dc} + i_{a1} + \sum_{n=2}^{\infty} i_{ac}n \quad (38)$$

i_{au} → The current present in the phase 'a' upper arm

i_{dc} → Dc component of the current

i_{ac} → Fundamental component of the current

$i_{ac}.n$ → Harmonic component of current.

$$i_{aL} = i_{dc} - i_{a1} + \sum_{n=2}^{\infty} i_{ac}.n \quad (39)$$

$$i_{ac} = i_{ac}m.\cos(n\omega t + \varphi_n) \quad (40)$$

∴ The total current $i_a = i_{au} + i_{aL}$ (41)

$$i_a = (i_{dc} + i_{a1} + \sum_{n=2}^{\infty} i_{ac}.n) + (i_{dc} - i_{a1} + \sum_{n=2}^{\infty} i_{ac}.n) \quad (42)$$

Now, let's consider about voltage for 'N' module in terms of capacitance:

$$i_a = I_o.\sin(\omega t - \varphi) \quad (43)$$

$$= (i_{dc} + i_{a1} + \sum_{n=2}^{\infty} i_{ac}.n) + (i_{dc} - i_{a1} + \sum_{n=2}^{\infty} i_{ac}.n) \quad (44)$$

$$\Delta V_{CU} = \frac{1}{2C}.N.\int(1 - m.\sin(\omega_o t).(\frac{i_a}{2} + \frac{i_{dc}}{3} + \sum_{n=1}^{\infty} i_{acn}).dt \quad (45)$$

$$\Delta V_{CL} = \frac{1}{2C}.N.\int(1 + m.\sin(\omega_o t).(-\frac{i_a}{2} + \frac{i_{dc}}{3} + \sum_{n=1}^{\infty} i_{acn}).dt \quad (46)$$

∴ The total 'R' phase voltage is shown in Equation (47)

$$V_a = V_{aU} + V_{aL} \quad (47)$$

By substituting Equation (45) and (46) in Equation (47); we shall have

$$= V_{dc} + \left(\frac{\Delta V_{CU} + \Delta V_{CL}}{2}\right) + \left(\frac{m\sin(\omega_o t).\Delta V_{CU} - m\sin(\omega_o t).\Delta V_{CL}}{2}\right) \quad (48)$$

$$= V_{dc} + \frac{1}{2C}.N.\int(1 - m.\sin(\omega_o t).(\frac{i_{aU}}{2} + \frac{i_{dc}}{3} + \sum_{n=1}^{\infty} i_{acn}).dt + \frac{1}{2C}.N.\int(1 + m.\sin(\omega_o t).(-\frac{i_{aL}}{2} + \frac{i_{dc}}{3} + n=1\infty iacn).dt \quad (49)$$

$$= \frac{m\sin(\omega_o t).\frac{1}{2C}.N.\int(1 - m.\sin(\omega_o t).(\frac{i_{aU}}{2} + \frac{i_{dc}}{3} + \sum_{n=1}^{\infty} i_{acn}).dt}{2} - \frac{m\sin(\omega_o t).\frac{1}{2C}.N.\int(1 + m.\sin(\omega_o t).(-\frac{i_{aL}}{2} + \frac{i_{dc}}{3} + \sum_{n=1}^{\infty} i_{acn}).dt}{2} \quad (50)$$

From above it can be concluded that, the system consists of both dc and ac components. Most important issue here is the steady state of a system with controller, if applied. To maintain its fundamental and eliminate the dc and ac components, a controller is needed to be implemented in the system. The controller should be designed so as to be fully suffice the Equation (51) and Equation (52).

$$=> [\int(1 - m\sin\omega_o t)\frac{i_{dc}}{3} + (1 - m\sin\omega_o t).\sum_{n=1}^{\infty} i_{acn}] = 0 \quad (51)$$

$$=> \frac{i_{dc}}{3} + \sum_{n=1}^{\infty} i_{acn} = 0 \quad (52)$$

From the Equation (51) and Equation (52), it is found that, load voltage depends upon the current i_V, difference between upper & lower capacitors; i_{cir} depends only on the DC link voltage, the sum of the arm voltages [36].

3. CONTROLLER DESIGN AND FAULT TOLERANT OPERATION OF MMC

One important problem associated with modular multilevel converter is the issue of circulating current at balanced and unbalanced load condition. Mainly two types of conditions are considered and as follows:

a) Under balanced condition, only positive sequence of current will flow in the buffer inductor/arm inductor.
b) Under unbalanced condition, all positive, negative and zero sequence of current will flow.

For better understanding, it can broadly classified as follows,

a) Inner current suppression of a MMC
b) Circulating current suppression method
c) Capacitor voltage balancing method
d) Synchronous Sampling Control and its effect
e) Dual Vector Control
f) Estimation of energy by using arm inductance and stored capacitance

Form the Equation (49) and Equation (50) one can conclude that, as the arm inductance increases, the circulating current decreases. Due to this effect there is an increase in the value of inductance, the cost and space requirement will also increase. It urges the need to control the circulating current instead of increasing inductance. It [22] proposes, under balanced conditions, negative sequence component of circulating current in each arm rotates at double the line frequency. So, Δ control method was stated by transforming the a-c-b sequence with a double line frequency into d-q sequence at rotational reference frame. But this method was not been able to eliminate the circulating current totally at underbalanced conditions. As per the article [23] a proposed control method with realization of instantaneous power of each leg, and also an algorithm to reduce the circulating currents and d-c link voltages ripples. Unfortunately it has a disadvantage of inclusion of double line frequency ripple. In [24], proposed a-b-c reference frame to control the circulating currents but have the disadvantage of generating a delay however, it cannot improve the transient response occurring in the inner balancing currents. Again in [25] proposed a model of predictive control which took ac-side current, circulating currents and sub-module voltage balancing, by detecting the switch status to minimize the cost function. But, this study [26] analyses each individual phase's instantaneous power to reduce the active power ripple, when negative sequence component was generated. This instantaneous power begins with the positive, negative and zero sequence components with double frequencies and dc components. The disadvantage of this method is the use of a complicated PIR notch filter used to control each component separately. Due to unbalance in the upper and lower arm of the MMC, circulating currents will develop. These even harmonics and circulating currents can be suppressed by using a controller and designed as follows.

$$\text{Re } h(s) = \frac{K_h . S}{s^2+(k\omega_0)^2} \qquad (h = 2, 4, 6\ldots\ldots) \tag{53}$$

$$H(s) = \frac{i_{cir(s)}}{i_{cir_r.f\,(s)}} = \frac{2Ls\,(\sum_{h=2,4,6\ldots} \frac{K_h.S}{s^2+h(\omega 0)^2})}{1+2Ls\,(\sum_{h=2,4,6\ldots} \frac{K_h.S}{s^2+(h\omega 0)^2})} \tag{54}$$

But i_{cir} will consist of the DC components also.

$$H_c\,(j_o) = \frac{2Lj\omega\,(\sum_{h=2,4} \frac{-jK_h.\omega}{-\omega^2+(h\omega 0)^2})}{1-2Lj\omega\,(\sum_{h=2,4} \frac{-jK_h.\omega}{-\omega^2+(h\omega 0)^2})} \tag{55}$$

By considering the upper arm, the output voltage of the upper arm is, $V_{top} = V_{dc}/4$, which lies in between: $k_1 * V_{top} < V_{top} < (k_1+1)\, V_{top}$; where k_1 is a positive integer, K_h is a proportional constant. In order to produce a voltage 'V_r' at a certain time, k_1 sub-module capacitors will be insufficient and if we consider (k_1+1), sub-module capacitors then it will generate over voltage. Hence, k_1 module is taken as I_r to provide major part, and (k_1+1) is taken as O_μ for the remaining part.

$$k_1 = \int \frac{V_r}{V_{rtop}} = \int \frac{V_r}{(\frac{V_{dc}}{N})} \tag{56}$$

Then the reference voltage can be calculated as:

$$V_{r\_ref} = V_r - k_1 . \frac{V_{dc}}{N} \tag{57}$$

In order to control the voltage balancing of the sub module capacitor there are two effective ways

a) Virtual loop mapping
b) Selective virtual loop mapping

The above mentioned two methods are based on the comparison of the capacitor voltage. In this method a counter up counter method is deployed to control the mapping relations which will be equal to or less than the carrier frequency. The range of counter is 0-(Counter-1) [27]-[35].

The above method is applicable only when the system is operated at well balanced conditions. But the system will retain such a position in practical due to variation in circulating currents, modulation singles. Conclusively, the accuracy of the method is applicable here. From the literature [36]-[37], a method is proposed where there is a need to sort the capacitor voltages frequently resulting consumption of more time & implementation of an avoidable complicacy in the hardware(complex at higher voltage levels).

Instead, once the maximum and minimum values of capacitor voltages and their corresponding directions can be picked. In order to minimize the delay of PWM signal, a synchronous sampling control is implemented. Here [47]-[53], it is considered with a continuous model instead of discrete model, due to the following advantages:

a) Discrete model do not allow an analytical approach to model the converter and design the control system.
b) Numerical solutions of sub-module with higher number of switching actions require considerable time.

Therefore adding some voltage will not affect the load voltage but it will affect the current, then the total circulating current will be controlled and system can maintain steady state condition.

$$\frac{V_{dc}}{2} - \frac{R}{2} i_{load} - \text{R. } i_{cir} - \frac{L}{2}\frac{d}{dt}(i_{load}) - \text{L. } \frac{d}{dt}(i_{cir}) - V_{ct} = V_R \quad (57)$$

$$V_{cu} = \frac{V_s}{2} - V_u - \frac{R}{2} i_{load} - \text{R. } i_{cir} - \frac{L}{2}\frac{d}{dt}(i_{load}) - \text{L. } \frac{d}{dt}(i_{cir}) \quad (58)$$

$$V_r + \frac{R}{2} i_{load} + \frac{L}{2}\frac{d}{dt}(i_{load}) = \frac{V_{cLow} - V_{ctop}}{2} \quad (59)$$

By taking the difference, $\frac{V_{cLow} - V_{ctop}}{2}$ =ev (error voltage) (60)

$$V_{ctop} = \frac{V_{top}}{2} - \text{ev} - V_{cir} \quad (61)$$

$$V_{cLow} = \frac{V_{dc}}{2} + \text{ev} - V_{cir} \quad (62)$$

So, V_{diff} = R. i_{cir} + L. $\frac{d}{dt}(i_{cir})$ (63)

In order to determine the difference voltage between the upper and lower capacitors, one should find the energy stored in the capacitor.

$$E^{\in}_{rtop} = \frac{C^{arm}}{2} (V^{\in}_{rtop})^2 = \text{N. } [\frac{C}{2}(V^{\in}_{rtop}/N)^2 \ ] \quad (64)$$

$$E^{\in}_{rlow} = \frac{C^{arm}}{2} (V^{\in}_{rlow})^2 = \text{N. } [\frac{C}{2}(V^{\in}_{rlow}/N)^2 \ ] \quad (65)$$

The change in energy stored in the capacitor is:

$$\frac{d}{dt}(E^{\in}_{cu}) = i_{uv}. V^{\in}_{cu} = (\frac{i_V}{2} + i_{cir})(\frac{V_s}{2} - \text{ev} - V_{cir}) \quad (66)$$

$$\frac{d}{dt}(E^{\in}_{cL}) = -i_{Lv}. V^{\in}_{cL} = (-\frac{i_V}{2} + i_{cir})(\frac{V_s}{2} + \text{ev} - V_{cir}) \quad (67)$$

The total energy,

$$E^{\in}_{c} = E^{\in}_{rtop} + E^{\in}_{rlow} \quad (68)$$

$$E^{\Delta}_{c} = E^{\in}_{rtop} - E^{\in}_{rlow} \quad (69)$$

Difference is:

$$\frac{d}{dt}(E_c^{\epsilon}) = (V_s - 2V_{cir}).\, i_{cir} - e_V.\, i_V \quad (70)$$

$$\frac{d}{dt}(E_c^{\Delta\epsilon}) = \left(\frac{V_s}{2} - V_{cir}\right).\, i_v - 2e_V.\, i_{cir} \quad (71)$$

Some important conclusions are:

a) $i_{cir}.V_s$ Represents the product of power delivered, $i_{cir}.V_{cir}$ represents the losses occurred in the system, $i_V.e_V$ is the power delivered to the load.
b) In overall, if the i_{cir} is controlled, the system capacitor energy can be controlled.
c) DC component of i_{cir} has no impact on the difference of capacitor energy as there are no DC components in 'ev'. The DC component of i_{cir} can only be used to control the total capacitor energy. But the AC component of i_{cir} having the fundamental frequency as the output voltage 'ev' can be employed to control the capacitor energy.
d) The product of $e_V.i_{cir}$ make the energy to change.
e) V_{diff}, i_V shall give the same effect but this is permissible for small R and L, thus we need to develop a control strategy for e_V, i_{cir} only.

One of other important issue associated with MMC HVDC system is fault tolerance while its applicability. It proposes HVDC system, offers the operational flexibility of VSC based systems in terms of active and reactive power control, black start capability, in addition to improved ac fault ride-through capability and the unique feature of current-limiting capability during dc side faults. This [31] paper proposed a protection scheme to implement fast fault clearance and automatic recovery for nonpermanent faults on dc lines. By employing double thyristor switches, the freewheeling effect of diodes is eliminated and the dc-link fault current is allowed to freely decay to zero. In order to mitigate the circulating currents of the MMC, computer simulation is carried out first and then verified experimentally with a combination of repetitive controller and harmonic elimination technique.

Table 4. Parameters Used for Five Level MMC Simulation and Experiment

MMC Level	Five
DC Voltage	V_{dc}=200V Dc
Circulating Current reference	I_{cref} = 0
Arm Inductors	L_1=L_2=L=3 mH
Switching frequency	S_f=100 Hz
Capacitor Value	C=16 µF/400V
Bandwidth of the controller	$\omega_c = 2000$
Load Parameters	L_r=10mH/R_r=30Ω
Gain of Resonant controller	Gr_c=1250
Resonant frequency of controller	ω_0=2000

The system has been tested with the parameters listed in Table IV. The experimental setup has been shown in Figure 4.

Figure 4. Experimental setup of five level MMC with controller

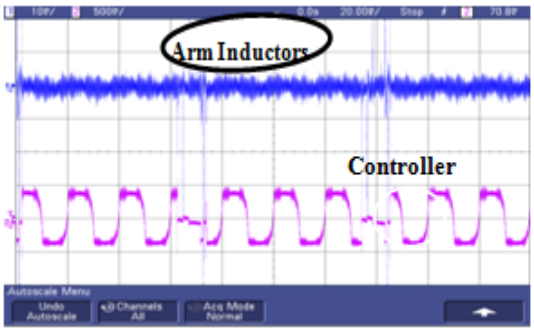

Figure 5. Fault tolerant operation of MMC

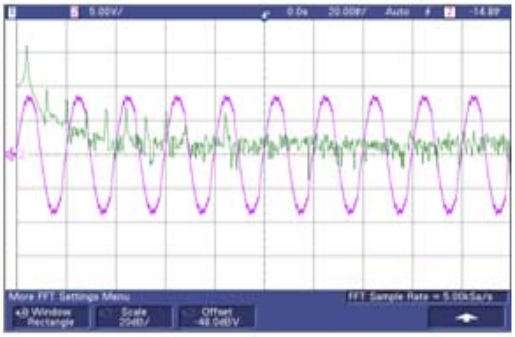

Figure 6. Voltage waveform and its FFT analysis

A model has been incubated and proposed with controller which is suitable for wide range of load with different modulation indexes. Prior to this, the system has been investigated for output voltage and fault tolerant operation. From the Figure 5, it is evident that, for a fault creation of 2 ms, capacitor voltage's got distributed within 3ms. Since, it is one of the important factors to access the controller performance; system without controller is distorted with its actual values and produces unwanted components called as harmonics. As shown in Figure 6, it is evident that output voltage is not distorted the presence of controller and all lower order harmonics are eliminated. The RMS values of phase to neutral current are 31.4A with controller and 29.2A without controller. From those values it is justified that, output current is also distorted due to circulating currents. It is to be kept in mind that each division is considered as 5ms. The results are compared with [8] and shown to better with this control technique.

4. CONCLUSION

Summing up, the following are the significant contributions and remarkable recommendations to explore the MMC towards effective and spatial usage on practical basis. This article justifies the scope of proposed technique by means of simulations and experimental verifications undergone in all the above described portions in a rationalize manner and hence to be treated and absorbed both in experimental and commercial implementation point of view. This article has been successfully reviewed and provides conclusions at the end of the each section to make the MMC more robostic in control for researchers further. Also, it has proposed a controller with detailed explanations. This proposed way of article is simple in understating, design and can substantially eliminate the RMS value of the circulating current compared with the existing method [8], while the voltages of the sub module capacitors are kept well balanced. This way is very helpful for reducing power losses of the MMC in real HVDC applications. The system can be applied to wide range of loads with various modulation indexes. The steady state analysis and harmonics can substantially reduce by the proposed method. It has been given successful recommendations on controller design, losses reduction, fault reduction and for voltage balancing consequently to reduce the circulating currents.

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