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# Islanding Detection of Inverter Based DG Unit Using PV System

**M.Divyasree, L.Venkata Narasimha Rao**
Department of Electrical and Electronics Engineering, K L University, A.P, India

| Article Info | ABSTRACT |
|---|---|
| | Distributed generation (DG) units are rapidly increasing and most of them are interconnected with distribution network to supply power into the network as well as local loads Islanding operations of DG usually occur when power supply from the main utility is interrupted due to several reasons but the DG keeps supplying power into the distribution networks. a new method for islanding detection of inverter-based distributed generation (DG). Although active islanding detection techniques have smaller non detection zones than passive techniques, active methods could degrade the system power quality and are not as simple and easy to implement as passive methods. The phenomenon of unintentional islanding occurs when a distributed generator (DG) continues to feed power into the grid when power flow from the central utility source has been interrupted. A simple islanding detection scheme has been designed based on this idea. The proposed method has been studied under multiple-DG operation modes and the UL 1741 islanding tests conditions and also using a PV system. The simulations results, carried out by MATLAB/Simulink, show that the proposed method has a small Non detection zone.<br><br> |

*Corresponding Author:*

M.Divyasree,
Department of Electrical and Electronics Engineering,
K L University,
A.P, India.
Email: divyasree.madivada@gmail.com

## 1. INTRODUCTION

Distributed generation (DG) provides many potential benefits, such as Lower energy costs, Improved reliability, improved power quality, Greater autonomy, upturn efficiency.In the last few years, small DGs in the range of 100 kW have gained popularity amongst industry and utilities. Anti-islanding detection methods can be divided into two main groups: passive and active methods. In passive methods, the decision whether an islanding condition occurred or not is based on measuring a certain system parameter and comparing it with a predetermined threshold. Active methods are designed to force the DG to be unstable during an islanding situation. In general, islanding detection methods could be classified into three main types that include active, passive, and communication-based methods. Passive methods, which are simple and easy to implement, detect islanding by setting an upper and lower threshold on a system parameter.

Active methods, on the other hand, rely on injecting deliberate disturbances to the connected circuit and then monitoring the response to determine an islanding condition [8]. Active methods include slide-mode frequency shift (SMS) [9], active frequency drift (AFD) or frequency bias [10], and Sandia frequency shift (SFS) [3]. Active methods have smaller NDZ, but, on the other hand, can degrade the power quality of the power system [8]. Other active methods rely on deliberately injecting negative sequence current and disturbance signals into the system through either the direct axis (d-axis) or the quadrature axis (q-axis) current controllers [1], [3] to detect islanding. Communication-based methods have negligible NDZ, but are

much more expensive than the former methods. A survey on the different islanding detection methods could be found in [8] and [9]. Thus, passive islanding detection methods suffer from large Non detection zones (NDZs). NDZs are defined as the loading conditions for which an islanding detection method would fail to operate in a timely manner. To enhance the performance of passive methods, a hybrid passive method based on monitoring the voltage unbalance and total harmonic distortion (THD) was proposed in [7].

This paper presents a new islanding detection method, which has the improvements of active and passive islanding methods, minor NDZ, and excellent precision. The control strategy of the voltage-source inverter has been designed to operate at unity power factor. Also, the dc side has been modelled by a controllable dc voltage source. The main concept of this paper is to change the dc-link voltage considering the PCC voltage changes during the islanding condition.

A simple and easy method like over/under voltage protection (OVP/UVP), can be used to detect an islanding condition. Once the scale of voltage exceeds a determined starting point value, an islanding condition is detected and DG is disconnected.

In this paper, the system is modelled in Section II. The proposed islanding detection method is discussed in Section III. The performance of the proposed method is evaluated in Section IV. The last section consists of conclusions.

## 2. SYSTEM UNDER STUDY

The system, which has been studied in this paper, is shown in Figure 1. This system consists of a distribution network modelled by a three-phase voltage source behind impedance, a load modelled by a three-phase constant impedance, and a DG system. The DG is modelled by a controllable dc voltage source behind a three-phase inverter whose rating is 100 kW. The other parameters have been given in [3], [4], and [5].
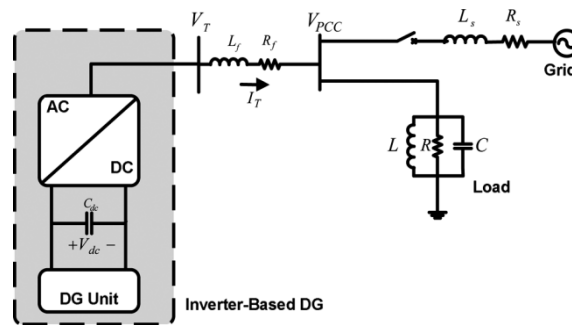


Figure 1. Modelled system

Figure 2 shows the control scheme based on dq synchronous reference frame. In this scheme, the dc-link voltage controller and reactive-power controller determine d and q components, respectively. The input power extracted from the DG unit is fed into the dc link. Hence, the voltage controller counteracts the voltage variation by specifying an adequate value of the d axis inverter current to balance the power flow of the dc link [6]. The reactive power controller, shown in Figure 2, specifies the reference value for the q component of the converter current. The reactive power reference value $Q_{ref}$ is set to zero in order to model a unity power factor DG operation. Also, Figure 2 shows two proportional-integral (PI) controllers for the d- and q-axis current controls. The outputs of controllers obtain the reference voltages for the PWM signal generator. The main features of the current control strategy are the limitation of the converter output current during a fault condition, providing over current protection, and decreasing the fault current contribution of the unit [6]. The instantaneous real and reactive power could be written in terms of the dq axis components, as follows [7], [8]:

$$P = \frac{3}{2} v_{dpcc} \cdot i_{dt} \tag{1}$$

$$Q = \frac{3}{2} v_{dpcc} \cdot i_{qt} \tag{2}$$

Where, $V_{dpcc}$ is the phase peak value of the PCC voltage. $i_{dt}$ and $i_{qt}$ are orthogonal components of inverter currents. The dq components of the voltage and current are constant values in the steady-state condition. Therefore, the controller provides the independent regulation d of q and components [7], [8]. The instantaneous voltages of the three phases could be expressed by the following equation [7], [8]:

$$\frac{d}{dt}i_{t(abc)} = -\frac{Rf}{L_f}i_{t(abc)} + \frac{1}{L_f}[vt_{(abc)} - vpcc_{(abc)}]$$

(3)

Where $i_{t(abc)}$ represents the DG current three-phase components. $R_f$ and $L_f$ are the filter resistance and inductance, respectively. $V_{t(abc)}$ and $v_{pcc(abc)}$ represent the DG terminal and PCC three phase voltages, respectively.
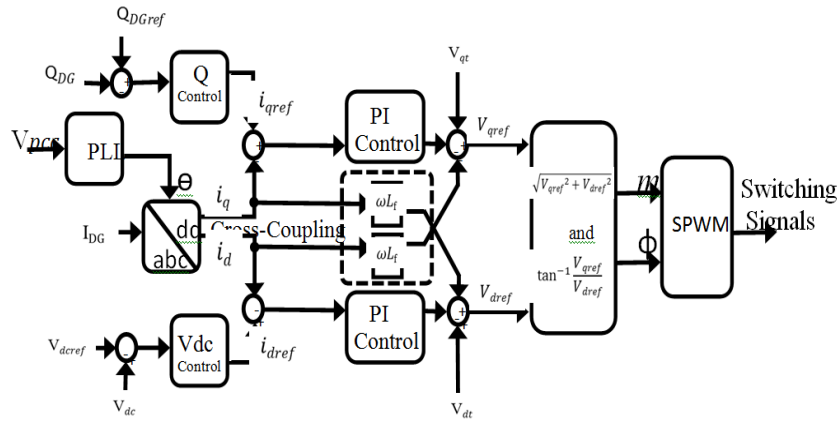


Figure 2. Block diagram of the DG inverter controller.

By using Park's transformation [7], (3) can be transformed to the rotating synchronous reference frame, as follows [3], [7] and [8]:

$$\frac{d}{dt}\begin{bmatrix} i_{dt} \\ i_{qt} \end{bmatrix} = \begin{bmatrix} \frac{-R_f}{L_f} & \omega \\ -\omega & \frac{-R_f}{L_f} \end{bmatrix}\begin{bmatrix} i_{dt} \\ i_{qt} \end{bmatrix} + \frac{1}{L_f}\begin{bmatrix} v_{dt} - vd_{pcc} \\ v_{qt} - vq_{pcc} \end{bmatrix}$$

(4)

Or,

$$\frac{d}{dt}\begin{bmatrix} i_{dt} \\ i_{qt} \end{bmatrix} = \begin{bmatrix} \frac{-R_f}{L_f} & 0 \\ 0 & \frac{-R_f}{L_f} \end{bmatrix}\begin{bmatrix} i_{dt} \\ i_{qt} \end{bmatrix} + \frac{1}{L_f}\begin{bmatrix} v_d \\ v_q \end{bmatrix}$$

(5)

Where,

$$v_d = v_{dt} - vd_{pcc} + \omega L_f i_{qt}$$

(6)

$$v_q = v_{qt} - vq_{pcc} - \omega L_f i_{dt}$$

(7)

The DG interface control is modified by using the set of equations shown in Figure 2. The magnitude and angle of the modulating signal are calculated and then the switching pattern of the inverter has been determined. PWM three-phase inverters should shape and control the three-phase output voltage in magnitude and frequency with the essentially constant input dc voltage [9]. In the linear region (i.e., ma≤ 1.0), the fundamental frequency component in the output voltage ((V_AN )1) determines the amplitude-modulation ratio(ma) , by the following equation [9]:

$$(V_{AN1}) = m_a \frac{v_{dc}}{2}$$

(8)

$$m_a = \frac{v_{control}}{v_{tri}} \tag{9}$$

Where $V_{control}$ is the peak amplitude of the control signal and the $V_{tri}$ is the amplitude of the triangular signal. Therefore, the line-to-line rms voltage at the fundamental frequency can be written, as follows [9]:

$$V_{L\text{-}L(line\text{-}line,rms)} = \frac{\sqrt{3}}{\sqrt{2}}(V_{AN}) = \frac{\sqrt{3}}{2\sqrt{2}}m_a v_{dc}$$
$$\approx 0.612 m_a v_{dc} \ (m_a \leq 1.0) \tag{10}$$

Now, the following equations can be written for $V_{dt}$ and $V_{qt}$:

$$v_{dt} = 0.612 \, m_a \, v_{dc} \cos(\emptyset) \tag{11}$$

$$v_{qt} = 0.612 \, m_a \, v_{dc} \sin(\emptyset) \tag{12}$$

Where $\emptyset$ is the angle by which the inverter voltage vector leads the line voltage vector.

In a lossless inverter, the instantaneous power at the ac and dc terminals of the inverter is equal. This power balance can be written, as follows:

$$v_{dc} \, i_{dc} = \frac{3}{2}(v_{dt} i_{dt} + v_{qt} i_{qt}) \tag{13}$$

At the dc link, we have:

$$i_{dc} = C_{dc} \frac{d}{dt} v_{dc} \tag{14}$$

By using (4) and (11)–(14), the following state equations can be written [7]:

$$\frac{d}{dt}\begin{bmatrix} i_{dt} \\ i_{qt} \\ v_{dc} \end{bmatrix} = [A]\begin{bmatrix} i_{dt} \\ i_{qt} \\ v_{dc} \end{bmatrix} + \begin{bmatrix} \frac{-1}{L_f} & 0 \\ 0 & \frac{-1}{L_f} \\ 0 & 0 \end{bmatrix}\begin{bmatrix} v_{dpcc} \\ v_{qpcc} \end{bmatrix}$$

$$[A] = \begin{bmatrix} \frac{-R_f}{L_f} & \omega & \frac{0.612m_a}{L_f}\cos(\emptyset) \\ -\omega & \frac{-R_f}{L_f} & \frac{0.612m_a}{L_f}\sin(\emptyset) \\ \frac{3\times0.612m_a}{2C_{dc}}\cos(\emptyset) & \frac{3\times0.612m_a}{2C_{dc}}\sin(\emptyset) & 0 \end{bmatrix} \tag{15}$$

## 3. ISLANDING DETECTION METHOD

The acceptable voltage deviation is in the range of 88% to 110% of the nominal voltage [1], [2]. Any voltage deviation in this range should not be detected and the corresponding load condition would be considered within the NDZ. It is assumed that DG has been designed to operate at a constant dc voltage of 900 V. In this section, a new analytical formulation is derived by the linearization of system state equations. Then, a new $V_{dc}$ -$V_{pcc}$ characteristic of DG will be explained, and the performance of this method will be evaluated.

### 3.1. Linearization of System State Equations

To measure the impact of deviation of ma on dc-link voltage, $\emptyset$ has been kept constant and only $m_a$ has been considered as a variable. As a result, (15) is a nonlinear equation. However, for a small perturbation around the equilibrium point ma, the following linear set of equations can be obtained, where subscript 0 denotes steady-state values [7], as shown in (16) at the bottom of the page. The inverter steady-state model can be obtained from the dynamic model by setting the derivative terms equal to zero. After transformation from abc to the dq reference frame, the voltages and the currents become dc quantities.

Hence, substituting:

$$\frac{d}{dt}\begin{bmatrix}\Delta i_{dt}\\\Delta i_{qt}\\\Delta v_{dc}\end{bmatrix} = [\Delta A]\begin{bmatrix}\Delta i_{dt}\\\Delta i_{qt}\\\Delta v_{dc}\end{bmatrix} + [\Delta B]\begin{bmatrix}\Delta v_{dpcc}\\\Delta v_{qpcc}\\\Delta m_a\end{bmatrix}$$

$$[\Delta A] = \begin{bmatrix}\frac{-R_f}{L_f} & \omega_0 & \frac{0.612 m_{a0}}{L_f}\cos\emptyset\\ -\omega_0 & \frac{-R_f}{L_f} & \frac{0.612 m_{a0}}{L_f}\sin\emptyset\\ \frac{3\times0.612 m_{a0}}{2C_{dc}}\cos\emptyset & \frac{3\times0.612 m_{a0}}{2C_{dc}}\sin\emptyset & 0\end{bmatrix}$$

$$[\Delta B] = \begin{bmatrix}\frac{-1}{L_f} & 0 & \frac{0.612.v_{dc0}.\cos\emptyset}{L_f}\\ 0 & \frac{-1}{L_f} & \frac{0.612.v_{dc0}.\sin\emptyset}{L_f}\\ 0 & 0 & \frac{3\times0.612 m_{a0}}{2C_{dc}}\left(\cos\emptyset.i_{dt0}+\sin\emptyset.i_{qt0}\right)\end{bmatrix}$$

$V_{dpcc}=|V_{pcc}|$, $V_{dpcc}= 0$, $i_d=I_d$, and $i_q=I_q$ , and simplification of the steady-state model resulted in the following equation:

$$\begin{bmatrix}-R_f & \omega L_f & 0.612 m_a\cos\emptyset\\ -\omega L_f & -R_f & 0.612 m_a\sin\emptyset\\ 0.612 m_a\cos\emptyset & 0.612 m_a\sin\emptyset & 0\end{bmatrix}\begin{bmatrix}i_{dt}\\i_{qt}\\v_{dc}\end{bmatrix}=\begin{bmatrix}|v_{pcc}1|\\0\\0\end{bmatrix} \qquad (17)$$



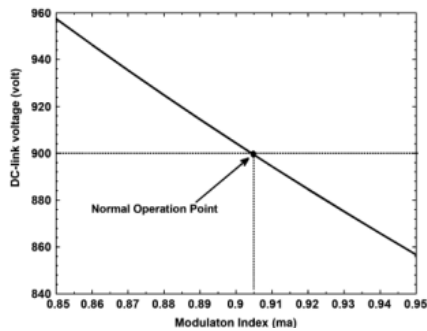Figure 3. Steady-state variations of $V_{dc}$ versus ma (with $L_f$=2.1mH, $\emptyset = 377 rad/s$, $R_f$=0.00145Ω, $\emptyset$=$20^0$ and $V_{pcc}$=1p.u



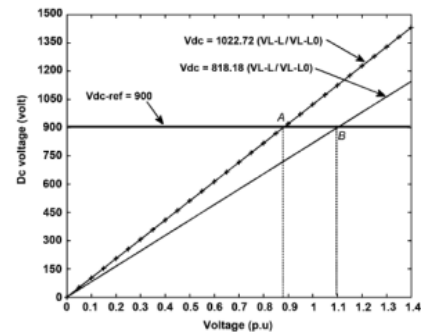Figure 4. DC voltage versus PCC voltage characteristic (DG and $V_{dc-ref}$ are set to 900 V)

By solving (17) for $i_{dt}$, $i_{qt}$ and $V_{dc}$, we have:

$$I_{dt} = \frac{\cos(2\emptyset)-1}{2R_f}|v_{pcc}| \qquad (18)$$

$$I_{qt} = \frac{\sin(2\emptyset)}{2R_f}|v_{pcc}| \qquad (19)$$

$$v_{dc} = \frac{(1.634\,R_f\cos\emptyset)-(1.634\,\omega L_f\sin\emptyset)}{R_f\,m_a}|v_{pcc}| \qquad (20)$$

Considering (18) and (19), it is obvious that $I_{dt}$ and $I_{qt}$ do not depend on the modulation index (ma). For the given system, the variations of $V_{dc}$ versus ma can be determined by using (20). By considering it as a constant value, (20) becomes a hyperbolic equation. But the part ma<0 is not acceptable and just the part 0<

ma<1 is the dominant. By scaling between 0.8 and 1, it can be seen that the deviation of ma versus $V_{dc}$ is linear and usually the normal operating point of the inverter is in this range. The Vdc-ma curve of this range has been shown in Figure 3 Considering (10), we have:

$$V_{dc0} = \frac{V_{L-L}}{0.612 \cdot m_a} \tag{21}$$

In steady-state condition, (10) can be written as follows:

$$V_{dc0} = \frac{V_{L-L0}}{0.612 \cdot m_{a0}} \tag{22}$$

By combining (21) and (22), we have:

$$V_{dc} = V_{dc0} \cdot \left(\frac{V_{L-L}}{V_{L-L0}}\right) \cdot \left(\frac{m_{a0}}{m_a}\right) \tag{23}$$

Considering (20) and Figure 3, it is obvious that the deviation of ma around the operating point does not have any major impact on drifting of the dc-link voltage. Therefore, the modulation index can be assumed to be constant (i.e.$m_a = m_{ao}$). Then, (23) can be written as follows:

$$V_{dc} = V_{dc0} \cdot \left(\frac{V_{L-L}}{V_{L-L0}}\right). \tag{24}$$

### 3.2. $V_{dc}$ - $V_{pcc}$ Characteristic

The $V_{dc}$ - $V_{pcc}$ (VL-L) characteristic of DG and dc reference voltage has been shown in Figure 4. In this figure, there are 2 lines which presenting the lower and upper dc voltage limits. Using (24) and assuming $V_{L-Lo}$ equal to 1 p.u, the slope of these lines ($V_{dco}$)can be determined for $V_{rmdc}$ =900 V and the dc voltage limits. The intersect point of DG and dc-link reference voltage curves is called the islanding operating point. In this figure, points "A " and " B" represent the operating point of the lower and upper dc-link voltage limits, respectively. Each operating point between these two lines is in the NDZ. In addition, in any kind of loading condition, the dc-link voltage would be placed within or without these boundaries. If $V_{dc}$ is accommodated within these limits, the voltage deviation will be in the allowable values, and islanding can occur and will not be detected (NDZ). In this paper, the DG reference dc voltage curve has been modified and expressed by the PCC voltage-dependent line.
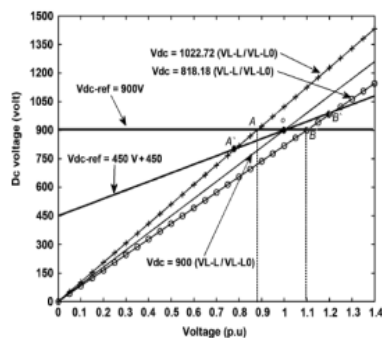


Figure 5. DC voltage versus the PCC voltage characteristic for DG and modified $V_{dc\text{-}ref}$
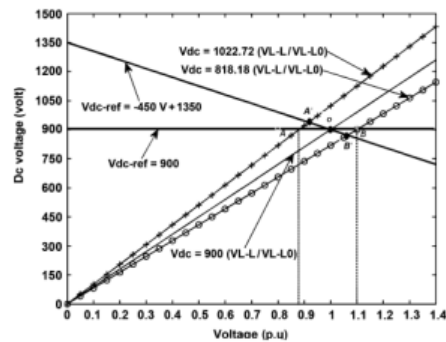
Figure 6. DC voltage versus the PCC voltage characteristic, effect of negative slope

This line should cross the point which has the rated dc voltage at the rated PCC voltage. It can be expressed by the following equation:

$$V_{dc-ref} = k_1 \cdot V_{PCC} + k_2. \tag{25}$$

Figure 5 presents the dc voltage versus the PCC voltage lines for three (dc voltage) conditions. By changing "A" and "B" points to "A" and "B," the NDZ is smaller, because these new points are outside the allowable voltage limits (88% and 110% of nominal voltage), so this condition can be easily detected.

As an example, the DG reference dc voltage can be rewritten as:

$$V_{dc-ref} = 450 . V_{PCC} + 450. \tag{26}$$

The load condition, which intersects the DG voltage line at point O, has an active power of 100 kW and the voltage of 1 p.u. Equation (26) intersects the lower and upper limits at point A and point B respectively. These points correspond to voltage levels that are beyond the allowable voltage levels. Thus, these loading conditions can be easily detected by using the over/under voltage protection (OVP/UVP) methods. As a result, a reduction in the NDZ can be achieved. The reference dc voltage can be expressed by a negative slope as:

$$V_{dc-ref} = -450 . V_{PCC} + 1350. \tag{27}$$

Figure 6 presents the dc voltage versus PCC voltage lines for the same conditions, shown in Figure 5. The lower and upper limits intersect the new DG line by (27) at points "A' " and "B'," respectively. The voltage levels of these two points are in the NDZ. Therefore, these loading conditions will not be detected by using OVP/UVP methods. Therefore, the negative slope in (27) will lead to an increase in the NDZ and the positive slope can reduce the NDZ. The values of parameters k1 and k2have been chosen so that the DG $V_{dc}$-$V_{pcc}$ slope is placed higher than the slope of all possible load lines within the NDZ. Considering (24), the following equations have been used to tune k1 and k2
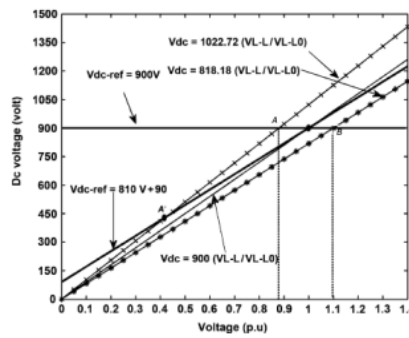


Figure 7. DC voltage versus the PCC voltage characteristic,with an effect of the Selection of (31)

$$\frac{V_{dc}-V_{dc0}}{V_{L-L}-V_{L-L0}} = \frac{dV_{dc}}{dv}|V_{L-L} = V_{L-L0} \tag{28}$$

$$\frac{V_{dc}-V_{dc0}}{V_{L-L}-V_{L-L0}} = \frac{V_{dc0}}{V_{L-L0}} \tag{29}$$

$$V_{dc} = \frac{V_{dc0}}{V_{L-L0}}V_{L-L} \tag{30}$$

Based on these equations, it can be stated that k1=Vdc0/VL-Lo (Vdco=900volts, VL-LO=1p.u.) and k2=0 are a suitable condition. But it must be mentioned that k2 cannot be equal to zero. This is because if k1=900 and k2=0, then the system will be very sensitive to PCC voltage perturbations,

And it will lead to undesirable system tripping. To protect the system from this situation based on the simulation results and IEEE 1547 Standard and other power system standards (the allowable voltage deviation for DGs below 500 kVA is 10% of the nominal voltage), is supposed to have a good choice for k2, when it is about 10% of the dc link voltage. As a result, (25) has been changed into the following form:

$$V_{dc-ref} = 810 . V_{PCC} + 90. \tag{31}$$

### 3.3. Performance Evaluation

The performance of the proposed islanding detection method as well as its NDZ depends on the Vdc-Vpcc DG characteristic. A PCC voltage variation (ΔV) will result in a dc-link voltage variation (ΔV) dc which could be expressed as:

$$V_{dc-ref} = V_{dc} \cdot \left(\frac{V_{L-L}}{V_{L-L0}}\right) = k_1 . V_{L-L} + k_2 \tag{32}$$

$$(V_{dc0} + \Delta V_{dc})\left(\frac{V_{L-L}(1+\Delta V)}{V_{L-L0}}\right) = k_1 \times V_{L-L0}(1+\Delta V) + k_2 \tag{33}$$

$$(V_{dc0} + \Delta V_{dc}) = \frac{k_1 \times V_{L-L0}(1+\Delta V) + k_2}{(1+\Delta V)} \tag{34}$$

Table 1 shows the calculated NDZs for different values of k1 and k2. The selection of the $V_{dc}$ - $V_{pcc}$ characteristic will have a great impact on NDZ. If the boundary between lower and upper limits of NDZ is a large number, it will lead to a wide NDZ. In some cases, NDZ has a large gap (e.g., case No. 2), while for other cases, it is relatively small (e.g., case No. 3). NDZ can either be represented in terms of power mismatch or in terms of the load R, L, and C. An accurate presentation of the NDZ can be found in [5].

Table 1: Ndz Upper Andlowerlimits Fordifferent $V_{dc}$ - $V_{pcc}$

| Case Number | $k_1$ | $k_2$ | Lower limit of NDZ | Upper limit of NDZ |
|---|---|---|---|---|
| 1 | 450 | 450 | 825 | 1092.9 |
| 2 | -450 | 1350 | 675 | 1478.6 |
| 3 | 810 | 90 | 885 | 938.5 |

The Details have been presented in the Appendix. This paper examines the NDZ of an OVP/UVP and OFP/UVP islanding scheme in case of using the implemented $V_{dc}$ - $V_{pcc}$ characteristic for different amounts of k1 and k2 . The results have been plotted in Figure 8.
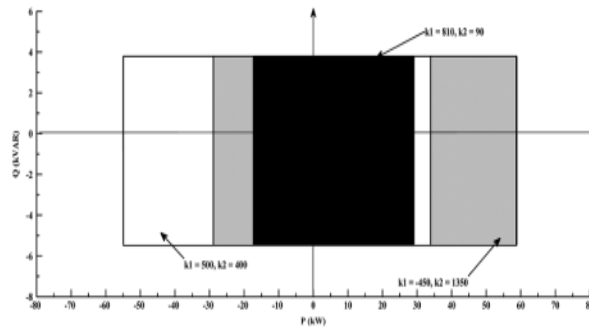


Figure 8. NDZ of the $V_{dc}$ -$V_{pcc}$ characteristic for a different amount of k1 and $k_2$

## 4. MATLAB /SIMULINK RESULTS

Table 2. System, DG, and load parameters

| Grid and Inverter Parameters | |
|---|---|
| DG Output power | 100kW |
| Switching Frequency | 8000Hz |
| Input DC Voltage | 900V |
| Voltage (Line to Line) | 480V |
| Frequency | 60Hz |
| Grid Resistance | 0.02 Ω |
| Grid Inductance | 0.3mH |
| Filter Inductance | 2.1mH |
| DG Controller Parameters | |
| Q Control | $K_p = 0.1, K_i = 0.01$ |
| $V_{dc}$ Control | $K_p = 0.15, K_i = 9.78$ |
| PI Control | $K_p = 1, K_i = 1250$ |
| Load Parameters | |
| R | 2.304 Ω |
| L | 0.00345 H |
| C | 2037 µF |

In this section,the test system presented in Figure 1 which is simulated in MATLAB/Simulink. The system, DG, and load parameters are listed in Table 2. The parameter $Q_{ref}$ has been set to 0 MVAr. The Islanding detection method has been tested for load with a quality factor ($Q_f$) of 1.77. The proposed islanding detection method has been also tested for various loading conditions specified in the UL 1741 Standard [3].

### 4.1. UL 1741 Testing

Based on the UL 1741 Standard, the active load power is adjusted to set the inverter at 25%, 50%, 100%,and 125% of the rated output power of the inverter. The reactive power has been adjusted between 95% and 105% of the balanced condition (unity power factor loading) in 1% steps [3]. The islanding detection scheme is tested based on the procedure presented in [3]. The DG interface has been equipped with the $V_{(dc-ref)}$ characteristic given in (31) and islanding has occurred at t =0.8s.

The first simulation result using the proposed method is shown in Figure 9. This figure shows the voltage at the PCC during an islanding condition, for the active load power adjusted at 50%, 100%, and 125% of its rated output power. The reactive power has been adjusted at 100% of the balanced condition. As can be seen in Figure 9, the PCC voltage exceeds the OVP/UVP thresholds in less than 100ms (after the occurrence of islanding).
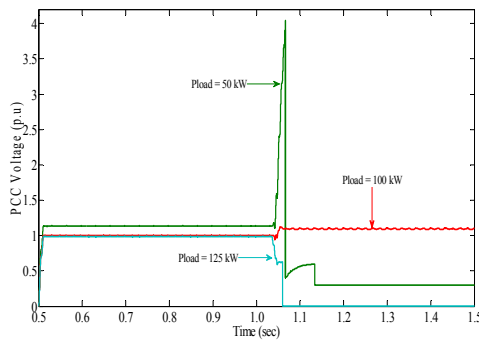


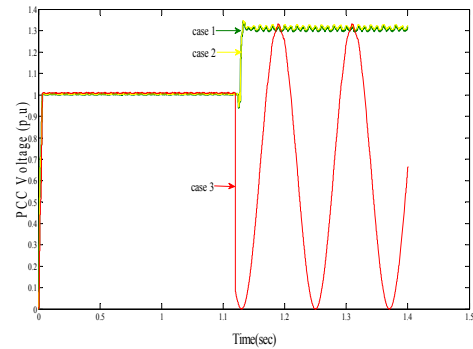Figire 9. PCC voltage using the proposed $V_{dc-ref}$ characteristic for different loads



Figure 10. PCC voltagewith $V_{dc-ref}$ characteristic for three cases

Figure 10 shows the voltage at the PCC during an islanding condition, for the following cases [4]:

Case 1) The load has been adjusted at 100% of rated active power with 101% reactive power in the balanced condition.

Case 2) The load has been adjusted at 100% of the rated active power with 100% reactive power.

Case 3) The load has been adjusted at 100% of its rated active power with 99% reactive power.

Table 3. Load Parameters For UL 1741 TESTS

| P% | Q% | R(Ω) | L(H) | C(μF) |
|---|---|---|---|---|
| 50 | 100 | 4.603 | 0.00345 | 2037 |
| 125 | 100 | 1.841 | 0.00345 | 2037 |
| 100 | 99 | 2.304 | 0.003488 | 2037 |
| 100 | 100 | 2.304 | 0.00345 | 2037 |
| 100 | 101 | 2.304 | 0.003419 | 2037 |

### 4.2. Effect of Load Switching

The proposed islanding detection method has been tested for load switching in the grid-connected operation mode. In parallel with the old load, which has been presented in Figure 1, the new load has been switched at t= 0.5 s and disconnected at t= 1s. Three cases have been simulated in this test. In all cases, the load apparent power is equal to 100 kVA but the power factor is 0.8 lead, 1.0 and 0.8 lag. The simulation results that include the PCC voltage, and the DG active and reactive power outputs for three different loading conditions have been presented in Figure 11. The voltage variation can be seen when the load is switched on and off. For simulated cases, the voltage and frequency variations are within the standard values. It is obvious that the proposed method does not interfere with the power system operation during normal conditions.
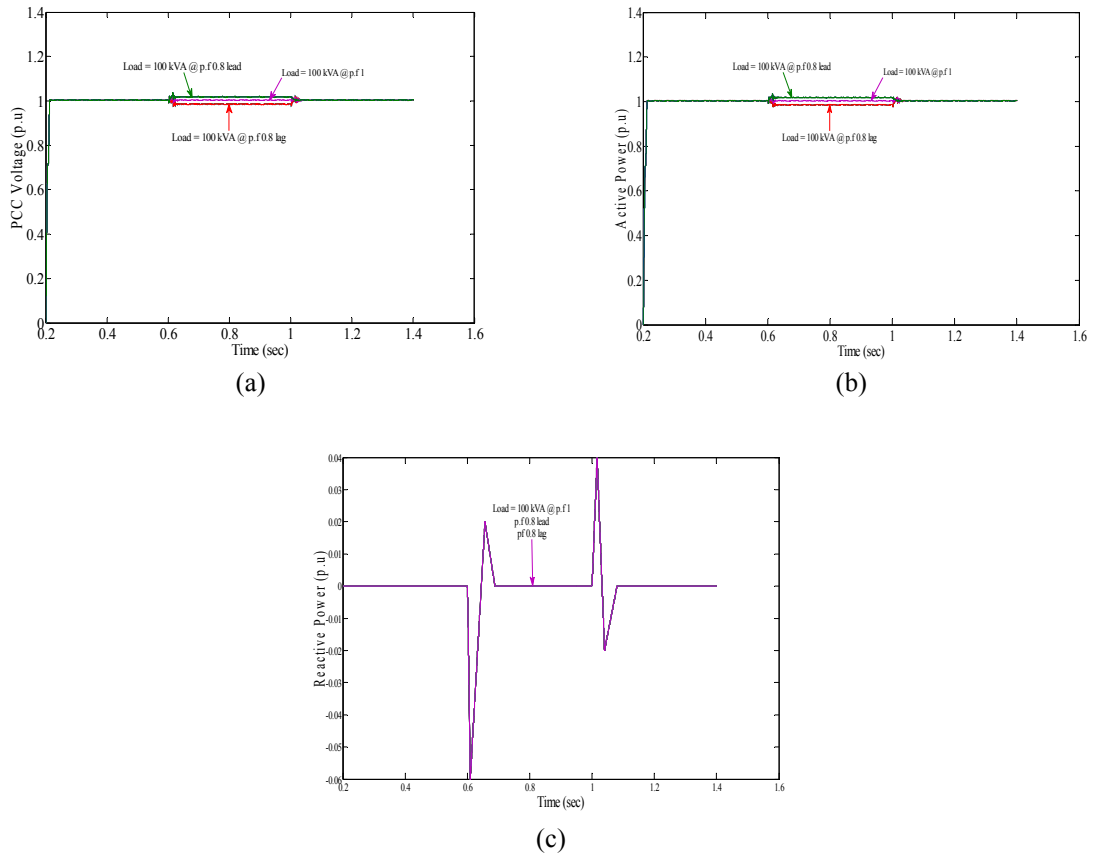
(a)

(b)

(c)

Figure 11. System response during load switching. (a) PCC voltage. (b) Inverter active power. (c) Inverter reactive power

## 4.3. Multiple-DG Operation Mode

The proposed islanding detection method has been tested in a system with multiple DGs. For the simplification and demonstration of the interactions, two DG units are used in this study. Figure 13 illustrates the operation of two DGs grid-connected inverters. Each DG is the same as the single DG system case and the rating of each of them is equal to 100 kW. They are connected to the PCC in parallel to supply the load with 200-kW active power. Every DG interface has been equipped with the $V_{dc\text{-}Vpcc}$ characteristic presented in (31). Islanding has been simulated at t= 0.8 s. The simulation result has been presented in Figure 14. It can be seen that DG loses its stable operation mode, and an islanding condition can be detected by using OVP/UVP methods in less than 50ms.
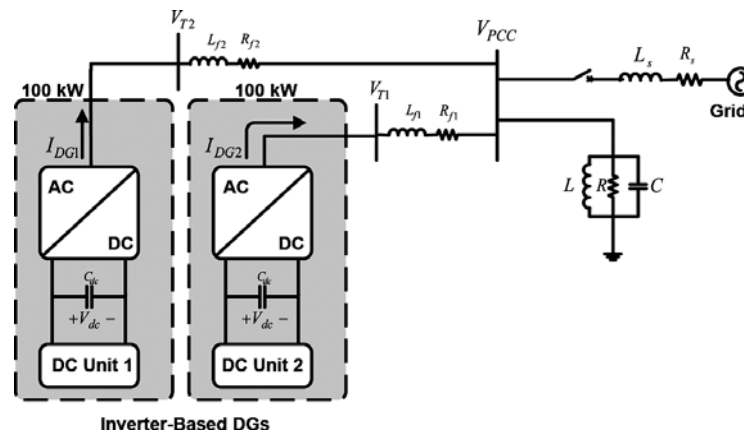


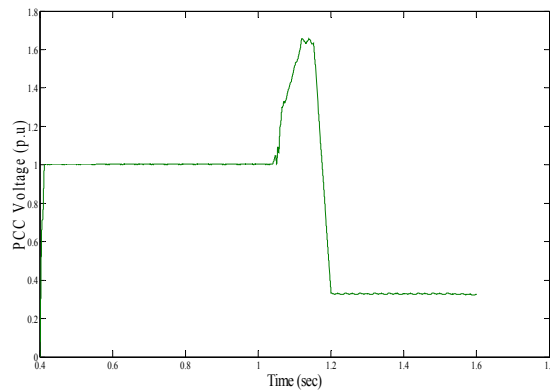Figure 13. Schematic diagram of the two-DG system

Figure 14. PCC voltage for the multiple-DG operation mode

### 4.4. Using PV System

The proposed islanding detection method has been operated using a PV system. The simulation result has been presented in Figure 15.
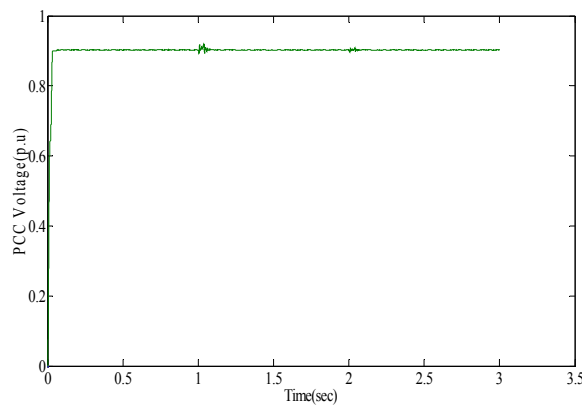


Figure 15. PCC voltage for the multiple-DG operation mode using PV system

### 5. CONCLUSION

This paper proposes a new method for islanding detection of an inverter-based DG unit by using the $V_{dc}$-$V_{pcc}$ characteristic. The $V_{dc}$-$V_{pcc}$ characteristic has been chosen so that the DG maintains its stable operation in grid-connected and islanding condition modes. Applying the proposed $V_{dc}$-$V_{pcc}$ characteristic to the DG results in a simple islanding detection method, which can be similar to OVP/UVP protections? The suggested method has been studied for the inverter-based DG unit under the multiple-DG operation mode and the UL 1741 test conditions conditions and also using a PV system. These simulation results show the effectiveness of the new islanding detection method for different operating conditions and also it has been shown that this method does not distort any voltage or current waveforms by injecting perturbations. Thus, it has high performance from a PQ point of view and also capable of detecting islanding conditions accurately within the minimum standard time.

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