

## A Novel Direct Torque Control for Induction Machine Drive System with Low Torque and Flux Ripples using XSG

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### ABSTRACT

The conventional Direct Torque Control (DTC) is known to produce a quick and robust response in AC drives. However, during steady state, stator flux and electromagnetic torque which results in incorrect speed estimations and acoustical noise. A modified Direct Torque Control (DTC) by using Space Vector Modulation (DTC-SVM) for induction machine is proposed in this paper. Using this control strategy, the ripples introduced in torque and flux are reduced. This paper presents a novel approach to design and implementation of a high performance torque control (DTC-SVM) of induction machine using Field Programmable gate array (FPGA). The performance of the proposed control scheme is evaluated through digital simulation using Matlab/Simulink and Xilinx System Generator. The simulation results are used to verify the effectiveness of the proposed control strategy.

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## 1. INTRODUCTION

Since its inception, the Direct Torque Control has gained popularity for induction machine drives. Indeed, the control variables that are the stator flux and torque are calculated from the quantities related to the stator without the intervention of mechanical sensor. The response of the DTC is fast, however it has some drawbacks such as notable torque and flux ripples and the variable commutation frequency behavior of the inverter. Many papers presented different approaches to minimize the flux and torque ripples [1]-[4]. In [1] and [3], electromagnetic torque and flux are controlled directly by the selection of a switching vector from a table selection. Nevertheless, the selected vector is not always the best one because only the sector is considered, where the flux space vector lies without considering its location.

To overcome the several disadvantages of DTC a new control technique called Direct Torque Control – Space Vector Modulated (DTC-SVM) [5]-[6] is developed. In this new method, the disadvantages of the DTC are eliminated. The DTC-SVM strategies are based on the same fundamentals as classical DTC; it provides dynamic behavior comparable with classical DTC.

In practice, the vector control algorithm for an induction machine is implemented utilizing digital signal processor (DSP). The DSP control procedure is performed sequentially; this may result in a slower cycling period if complex algorithms are involved. Employing field programmable gate array (FPGA) in implementing vector control strategies provides advantages such as simpler hardware and software design, rapid prototyping, hence fast switching frequency and high speed computation [7]-[8].

The paper devotes to a comparative study between the performances of two approaches: (i) Classical DTC (ii) DTC-SVM. These strategies are designed using Xilinx System Generator (XSG) and Matlab/Simulink software packages and implemented on FPGA controller.

## 2. BASIC PRINCIPLE OF DTC

The main idea of DTC is to recover the reduction of the ripples of torque and flux, and to have superior dynamic performances. Figure 1 present a possible schematic of Direct Torque Control. There are two different loops corresponding to the magnitudes of the stator flux and torque. The error between the estimated stator flux magnitude  $\varphi_s$  and the reference stator flux magnitude  $\varphi_s^*$  is the input of a two level hysteresis comparator whereas the error between the estimated torque  $T_e$  and the reference torque  $T_e^*$  is the input of a three level hysteresis comparator. The outputs of the stator flux error and torque error hysteresis blocks, together with the position of the stator flux are used as inputs of the switching table.

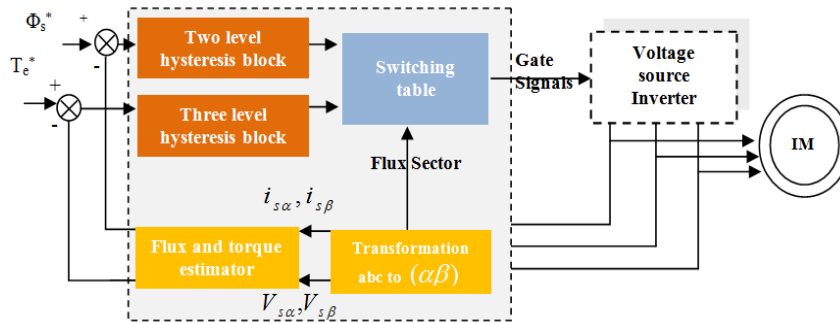


Figure 1. Block diagram of DTC

The selection vector is based on the hysteresis control of the torque and the stator flux. In the basic form the stator flux  $\varphi_s$  is estimated with:

$$\varphi_s = \int_0^t (V_s - R i_s) dt \quad (1)$$

The stator voltage and stator current are calculated from the state of three phase ( $S_a, S_b, S_c$ ) and measured currents ( $i_a, i_b, i_c$ ).

$$V_s(S_a, S_b, S_c) = \sqrt{\frac{2}{3}} E_0 (S_a + S_b e^{j\frac{2\pi}{3}} + S_c e^{j\frac{4\pi}{3}}) \quad (2)$$

$$i_s(i_a, i_b, i_c) = \frac{2}{3} (i_a + i_b e^{j\frac{2\pi}{3}} + i_c e^{j\frac{4\pi}{3}})$$

Phase angle and stator flux amplitude are calculated in expression (3).

$$\theta_s = \arctg\left(\frac{\varphi_{s\beta}}{\varphi_{s\alpha}}\right)$$

$$\varphi_s = \sqrt{\varphi_{s\alpha}^2 + \varphi_{s\beta}^2} \quad (3)$$

The developed electromagnetic torque  $T_e$  of the machine can be evaluated by Equation (4):

$$T_e = \frac{3}{2} p (i_{s\beta} \phi_{s\alpha} - i_{s\alpha} \phi_{s\beta}) \quad (4)$$

The stator flux vector is moving along a straight axis colinear to that of the voltage vector required by the inverter:

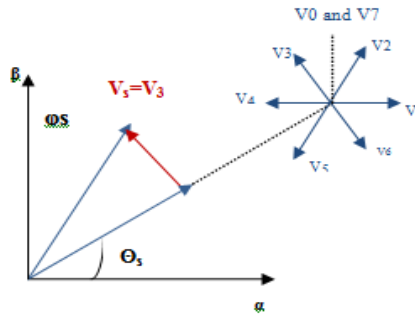


Figure 2. Stator flux vector evolution in the first sector

**3. DTC SPACE VECTOR MODULATION**

The DTC algorithm is based on the instantaneous values and directly calculated the gate signals for the inverter. The control algorithm in DTC-SVM is based on average values whereas the switching signals (Sa, Sb and Sc) for the inverter are calculated by space vector modulator [9]-[11].

**3.1. Principle of Vector MLI**

For each period of modulation of the inverter, the three phase voltages provided by the control algorithm can be expressed in a fixed reference linked to the stator, through their projections  $V_{s\alpha}$  and  $V_{s\beta}$ .

The inverter has six switching cells, giving eight possible switching configurations. These eight switching configurations can be expressed in the plane  $(\alpha, \beta)$  by 8 vectors tensions.

Knowing that in the graduation phase voltages ( $V_a, V_b, V_c$ ) are represented in the plane by a vector  $V_s$ . The principle of vector MLI is to project the desired stator voltage vector  $V_s$  on the two adjacent vectors corresponding to two switching states of the inverter. The values of these projections provide the desired commutation times.

**3.2. General Structure of the Control DTC-SVM**

Most existing blocks in the control DTC-SVM are identical to those of control DTC as shown in the following figure (3). The new blocks will be discussed below.

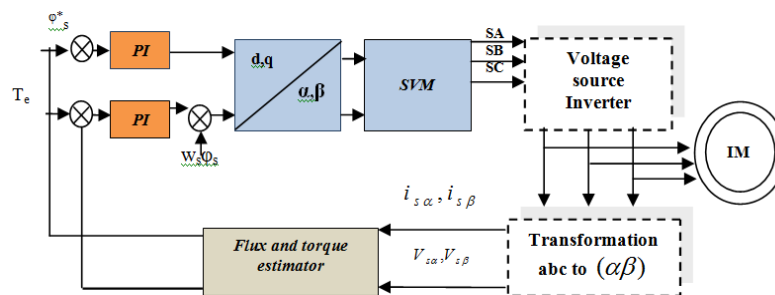


Figure 3. Block diagram of DTC-SVM

**3.3. Calculation of time of application of the status of the inverter**

Each modulation period  $T_{mod}$  of the inverter, the projected vector  $V_s$  on the two adjacent vectors assures the switching time of calculation.

The key step of the SVM technique is the determination of  $T_i$  and  $T_{i+1}$  during every modulation period  $T_{mod}$ . To illustrate the methodology we consider the case where  $V_s$  can be compounded by the active voltage vectors  $V_1$  and  $V_2$ . The projection of the reference voltage vector on  $V_1$  and  $V_2$  is illustrated in the following figure:

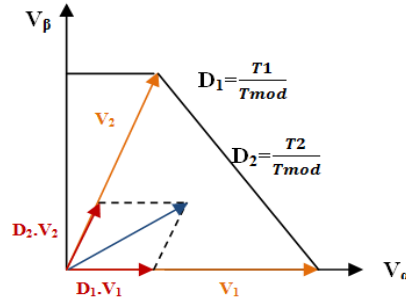


Figure 4. Projection of the reference voltage vector on  $V_1$  and  $V_2$

The active voltage vectors  $V_1$  and  $V_2$  are given as follow:

$$\begin{cases} \bar{V}_1 = \sqrt{\frac{2}{3}} \cdot E \cdot e^{j0} \\ \bar{V}_2 = \sqrt{\frac{2}{3}} \cdot E \cdot e^{j\frac{\pi}{3}} \end{cases} \quad (5)$$

Expressing the voltage vector  $V_s$  in the graduation  $(\alpha, \beta)$  we have:

$$\bar{V}_s = V_{s\alpha} + jV_{s\beta} = \frac{T_1}{T_{\text{mod}}} \bar{V}_1 + \frac{T_2}{T_{\text{mod}}} \bar{V}_2 \quad (6)$$

Expanding this equation it is possible to express the time  $T_1$  and  $T_2$  in terms of  $V_{s\alpha}$  and  $V_{s\beta}$ . The conduction time will be expressed as follows:

$$\begin{cases} T_1 = (\sqrt{\frac{3}{2}} V_{s\alpha} - \sqrt{\frac{1}{2}} V_{s\beta}) \cdot \frac{T_{\text{mod}}}{E} \\ T_2 = \sqrt{2} V_{s\beta} \cdot \frac{T_{\text{mod}}}{E} \end{cases} \quad (7)$$

To facilitate the calculations, we normalize the voltages  $V_{s\alpha}$  and  $V_{s\beta}$  by posing:

$$\begin{cases} \hat{V}_{s\alpha} = \frac{V_{s\alpha}}{E} \sqrt{2} \\ \hat{V}_{s\beta} = \frac{V_{s\beta}}{E} \sqrt{2} \end{cases} \quad (8)$$

Consequently, the duties expressions are given as follows:

$$\begin{aligned} D_1 &= \frac{\sqrt{3}}{2} \cdot \hat{V}_{s\alpha} - \frac{1}{2} \cdot \hat{V}_{s\beta} \\ D_2 &= \hat{V}_{s\beta} \\ D_0 &= 1 - D_1 - D_2 \end{aligned} \quad (9)$$

The space vector in sector 1 is shown in figure (5). The time duration of zero vectors is divided equally into  $(V_0, V_1, V_2, V_7, V_2, V_1, V_0)$ , whereas the time duration of each nonzero vector is distributed into two parts. This sequence can ensure that is one phase switches when the switching pattern switches, thus can reduce the harmonic component of the output current and the loss of switching devices.

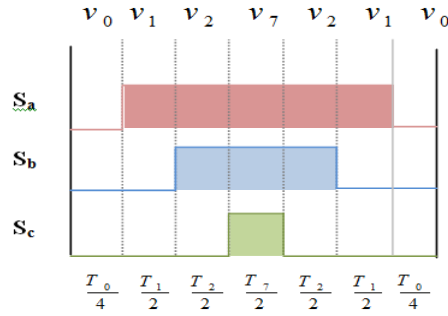


Figure 5. Sequences of the switches states in sector N1

The duties of each phase of the inverter are presented as follows:

$$\begin{aligned}
 S_a &= 0.5(1 + D_1 + D_2) \\
 S_b &= 0.5(1 - D_1 + D_2) \\
 S_c &= 0.5(1 - D_1 - D_2)
 \end{aligned}
 \tag{10}$$

**4. SIMULATION AND RESULT**

The DTC and DTC-SVM scheme for induction machine are simulated using Matlab/Simulink and Xilinx System Generator and their results have been compared. The machine parameters used for simulation are given in this table.

Table 1. Induction Machine parameters

Voltage	220/380 v
Stator resistance $R_s$	5.717 $\Omega$
Rotor resistance $R_r$	4.282 $\Omega$
Stator inductance $L_s$	0.464 H
Rotor inductance $L_r$	0.464 H
Mutual inductance M	0.441 H
Moment of inertia J	0.0049 Kg.m <sup>2</sup>

**4.1. Simulink Model of Direct Torque Control**

The simulation of DTC was conducted using Simulink\MATLAB. The inverter switching pulses are obtained from the switching table which decides the pulses from the error signals of torque and flux. The overall DTC model is shown in Figure 6.

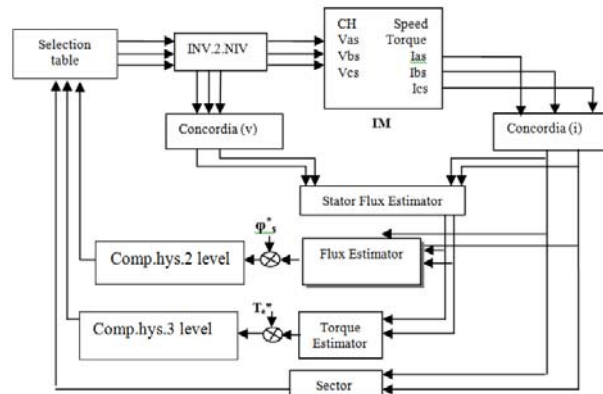


Figure 6. Simulink Model of DTC

**4.2. Simulink Model of Space Vector Modulated Direct Torque Control obtained with Matlab/Simulink**

Figure 7 illustrate the simulation block of the DTC-SVM control. The system is composed of the machine, PI controllers, three phase voltage source inverter, reference frame transformation blocks Concordia and Park. The Insulated-gate bipolar transistor IGBT switches are controlled using space vector modulation technique.

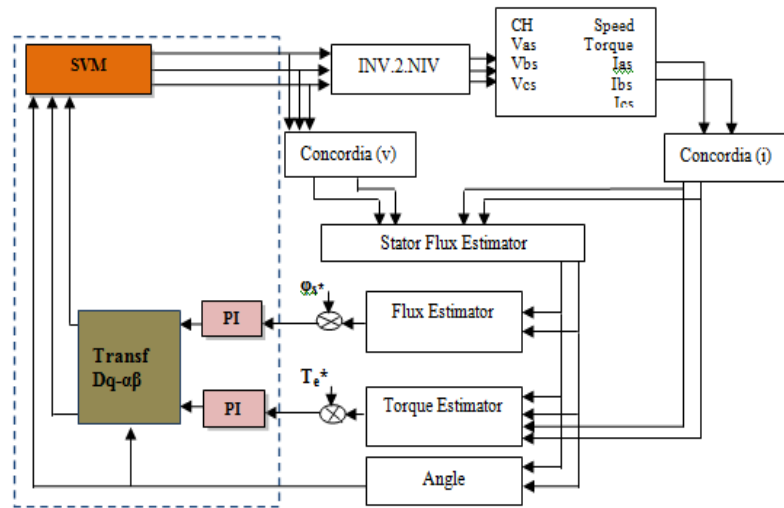


Figure 7. Simulink Model of DTC-SVM

The simulation of this technique is made through the following model:

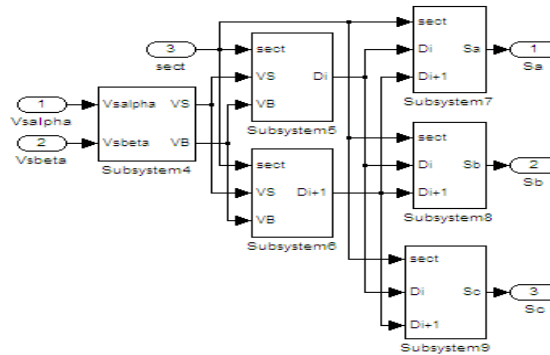


Figure 8. Simulink Model of bloc SVM

**4.3. Simulink Model of Space Vector Modulated Direct Torque Control obtained with Xilinx System Generator**

Initially, an algorithm is designed and simulated at the system level with the floating-point Simulink blocksets. A hardware representation of FPGA implementation is then derived using XSG. The XSG provides a bit-accurate model of FPGA circuits and automatically generates a synthesizable VHDL code for implementation in Xilinx FPGA. For DTC-SVM modeling, the blocks used are mostly multipliers, adders, Cordic sin cos, etc. The detailed steps are shown in the following diagram in Figure 9. The XSG design of proposed DTC-SVM is shown in Figure 10. The block Calcul\_Vsalph\_Vsbeta is used to project the three-phase voltages in the repository ( $\alpha, \beta$ ) by performing the processing Clarke as shown in Figure 10(a). The block SVM generates a series of pulses to be used subsequently to carry out the control signals used in the model of the inverter as shown in Figure 10(b) and 10(c). The XSG design of torque and flux estimator is shown in Figure 11-12.

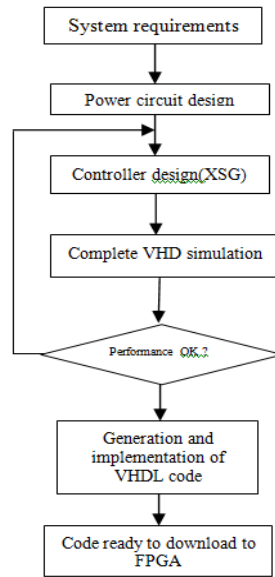


Figure 9. Induction machine drive controller design and implementation process

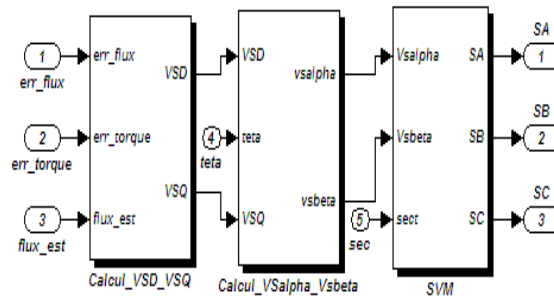


Figure 10. Xilinx Model of SVM

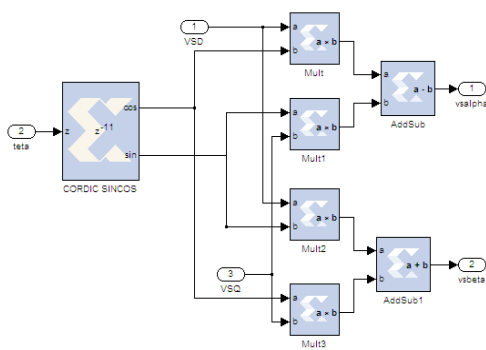


Figure 10(a). Calcul VsalpHa Vsbeta

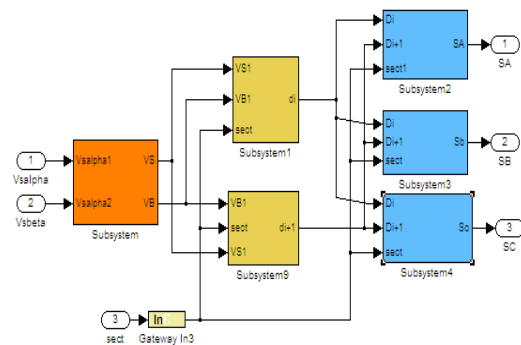


Figure 10(b). VM bloc in XSG

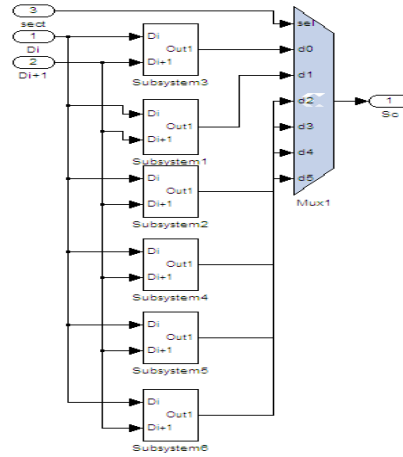


Figure 10(c). Calcul Sc

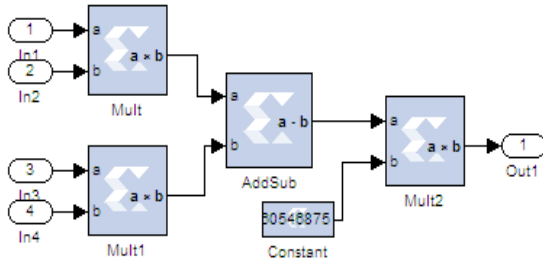


Figure 11. Model of electromagnetic torque

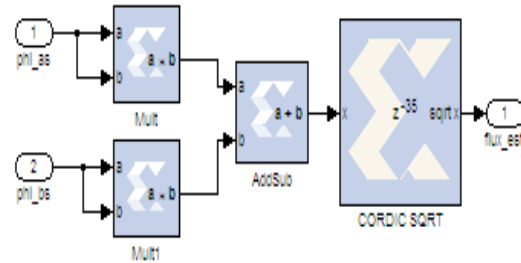


Figure 12. Model of flux estimator

**4.4. SIMULATION RESULTS**

The performance of the induction machine under different operating conditions was also investigated in order to verify the robustness of the proposed control scheme. The steady state behavior of induction machine with the conventional DTC and DTC-SVM are illustrated in Figure 13-15.

It is possible to see in Figure 13(a), (b), (c) an appreciable reduction of electromagnetic torque ripple has been obtained using the DTC-SVM. For the DTC, torque variation of the hysteresis band equal to 1.1. The high ripple observed in the DTC is reduced when we use the DTC-SVM, because in SVM, many vectors (IGBT states) are selected to adjust the flux and torque ripple in each sample time, whereas in DTC just one vector is selected to adjust ripple inside hysteresis bands of flux. Using SVM control provides the system with minimum ripple for flux as shown in Figure 14, where the flux ripple percentage is about 0.92%.

The DTC-SVM of induction machine presents the advanced performance to achieve tracking of the desired smooth circular trajectory of stator flux locus shown in Figure 15.

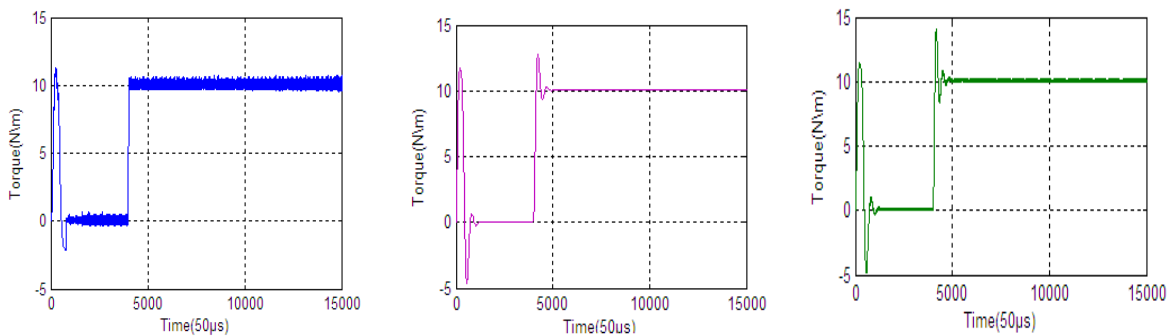


Figure 13. Electromagnetic torque, (a): DTC using MATLAB, (b) DTC-SVM using MATLAB, (c): DTC-SVM using XSG



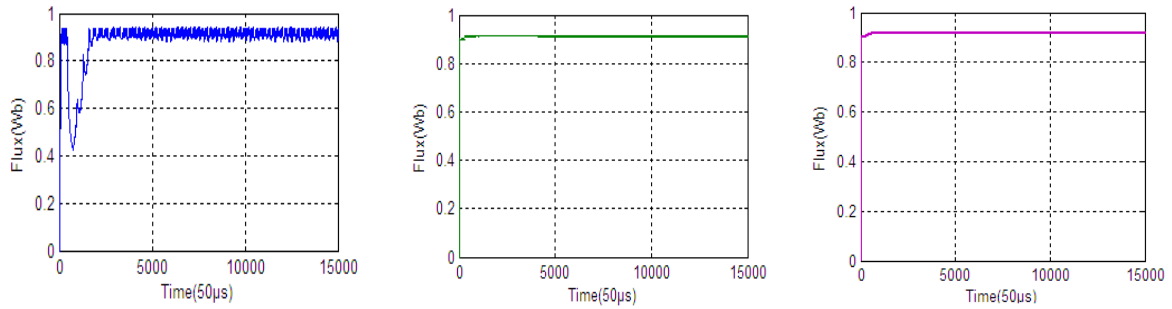


Figure 134. Stator flux DTC using MATLAB, (b): DTC-SVM using MATLAB, (c): DTC-SVM using XSG

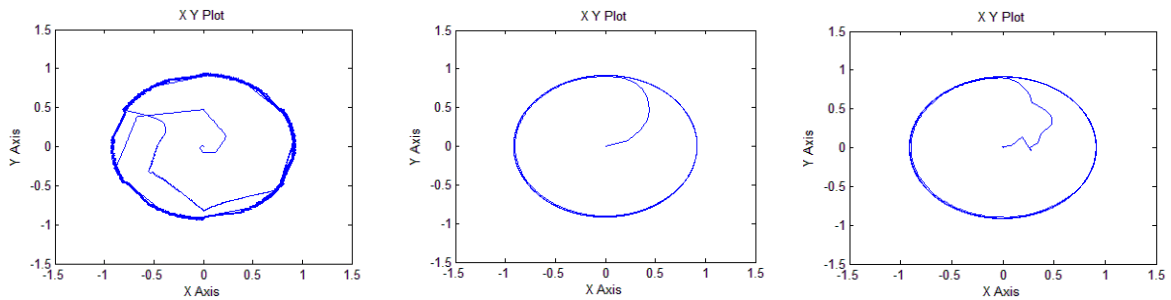


Figure 15. Trajectory of stator flux: DTC using MATLAB, (b): DTC-SVM using MATLAB, (c): DTC-SVM using XSG

Table 2. The percentage flux and torque error for DTC and DTC-SVM

Control strategies	Flux ripple (%)	Torque ripple (%)
DTC using Matlab	5.52	11
DTC-SVM using Matlab	0.92	1
DTC-SVM using XSG	1.84	2

The best results are given by DTC-SVM using MATLAB\SIMULINK, this is due to the arbitrary choice of the number of bits at XSG.

## 5. FPGA SIMULATION RESULTS OF DTC-SVM

The above designed model is implemented using FPGA Editor. FPGA Editor reads the NCD file generated by the Map or Place & Route process, which contains the logic and routing of the design mapped to components, such as CLBs and IOBs. The internal structure of FPGA is shown in Figure 16.

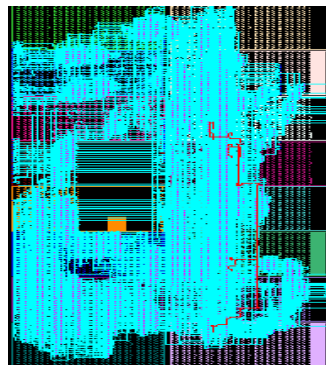


Figure 146. Internal structure of FPGA

The result of the resources used is shown in the following table:

Table 3. The result of the resources

Slice logic utilization	Used	Available	Utilization
Number of slices LUTs	10,511	44,800	23%
Number used as Logic	9,869	44,800	22%
Number of DSP48Es	109	128	85%
Number of slice registers	655	44,800	1%

## 6. CONCLUSION

This paper has been devoted to the comparison between the performances of the DTC and DTC-SVM strategy. The steady state features of the induction machine as well as the transient behavior under both approaches have been commented and compared. The simulation result clearly indicates the high performance of DTC-SVM. The proposed high performance scheme is designed using XSG and Matlab/Simulink blocksets and implemented on Xilinx Virtex 5 FPGA. Numerical simulations have been carried out showing the advantages of the DTC-SVM with respect to the DTC. This work is the first step towards implementation on FPGA of DTC-SVM. Future work will extend this experimental validation to the study.

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