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Design of New Single-phase Multilevel Voltage Source Inverter

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ABSTRACT

Multilevel inverters with more number of levels can produce high quality voltage waveforms. In this paper, a new single-phase structure for multilevel voltage source inverter is proposed which can generate a large number of levels with reduced number of IGBTs, gate driver circuits and diodes. Three algorithms for determination of dc voltage sources' magnitudes are presented which provide odd and even levels at the output voltage waveform. A comparison is presented between proposed multilevel inverter and conventional cascade topology. The proposed topology is analyzed by the experimental and simulation results.

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1. INTRODUCTION

Multilevel inverters are power electronic systems which produce a suitable AC output voltage waveform from several dc voltages as inputs [1]. In recent years, Multilevel inverters have been utilized in medium and high power applications such as flexible AC transmission system (FACTS) [2], industrial motor drives [3], traction electric vehicle applications, drive systems [4], [5] and so on.

Multilevel inverters in comparison with the traditional two-level voltage inverter have advantages such as smaller output voltage level, better electromagnetic compatibility, lower harmonic components and lower switching losses [6], [7]. There are three renowned kinds of multilevel inverter which have been called classical multilevel inverter topologies. These are Neutral-Point Clamped (NPC), Flying capacitor (FC) and Conventional cascade H-bridge inverter (CHB) [8]-[10].

Conventional cascade topology is the most important topology among classical topologies. Because this topology needs the least number of power electronic devices and can produce many levels at output voltage [11], [12]. A cascade multilevel inverter consists of a number of H-bridge converter units with separate dc source for each unit and it is connected in cascade or series [13]. In symmetric cascade multilevel inverter, DC voltage sources of similar cells are the same. For the same number of power electronic components, asymmetric cascade multilevel topologies significantly increase the number of level at output voltage waveforms. In these topologies, DC voltage sources of different cells are non-equal [14], [15]. However, this structure requires to a large number of unidirectional switches. The most important Part in multilevel inverters is switches which increase the cost and control complexity and tend to reduce the overall reliability and efficiency [16], [17].

In this paper, a new structure for multilevel voltage source inverter is presented which can generate

many levels with minimum number of IGBTs, gate driver circuits and diodes.

2. THE STRUCTURE OF CONVENTIONAL CASCADE MULTILEVEL INVERTER

The structure of conventional cascade multilevel inverter is shown in Figure 1. The output voltage of cascade inverter is obtained by summing the output voltages of full-bridges and is obtained by the following relationship:

$$V_o = V_{o1} + V_{o2} \dots + V_{on} \quad (1)$$

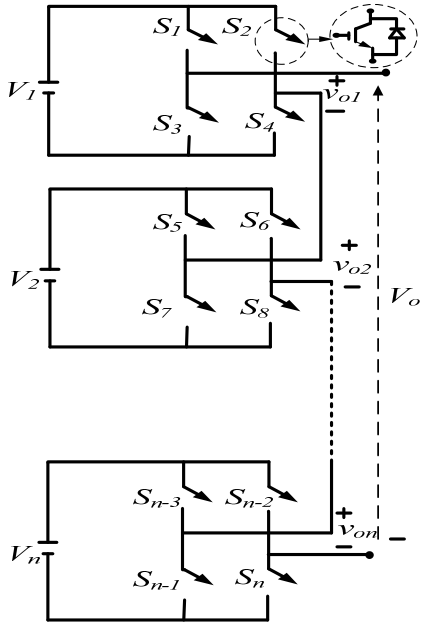

Figure 1. The structure of conventional cascade multilevel inverter

In this structure, each switch consists of an IGBT and one diode (or anti-parallel diode). If all dc voltage sources in Figure 1 are the same, the inverter is known as symmetric multilevel inverter. To provide a large number of output levels without increasing the number of power electronic elements, asymmetric multilevel inverters can be used. In [16], [17], the dc voltages sources are proposed to be chosen according to a geometric progression with a factor of two or three, which are called binary and trinary configurations. In symmetric, binary and trinary configurations, the magnitudes of dc voltage sources are selected by the following equations:

For symmetric configuration:

$$V_1 = V_2 = \cdots = V_n = V \quad (2)$$

For *m*th full-bridge converter in binary configuration:

$$V_m = (2^{m-1}) \times V \qquad m = 1,2, \dots, n \quad (3)$$

For *m*th full-bridge converter in trinary configuration:

$$V_m = (3^{m-1}) \times V \qquad m = 1,2, \dots, n \quad (4)$$

Where V represents the magnitude of voltage of the first full-bridge converter. Table 1 shows the number of IGBTs, levels, maximum output voltage and the relation between the number of IGBTs and levels in symmetric and asymmetric configurations.

Table 1. Power component requirments in conventional cascade inverter

	Symmetric Structure	Asymmetric Structure	
		Binary configuration	Trinary configuration
Number of IGBTs	4n	4n	4n
Voltage levels	2n+1	(2^{n+1}) -1	3^n
maximum output voltage	n×V	$(2^n - 1) \times V$	$\frac{(3^n - 1) \times V}{2}$
Relation between the number of IGBTs and levels	$2(N_{level} - 1)$	$4\left[\frac{\ln(N_{level}+1)}{\ln 2} - 1\right]$	$4\frac{\ln N_{level}}{\ln 3}$

Where n represents the number of dc voltage sources. It is important to note that in all configurations, the numbers of IGBTs, gate driver circuits and diodes (or anti-parallel diodes) are the same.

3. PROPOSED MULTILEVEL INVERTER

Figure 2 shows the basic unit topology for proposed multilevel inverter, which consists of a diode, an IGBT and a dc voltage source. In this circuit, when the Sswitch is turned off, the output voltage will be zero, but when the Sswitch is turned on, the diode is reverse biased and the output voltage will be V. Hence, by the use of this method the output voltage is controlled. This method is the basic of proposed multilevel inverter.

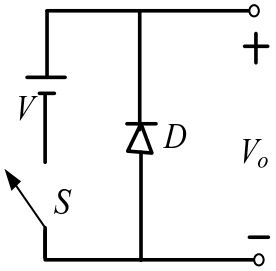

Figure 2. The basic unit of proposed multilevel inverter

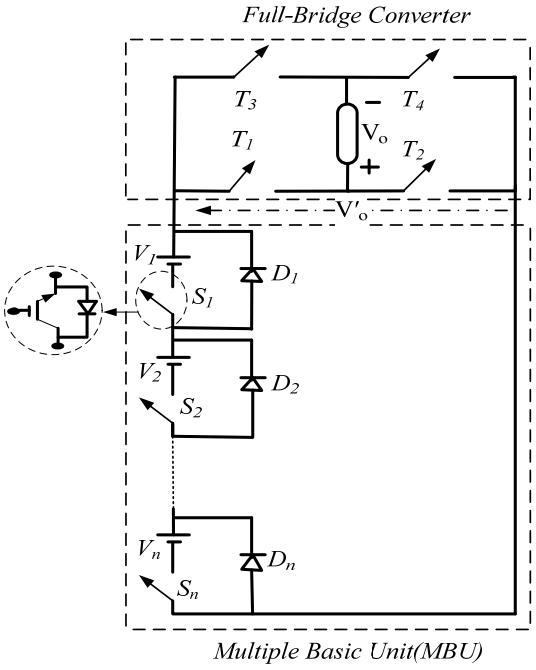

Figure 3. Proposed single-phase multilevel voltage source inverter topology

The proposed basic unit shown in Figure 2 can be extended as shown in Figure 3, which is called Multiple Basic Unit (MBU). The MBU can increase the possible values of V'_o. The MBU generates a staircase voltage waveform (V'_o) with positive polarity $(0, V_1, V_2, V_3, \dots, V_n)$.The MBU is connected to a full-bridge converter, which particularly alternates the input voltage polarity and generates positive or negative staircase waveform (V_o) at the output $(0, \pm V_1, \pm V_2, \dots, \pm V_n)$. The proposed single-phase multilevel voltage

source inverter topology, which is based on the combination of MBU and a full-bridge converter, is shown in Figure 3.

Table 2 Shows the ON switches look-up table for proposed single-phase multilevel inverter topology.

Table 2. Magnitudes of (V'_o) and (V_o)for different states of switches in proposed structurs

state	Switches states									V′o	Output voltage(V_o)
	S_1	S_2	….	S_{n-1}	S_n	T_1	T_2	T_3	T_4		
1	0	0	…….	0	0	1	0	1	0	0	0
2	1	0	….	0	0	1	0	0	1	V_1	V_1
3	1	0	….	0	0	0	1	1	0	V_1	$-V_1$
4	0	1	….	0	0	1	0	0	1	V_2	V_2
5	0	1	….	0	0	0	1	1	0	V_2	$-V_2$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
2n	0	0	….	1	1	1	0	0	1	V_n	V_n
2n+1	0	0	….	1	1	0	1	1	0	V_n	$-V_n$
2n+2	1	1	…..	0	0	1	0	0	1	(V_1+V_2)	(V_1+V_2)
2n+3	1	1	….	0	0	0	1	1	0	(V_1+V_2)	$-(V_1+V_2)$
⋮	⋮	⋮	….	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
$2^{(n+1)}$-2	1	1	….	1	1	1	0	0	1	$(V_1+V_2+\ldots+V_n)$	$(V_1+V_2+\ldots+V_n)$
$2^{(n+1)}$-1	1	1	….	1	1	0	1	1	0	$(V_1+V_2+\ldots+V_n)$	$-(V_1+V_2+\ldots+V_n)$

In the proposed inverter, the number of IGBTs can be determined by (5):

$$\boldsymbol{N_{IGBTs} = n + 4} \quad (5)$$

In the proposed structure, the switches are unidirectional. Each unidirectional switch consists of an IGBT and an anti-parallel diode. In the recommended structure,the number of diodes is given by following equation:

$$\boldsymbol{N_{diode} = 2n + 4} \quad (6)$$

4. DETERMINATION OF THE DC VOLTAGE SOURCES MAGNITUDES

In this section, three algorithms for determination of the dc voltage sources magnitudes are proposed.

a) First algorithm:

In this algorithm, the values of dc sources are the same. Hence, we have:

$$V_1 = V_2 = \cdots = V_n = V \quad (7)$$

This structure is called symmetric topology. Using this algorithm, the number of output voltage levels and maximum output voltage are given by (8) and (9), respectively:

$$N_{level} = 2n + 1 \quad (8)$$

$$V_{Omax} = n \times V \quad (9)$$

Using (5) and (8), the relation between the number of IGBTs and levels is obtained as follows:

$$N_{IGBT} = \frac{N_{level}+7}{2} \quad (10)$$

From (6) and (8), the relation between the number of power diodes and output levels is calculated by following equation:

$$N_{diode} = N_{level} + 3 \quad (11)$$

b) Second algorithm:

In this algorithm, the dc source magnitudes are chosen according the following equations:

$$V_1 = V \quad (12)$$

$$V_m = 2V \quad for\ m = 2, 3, 4, \dots, n \quad (13)$$

In the proposed algorithm, the number of levels and maximum output voltage are given as follows:

$$N_{level} = 4n - 1 \quad (14)$$

$$V_{omax} = (2n - 1) \times V \quad (15)$$

Considering (5) and (14), we have:

$$N_{IGBT} = \frac{N_{level}+17}{4} \quad (16)$$

Using (6) and (14), it is obvious that we have:

$$N_{diode} = \frac{N_{level}+9}{2} \quad (17)$$

c) Third algorithm:

In this algorithm, the values of dc sources are proposed to be chosen according to the following equations:

$$V_1 = V \quad (18)$$

$$V_m = 2^{(m-1)}V \quad for\ m = 2, 3, 4, \dots, n \quad (19)$$

For this method, the number of levels and the peak output voltage are calculated using the following relationships, respectively:

$$N_{level} = 2^{(n+1)} - 1 \quad (20)$$

$$V_{omax} = (2^n - 1) \times V \quad (21)$$

The third algorithm for the determination of values of dc sources is in binary fashion, which results in an exponential increase in the number of overall output voltage levels.

In above equations n represents the number of dc voltage sources. From (5) and (20), we have:

$$N_{IGBT} = \frac{ln(N_{level}+1)}{\ln(2)} + 3 \quad (22)$$

Also, considering (6) and (20), it is clear that we have

$$N_{diode} = 2\left[\frac{ln(N_{level}+1)}{\ln(2)}\right] + 2 \quad (23)$$

The second and third algorithms are called asymmetric topologies. The proposed multilevel voltage source inverter could be a suitable power converter candidate in unidirectional power flow applications such as wind turbine with permanent magnet (PM) or Synchronous Generator (SG) and photovoltaic systems application and so on.

5. COMPARISON OF PROPOSED STRUCTURE WITH CONVENTIONAL CASCADE STRUCTURE

Power IGBTs are the most important element in multilevel inverter structures which define the circuit size, reliability, cost, control complexity and installation area. Figure 4 compares the number of IGBTs versus the number of levels for the first recommended structure (or symmetric structure) with symmetric conventional cascade topology. It is obvious that the proposed symmetric topology needs fewer IGBTs to realize N_{level} for output voltage waveform.

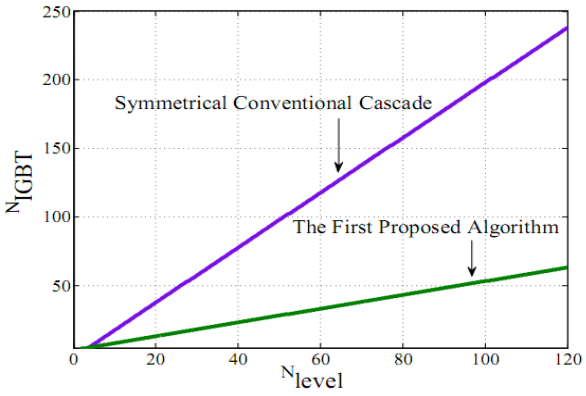

Figure 4. Comparison of N_{IGBTs} for the first recommended structure with symmetric conventional cascade

Figure 5 shows the number of IGBTs versus the number of output levels for the asymmetric recommended structures (the second and third algorithms) with binary and trinary conventional cascade inverter structures. This figure shows the third proposed algorithm requires less number of IGBTs than other structures to realize N_{level} forV_o.

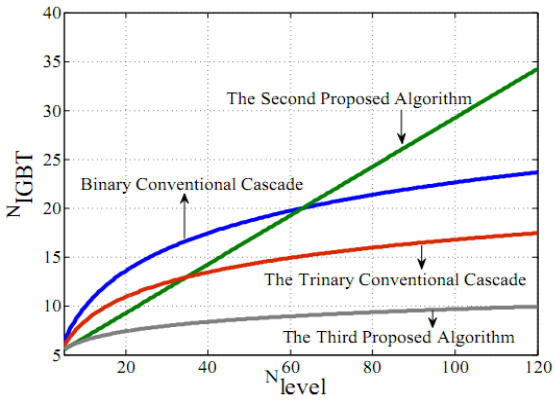

Figure 5. Comparison of N_{IGBTs} for the asymmetrical recommended structures with binary and trinary conventional cascade

It is important to note that in proposed topology, the number of IGBTs and gate driver circuits are the same. Hence, the third suggested topology requires minimum number of gate drivers. The gate driver circuits are the electronic part of the circuit and increasing the number of gate driver circuits is a considerable deficiency. Because increasing gate driver cause increasing costs and control complexity.

Figure 6 compares the number of diodes versus the number of levels in the symmetric proposed topology and symmetric conventional cascade inverter. As shown in this figure, the proposed symmetric topology requires fewer numbers of diodes than symmetric cascade topology.

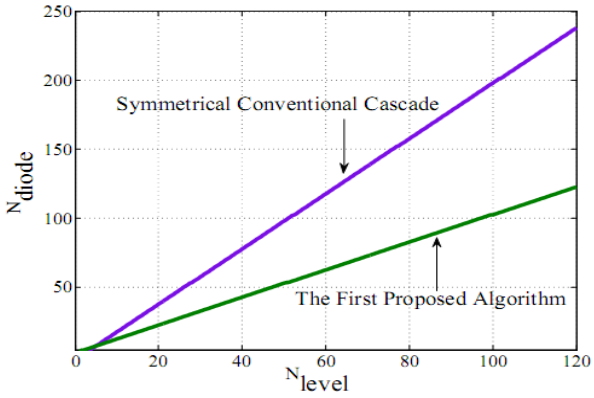

Figure 6. Comparison of N_{diode} to realize N_{level} voltages in the proposed symmetric topology and symmetric conventional cascade

Figure 7 shows the number of diodes versus the number of output voltage levels in the asymmetric proposed topologies and conventional cascade inverter. This figure shows that the number of diodes in thirdalgorithm of proposed topology is lower than other topologies.

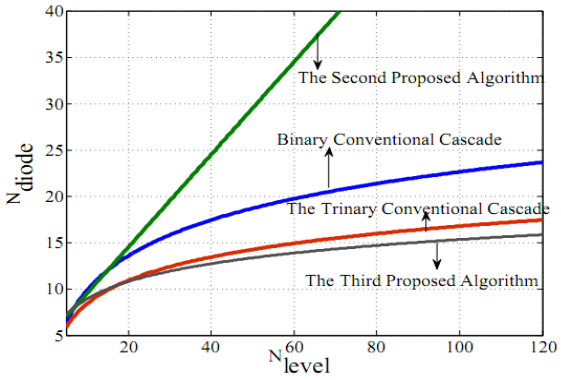

Figure 7. Comparison of N_{diode} to realize N_{level} voltages in the proposed asymmetric topologies and asymmetric conventional cascade

6. EXPERIMENTAL AND SIMULATION RESULTS

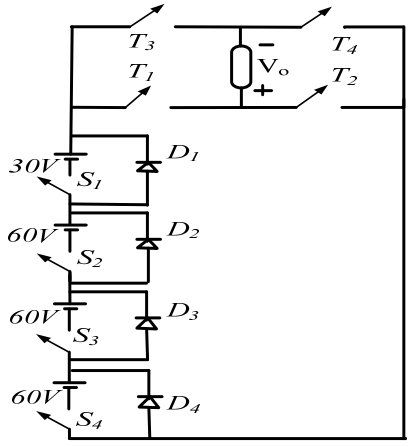

Figure 8. Proposed 15-level asymmetric inverter according to the second algorithm

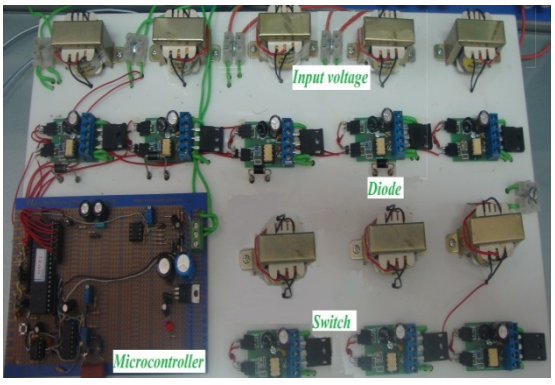

Figure 9. Photo of the archetype

In this section, the simulation and experimental results for the 15-level asymmetric topology (according to the second algorithm) is studied. The MATLAB software is utilized for simulation. Figure 8 shows 15-level asymmetric inverter structure based on the second proposed algorithm. Figure 9 shows photo of the archetype.

The inverter consists of four DC voltage sources with magnitudes of 30V and 60V. A test has been made on the R-L load (R = 140Ω and L = 40mH).The switches are IRFP450 MOSFET's with internal anti-parallel diodes. The gate drivers are TLP250 and diodes are MUR460.

The total harmonic distortion (THD) evaluates the quantity of harmonic contents in the output waveform and is a popular performance index for power converters. Several modulation techniques have been introduced for multilevel inverters such as sinusoidal PWM, space vector PWM, selective harmonic elimination, fundamental frequency-switching and others [18]-[24].

In this paper, the fundamental frequency-switching strategy has been used. The benefit of the fundamental frequency-switching technique is its low switching frequency compared to other control strategies [25]. It is noticeable that the calculation of the optimal switching angles for different objective such as the elimination of selected harmonics and minimizing the total harmonic distortion is not the objective of this paper. Table 3 shows the magnitude of output voltage for various states of switches in suggested 15-level asymmetric structure.

Table 3. Switches states for 15-level asymmetric topology

State	Switches states								V_o
	S_1	S_2	S_3	S_4	T_1	T_2	T_3	T_4	
1	1	1	1	1	1	0	0	1	210V
2	0	1	1	1	1	0	0	1	180V
3	1	0	1	1	1	0	0	1	150V
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
7	1	0	0	0	1	0	0	1	30V
8	0	0	0	0	1	0	1	0	0
9	1	0	0	0	0	1	1	0	-30V
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
13	1	0	1	1	0	1	1	0	-150V
14	0	1	1	1	0	1	1	0	-180V
15	1	1	1	1	0	1	1	0	-210V

Figure 10 shows the control block diagram for proposed topology.

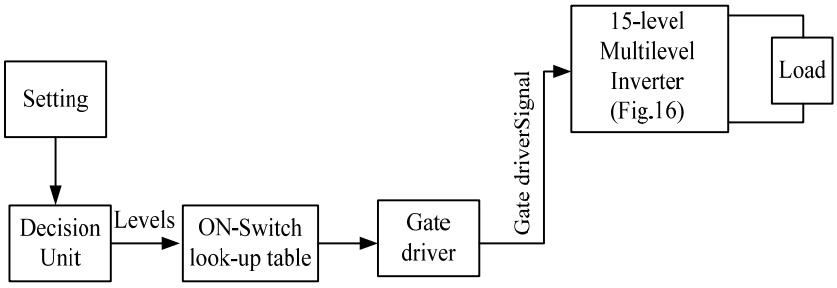

Figure 10. Control block diagram for proposed topology

The simulation and measurement results are shown in Figure 11. According to the simulations, THDs of the output voltage and current are 3.83% and 1.17%, respectively. This figuresshows that the simulationsand experimental results have a good agreement to each other.To generate a desired output with high power quality, the number of voltage levels should be increased.

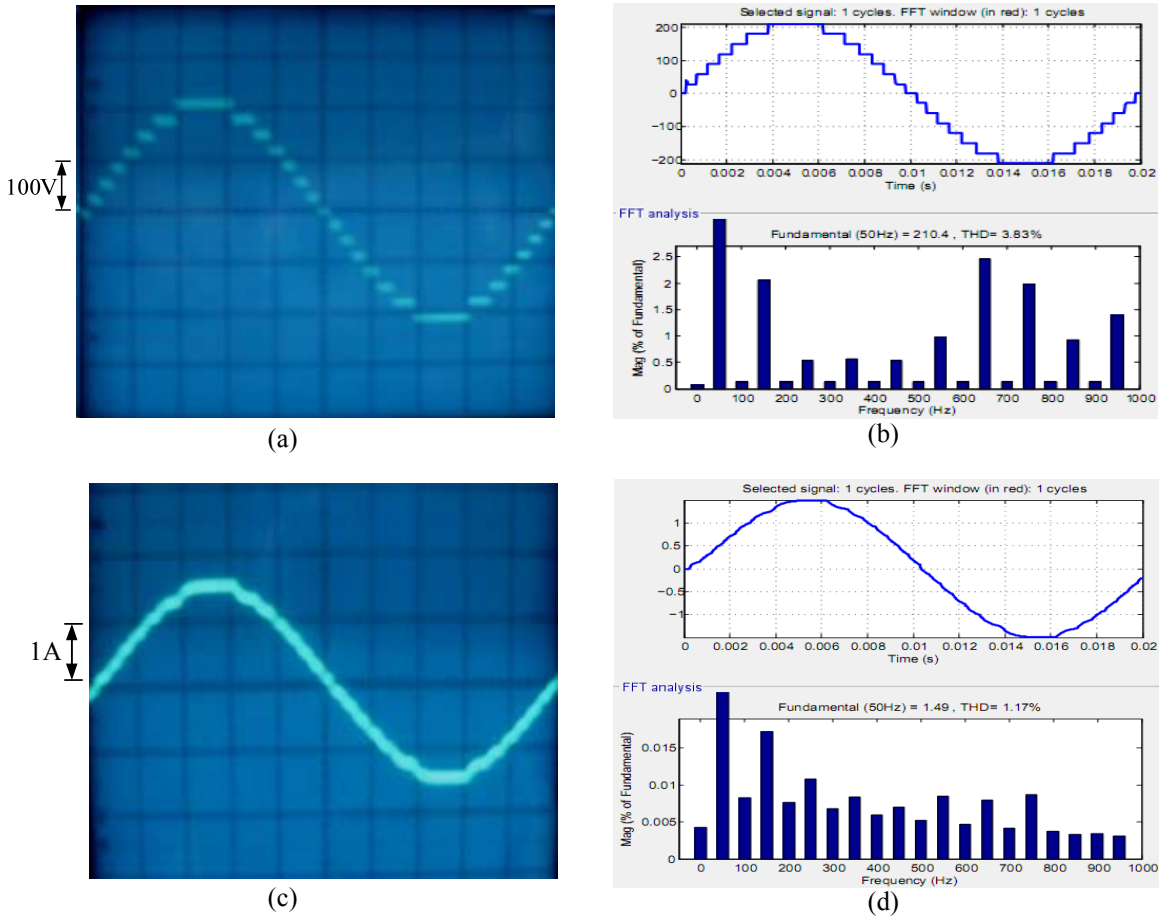

Figure 11. Simulation and measurement results (Time/div =2 ms) and (Voltage/div =10 V by1:10probe): (a) Experimental output voltage;(b) Simulation output voltage and harmonic spectrum (THD=3.83%); (c) Experimental output current; (d)Simulationoutput current and harmonic spectrum (THD= 1.17%).

7. CONCLUSION

In this paper, a new multilevel voltage source inverter has been proposed. For proposed structure, three algorithms have been presented for determination of dc sources values. These algorithms can generate all levels (odd and even) at the output voltage waveform. The comparison between the proposed topology and the conventional cascade topology has been presented. It was shown that the third algorithm required minimum number of IGBTs, gate drivers and diodes.The simulation and experimental results have been presented for a 15-level inverter based on the second algorithm to validate the ability of the proposed topology in generating of desired output voltage.

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