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A Novel Topology of Multilevel Inverter with Reduced Number of Switches and DC Sources

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ABSTRACT

This paper introduces new topology of cascaded multilevel inverter, with considerable reduction in the number of switches and DC voltage sources. The proposed topology is based on asymmetrical multilevel inverter which produces 21 levels of output with the use of 11 unidirectional switches, 3 diodes and 4 DC voltage sources. The advantages of this topology are reduction in the number of switches (2 nos.) and gate driver circuits (2 nos.), reduction in the number of DC sources (2 nos.) also cost, complexity, and space required for hardware is reduced without sacrificing the quality output of the inverter. To reduce the THD further Level shifting SPWM techniques such as PD, POD & APOD are used and comparison is shown on the basis of THDs obtained from the above SPWM techniques. Frequency of carrier waves is 1KHz, and modulation index is 1.0. To validate the proposed topology the circuit is simulated and verified by using MATLAB/Simulink.

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1. INTRODUCTION

Now-a-days, in industries, power conversion systems become very popular and are used extensively. The power conversion system includes AC-DC, DC-AC, DC-DC, AC-AC conversions. Many high and medium voltage applications require such power conversion systems. Those applications are HVDC transmission, FACTS, AC/DC drives, renewable energy sources such as PV solar cells, wind, fuel cells etc. [2]-[4]. This paper concentrates on DC-AC conversion (Inverter action). A conventional single phase inverter is able to produce voltage levels of +Vdc, 0, -Vdc, so the output waveform of the inverter is quasi-square wave, which is not advisable to use as an input to any AC system. Hence, to get nearly sinusoidal waveform, multilevel inverter is introduced in 1975 [10]. The output of multilevel inverter is a staircase wave, which is nearly sinusoidal. By increasing the number of output voltage levels in multilevel inverter the THD can be minimized. Also ripple content in the output of multilevel inverter is lesser than that of conventional inverter [9]. One more advantage that MLI possesses over the conventional inverter is voltage stress across the individual switch is lesser in case of MLI [5]. Many topologies of MLI are developed and studied. They are generally classified into:

a) Flying-capacitor inverter
b) Diode-clamped inverter
c) Cascaded H-bridge inverter

From these inverter topologies cascaded H-Bridge multilevel inverter is widely used [6]-[7]. Cascaded inverter has ‘n’ number of series connected cells, with an individual DC voltage source connected to each cell. There are two groups of cascade multilevel converters, the symmetric and the asymmetric

multilevel converters. In symmetric MLI all the DC voltage sources used are of equal magnitude, whereas in asymmetric MLI magnitudes of DC voltage sources are unequal.

In the asymmetric topologies, the values of DC voltage sources magnitudes are unequal. By giving proper switching sequence to the gate driver circuits, desired number of output voltage levels can be obtained. So the number of power electronic components required, will be reduced as compared to that of MLI with symmetrical DC voltage sources [8]. One of the advantages of asymmetrical MLI is that with the same number of switches and DC voltage sources, the number of output voltage level obtained is more, when compared to the symmetrical topology.

This paper proposes new asymmetric topology for 21- level voltage output with reduced number of switches. The proposed topology has been also analyzed without using any PWM technique. But after using SPWM techniques THD of the output can be reduced further. Three techniques of SPWM are used here and compared among themselves, to figure out the technique which gives least THD.

2. PROPOSED TOPOLOGY

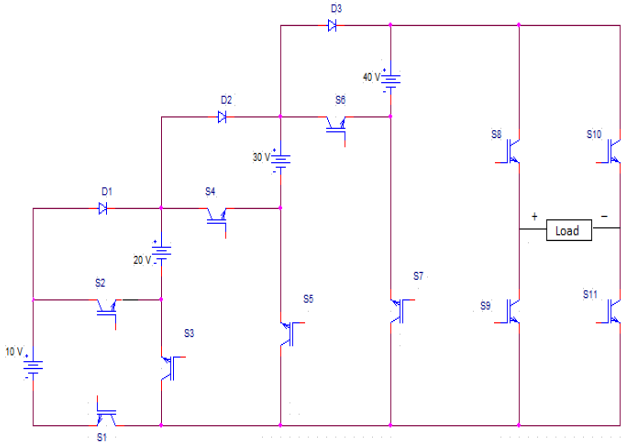

Figure 1. Proposed topology

The proposed topology has been successful in significantly reducing the switch count and no. of DC voltage sources. It consists of four asymmetrical DC voltage sources for 21 levels. Increments in the DC voltage sources are in the fashion n, 2n, 3n, 4n.... Where n = lowest DC voltage source magnitude. Proposed topology follows one relation between number of output voltage levels and number of DC sources. The relation is,

$$N_{level} = N_{DC} (N_{DC}+1) + 1$$

Where, N_{level}= Number of levels, N_{DC}= Number of DC sources.

The following table shows the switching sequence given to the proposed topology to generate 21 level voltage output.

Table 1. Switching states of proposed topology

Sr. No	Output Voltage Level	S1	S2	S3	S4	S5	S6	S7	
1	0	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
2	±Vdc	ON	OFF	OFF	OFF	OFF	OFF	OFF	
3	±2Vdc	OFF	OFF	ON	OFF	OFF	OFF	OFF	
4	±3Vdc	OFF	OFF	OFF	OFF	ON	OFF	OFF	
5	±4Vdc	OFF	OFF	OFF	OFF	OFF	OFF	ON	
6	±5Vdc	ON	OFF	OFF	OFF	OFF	ON	OFF	
7	±6Vdc	OFF	OFF	ON	OFF	OFF	ON	OFF	
8	±7Vdc	OFF	OFF	OFF	OFF	ON	ON	OFF	
9	±8Vdc	ON	OFF	OFF	ON	OFF	ON	OFF	
10	±9Vdc	OFF	OFF	ON	ON	OFF	ON	OFF	
11	±10Vdc	ON	ON	OFF	ON	OFF	ON	OFF	

H - BRIDGE

3. PULSE WIDTH MODULATION METHODOLOGY

For an n – level inverter the multicarrier PWM method uses n-1 triangular carrier signals and only one modulating sinusoidal signal is applied as reference. The zero reference is placed in the middle of the carrier set. At every instant each carrier signal is compared with the modulating sinusoidal signal. Each comparison gives one if the modulating signal is greater than the triangular carrier signal, otherwise zero. The Multicarrier PWM method is categorized into 2 groups:

1) Phase shifted PWM method, where the multiple carriers are phase shifted accordingly.

2) Carrier disposition methods (CD) where the reference signal is sampled through a number of carrier signals displaced by continuous increments of the reference signal amplitude. Further carrier disposition PWM method is grouped into three:

a) Phase Disposition (PD) Method - The phase disposition method has an equal number of carrier signals above and below the zero reference and are in phase with the same amplitude and frequency.

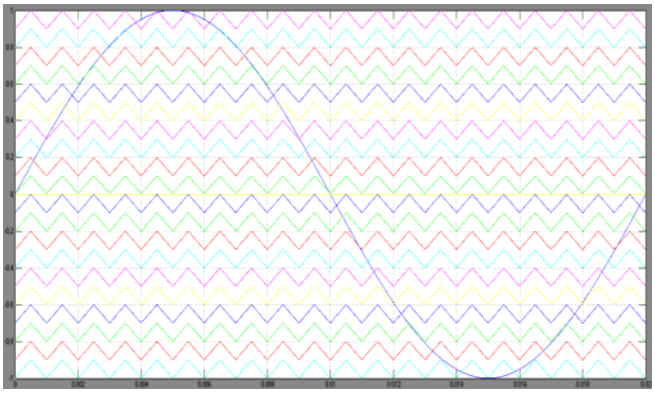

Figure 2. PD PWM

b) Alternative Phase Opposition Disposition (APOD) Method - All carrier waveforms in this APOD method are phase-displaced by 180° alternatively.

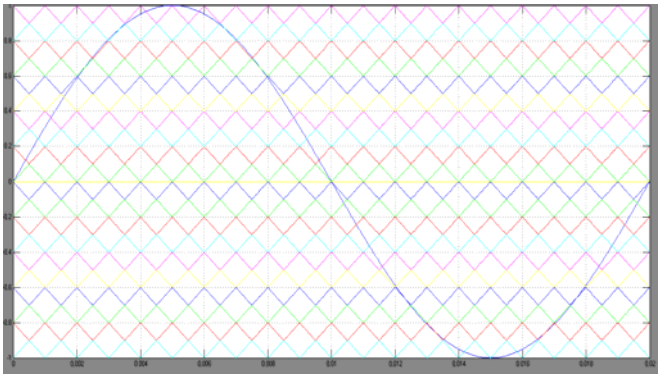

Figure 3. APOD PWM

c) Phase Opposition Disposition (POD) Method - All carrier signals above the zero reference are in the same phase but the carrier signals below the zero reference are phase shifted by 180 degrees.

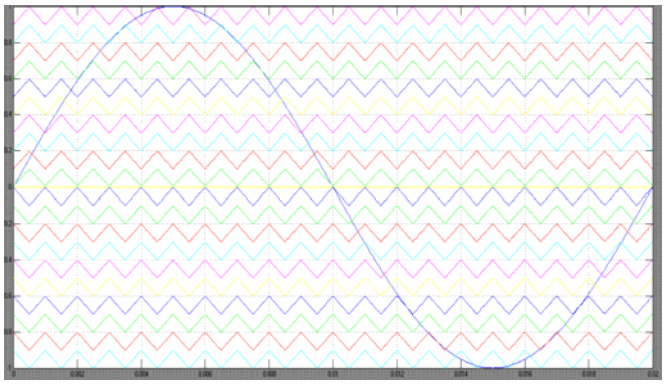

Figure 4. POD PWM

4. PULSE GENERATION CIRCUIT

For the pulse generation in the new topology 20 carriers signals are employed with the amplitude of each triangular carrier as 0.1 and frequency 1KHz. One sinusoidal wave of amplitude 1 and frequency 50 Hertz is employed as a reference signal. In order to turn on the switches in the particular desired instants, pulse generation circuit is used. In this circuit, the reference signal is compared with the carrier signal and the output of the comparison is fed to the logic gates and the required pulse pattern is generated at the output of the logic gates to trigger the switches. The pulse generation circuit implementing PD PWM technique is shown in Figure 5.

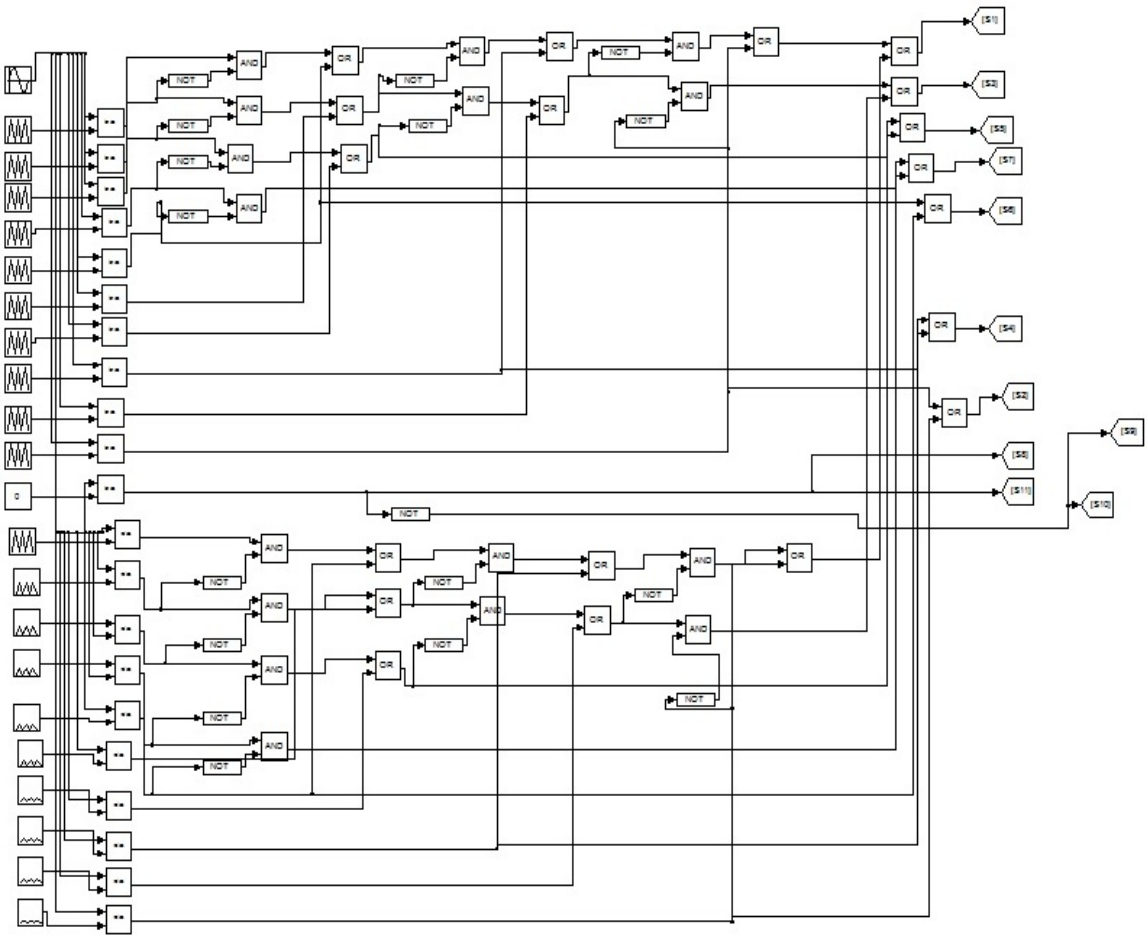

Figure 5. Pulse Generation Circuit

5. SIMULATION RESULTS

Proposed circuit is validated on MATLAB/Simulink platform. IGBT in parallel with the series RC snubber circuit is used as a switch. The magnitudes of DC voltage sources taken are 10V, 20V, 30V, 40V. Load resistance is taken as 10Ohm. Repeating sequence block is used to generate the switching sequence. Pulse generators are used to give pulses to the H - bridge. Figure 3 shows the circuit diagram of proposed topology. Figure 4 shows the 21 level output of the inverter. Figure 5 shows THD content in the output. It is **12.69%**. Figure shows THD of the output waveforms after using PD, POD, APOD PWM techniques.

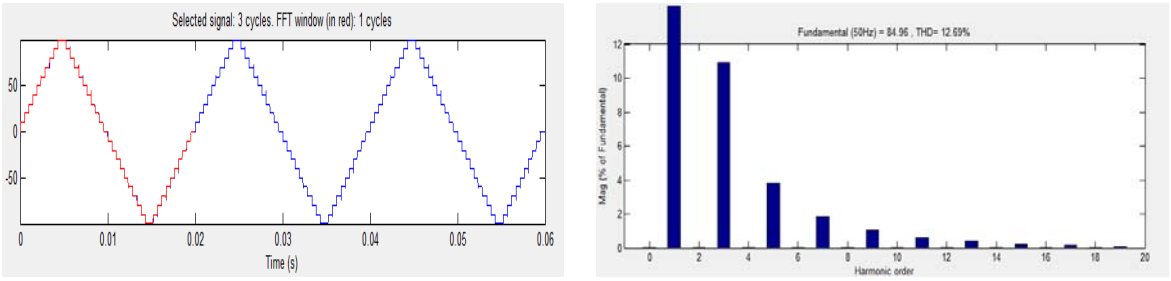

Figure 6. THD of the output waveform without any PWM technique

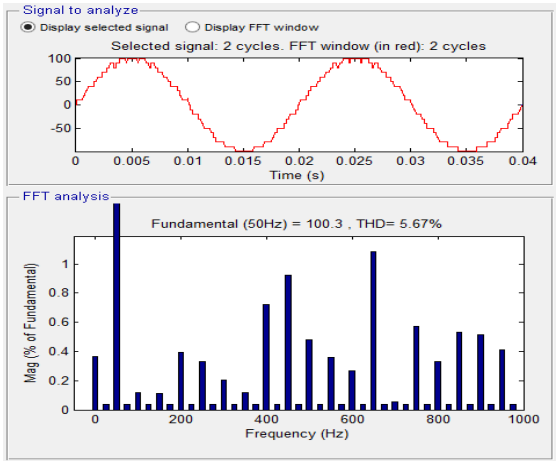

Figure 7. THD of the output waveform using PDPWM technique

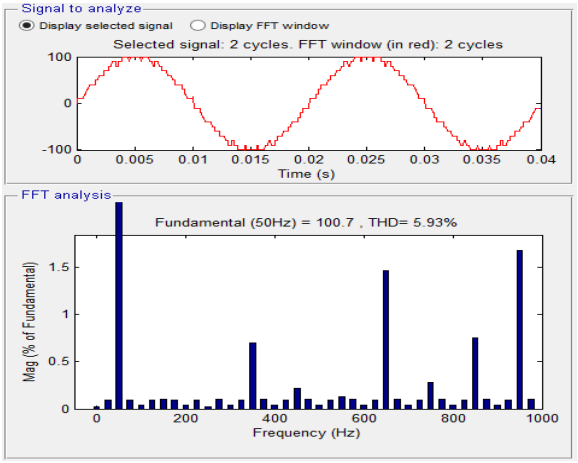

Figure 8. THD of the output waveform using PODPWM

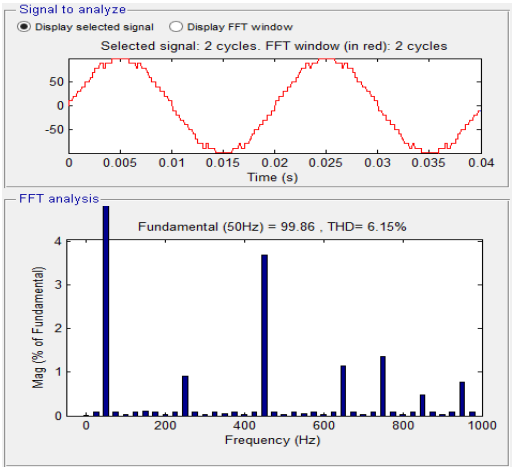

Figure 9. THD of the output waveform using APODPWM

Table 2. Comparison of SPWM techniques

Sr. No.	PWM Technique	THD (%)
1.	PD	5.67
2.	POD	5.93
3.	APOD	6.15

6. CONCLUSION

In this paper, a new topology for 21 levels is proposed with reduced number of switches and DC sources. Thus, this new circuit will require lesser hardware space, lesser cost; also the complexity of the circuit will reduce.The FFT analysis done with the fundamental switching frequency resulted in the THD of 12.69%. From the FFT analysis, it is found that PDPWM technique gives least THD. The new circuit is examined in MATLAB/Simulink. It is observed that even after the reduction in switches and sources, the desired output is obtained.

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