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FPGA Based V/f Control of Three Phase Induction Motor Drives Integrating Super-Lift Luo Converter

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ABSTRACT

The significance of Elementary Positive Output Super-Lift Luo Converter (EPOSLLC) in constant Voltage/Hertz (V/f) controlled Induction Motor (IM) drive is presented. The traditional IM drive which integrates phase controlled rectifier or boost converter in the facade end upshot tribulations like DC link fluctuations and deprived DC link voltage level. To overcome the problem, the conventional DC-DC converter is replaced with Proportional plus Integral (PI) controlled EPOSLLC in the front end of IM drive that produces the DC link voltage in geometric progression. The Voltage Source Inverter (VSI) of the suggested system renders both open loop and closed loop V/f control scheme for IM by feedback regulated Sinusoidal Pulse Width Modulation (SPWM) technique. Simulation and experimental works are conceded and results presented to demonstrate the viability of the proposed approach. Simulation is carried out using MATLAB /SIMULINK software and the experimental setup is built with Field Programmable Gate Array (FPGA) Spartan-6 processor. The anticipated EPOSLLC is found fit for V/f controlled IM drives considering the DC link Voltage, Speed response of IM and Total Harmonic Distorion (THD) in IM current.

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1. INTRODUCTION

Induction Motors are the Workhorse of the Industry due to its economy of procurement, installation and use. Recent development in the field of Power Electronics planted a wide usage of Induction Motor (IM) in the adjustable speed drives where speed control of the motor is highly required and squirrel cage type of IM is very popular in that case.The basic control involved in variable speed control of IM is application of a variable frequency and variable magnitude of AC voltage to the motor for the attainment of variable speed operation. Many techniques are already introduced to control the IM parameters [1]. However, the method by name constant Voltage/Hertz (V/f) is versatile in use. Further, the V/f technique is classified into open loop and closed loop control. The open loop V/f control of IM presented in [2] use the arrangement of Voltage Source Inverter (VSI) fed IM with source input as DC which fails to discuss the influence of DC link fluctuations in the IM drive due to load disturbance and also the results obtained are ideal. The closed loop V/f control overcomes the problem with the load disturbance that prevails in open loop V/f control of IM. However, the focus on quality DC link voltage for feedback processing is handled by means of a braking circuit [3] which complicates the system design. To introduce the importance of DC link voltage, a new model [4] is developed to utilize the DC link voltage in more efficient way, but the maximum starting current and Total Harmonic Distortion (THD) in stator current of IM are still the barrier factors of practical implementation.

In addition, using a DC link capacitor to reduce the THD in stator current of IM is developed [5] but the DC link flickering which is not suitable for feedback controlled system is not eliminated. Instead of adding a passive element to the IM drive system for the purpose of reducing THD, the view turned on to the Pulse Width Modulation (PWM) technique used to generate gate pulse for VSI through which the required variable voltage and variable frequency is attained simultaneously reducing the THD. Among different PWM techniques, the Sinusoidal Pulse Width Modulation (SPWM) [6], [7] is most popular and simple technique applicable for IM drives. In SPWM technique, two signals (a sinusoidal reference signal and a high triangular carrier signal) are compared to provide two statuses (high or low) of output. On the other hand, the ripple content in the DC link voltage destroys the feature of SPWM technique by distorting the output current of VSI. The research work [8] developed a separate DC link voltage control in addition with complex PWM control for back-back converter fed IM drive, but it is not economic for low power IM drives. The influence of DC link fluctuations over the THD of IM current and voltage is very clearly presented in [9] under different working conditions and concluded that the DC fluctuations has an effect on IM parameters. To triumph over the above mentioned drawbacks, the simple DC-DC converters such as boost, buck and buck-boost converters were introduced in the façade end of VSI fed IM drive [10], [11]. Using boost converter in IM drives, only twice the input DC is attainable in DC link [12] and hence another factor, DC link voltage level comes into play.

An advanced DC-DC converter in Super-Lift Luo converter series [13], [14] by name Elementary Positive Output Super-Lift Luo Converter (EPOSLLC) produce output voltage in geometric progression overcomes the problem that exist in conventional boost converter. However, EPOSLLC is not competent while used with constant conduction duty and the investigation [15] held to control EPOSLLC using PI regulator fails to show improvement of EPOSLLC under load and line variation.

This paper implements a superior PI control of EPOSLLC in the front end of both open loop and closed loop V/f controlled IM drives. The proposed IM drive grasp features such as DC link voltage level 1.5 times greater than the conventional boost converter reduced THD in Stator Current of IM, fluctuation free DC link voltage and improved speed regulation of IM.

2. DESIGN OF IMPROVED PI CONTROLLER FOR PROPOSED EPOSLLC

The work presented in this paper mainly focus on regulated DC-DC conversion that feeds VSI-IM drive. One of the advanced DC-DC converters from the family of positive output Super-lift Luo series have been chosen for the intended scheme. The positive output Super-lift Luo converter has some sub-series such as Main series, Additional series, Enhanced series, Re-enhanced series and Multiple-enhanced series. The elementary circuit from Main series is implemented for the proposed arrangement. The elementary circuit and equivalent circuit during switch ON and OFF are shown in Figure 1.

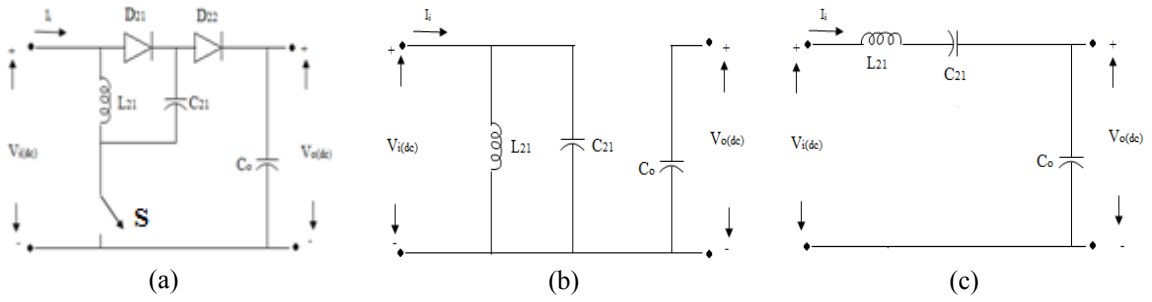


Figure 1. (a) Equivalent circuit of EPOSLLC, (b) EPOSLLC during switch ON, (c) EPOSLLC during switch OFF

The voltage across C_{21} is charged to $V_{i(dc)}$ which is the rectified input to EPOSLLC. The current through the inductor L_{21} increases with $V_{i(dc)}$ during switch ON and decreases with $-(V_{o(dc)} - 2V_{i(dc)})$ during switch OFF of EPOSLLC. The average output voltage of EPOSLLC is:

$$V_{o(dc)} = \frac{2 - \gamma}{1 - \gamma} V_{i(dc)} \quad (1)$$

Where, $V_{o(dc)}$ is the average output voltage of EPOSLLC, $V_{i(dc)}$ is the input voltage of EPOSLLC and γ is conduction duty.

The output current of EPOSLLC is:

$$I_{o(dc)} = \frac{1-\gamma}{2-\gamma} I_{i(dc)} \quad (2)$$

Where, $I_{o(dc)}$ is the average output current of EPOSLLC and $I_{i(dc)}$ is the input current of EPOSLLC. The voltage transfer gain (G) of EPOSLLC is given by:

$$G = \frac{2-\gamma}{1-\gamma} \quad (3)$$

Whereas, the voltage transfer gain of conventional boost converter is:

$$G = \frac{1}{1-\gamma} \quad (4)$$

On comparing (3) and (4), it is obvious that for the same conduction duty, EPOSLLC produce 1.5 times the voltage transfer that of the conventional boost converter.

The control strategy of EPOSLLC using PI regulator is exposed in Figure 2. The error in the actual DC link voltage with respect to the reference DC link voltage is the input to the PI controller.

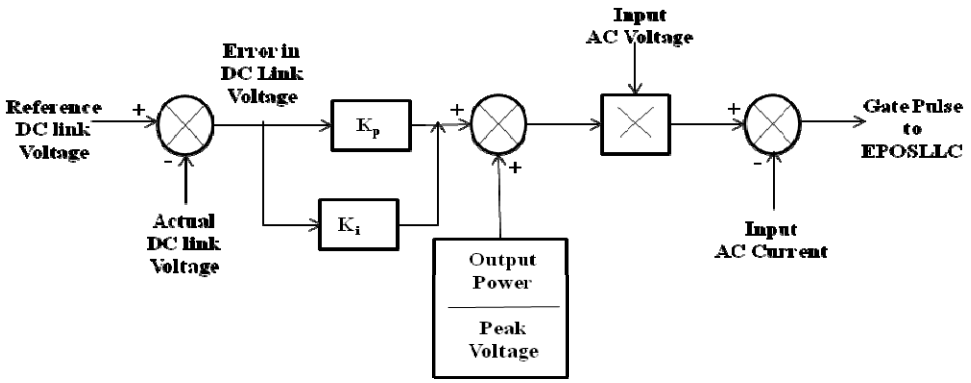


Figure 2. Control strategy of EPOSLLC

The PI controller for anticipated EPOSLLC is designed by finding the appropriate value of proportional gain (K_p) and integral time (T_i). The first step in determining K_p and T_i is to develop the state model of EPOSLLC.The state model of EPOSLLC [16], [17] is determined by assuming the state variables x_1 (current flowing through L_{21}), x_2 (Voltage across C_{21}) and x_3 (Voltage across C_o) and input variable u (input voltage of EPOSLLC). Considering negligible input and output resistance of proposed EPOSLLC, the state-space averaging model of EPOSLLC is given by:

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \end{bmatrix} = \begin{bmatrix} \frac{1}{L_{21}} & \frac{\gamma-1}{L_{21}} & \frac{\gamma-1}{L_{21}} \\ \frac{1-2\gamma}{C_{21}} & \frac{-\gamma}{C_{21}} & 0 \\ \frac{1-\gamma}{C_o} & 0 & \frac{1}{C_o} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} + \begin{bmatrix} \frac{1}{L_{21}} \\ \frac{\gamma}{C_{21}} \\ \frac{1}{C_o} \end{bmatrix} u \quad (5)$$

Based on Zeigler – Nichols tuning method [18], K_p and T_i are resolved by applying the step input to the mathematical model (5) of EPOSLLC to attain S – shaped curve and is shown in Figure 3. By drawing a

tangential line to the S-shaped curve gives the constants delay time (L = 0.005s) and time constant (T = 0.015s). From the value of L and T, the K_p (9.36) and T_i (0.016s) are straight away resoluted from Zeigler – Nichols chart.

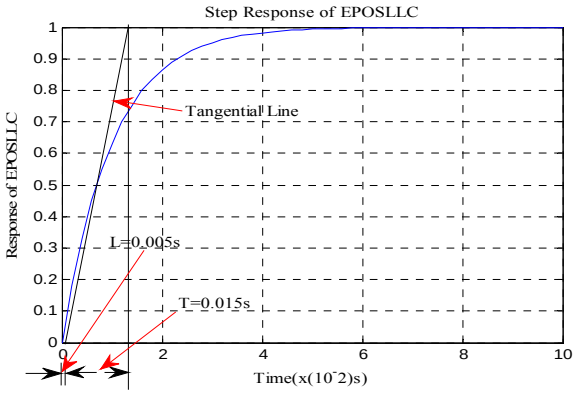


Figure 3. S-shaped step response of EPOSLLC

3. DRIVE TOPOLOGY OF PROPOSED SCHEME AND CALCULATION OF IM PARAMETERS

This section explains the two different topologies of IM drive intended and followed by IM parameters calculation. Figure 4 and Figure 5 shows the open loop and closed loop V/f control topology of proposed scheme.

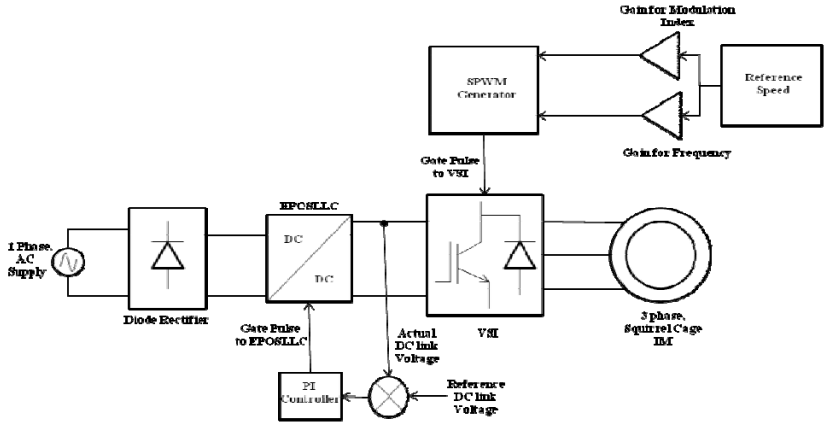


Figure 4. Proposed Scheme with Open Loop V/f Control Topology

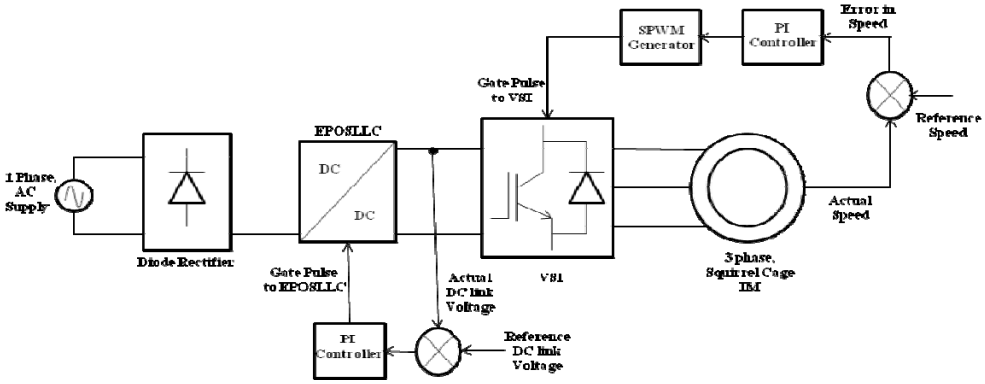


Figure 5. Proposed Scheme with Closed Loop V/f Control Topology

Both the scheme presented above incorporates PI controlled EPOSLLC arrangement in the façade end of VSI. The open loop V/f controlled IM drive depicted in Figure 4 process the reference speed that is multiplied with the fixed gain values of modulation index and frequency of the reference sine wave used in SPWM technique for generating gate signals to VSI. Whereas, the closed loop V/f controlled IM drive shown in Figure 5 uses the PI controller for regulating the error in speed of IM via SPWM technique.

Apart from the control technique discussed above, the critical parameter estimation of IM is necessary and to assess, the per-phase equivalent circuit of IM in the proposed scheme is designed and shown in Figure 6. In Figure 6, the different parameters of IM are Stator resistance (R_S), Stator inductance (X_S), Stator phase current (I_S), Mutual Inductance (X_M), Magnetizing Current (I_M), Rotor resistance (R_R), Rotor inductance (X_R), Rotor current (I_R) and Slip (S). For the case presented, the required speed of IM is 1000rpm and the factors such as IM current, Power factor (P.F.) and efficiency (η) are calculated in this section.

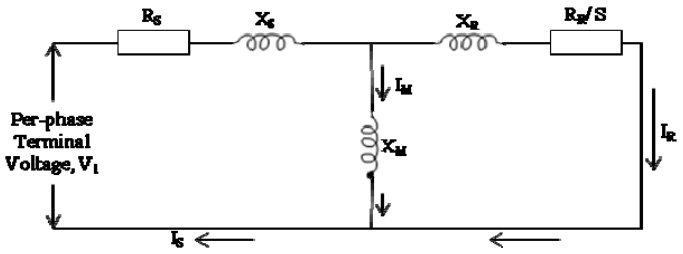


Figure 6. Per-Phase Equivalent circuit of Proposed IM

Using Kirchoff's Current law, the primary phase current of IM is specified by,

$$I_S = I_M + I_R \tag{8}$$

The expression for magnetizing current (I_M) is,

$$I_M = \frac{E_S}{jX_M} \tag{9}$$

Where, E_S is internal e.m.f. of IM.

The rotor current is,

$$I_R = \sqrt{\frac{(\omega)(S)(T)}{R_R(1 - S)}} \tag{10}$$

Where, ω is the required speed of IM, in (rps) and T is the torque developed by IM. From (9) & (10), the phase current of IM is determined and the efficiency of IM is given by:

$$\eta = \frac{P_O}{P_O + P_L} \tag{11}$$

Where, P_O is power output by IM and P_L is the IM losses.

The output power and losses of IM is given by:

$$P_O = \frac{(1 - S)\, P_{link}}{S} \tag{12}$$

$$P_L = 3(|I_S|^2 R_S + |I_R|^2 R_R) \tag{13}$$

Where, P_{link} is the DC link power of the IM drive.

From (12), it is understandable that the deprived DC link voltage reduces the magnitude of DC link power and tends to huge drop in output power of IM. This proves that the DC link voltage plays a vital role in the efficiency point of IM. The various factors discussed above were calculated for the anticipated scheme of 400V, 50Hz, 1410rpm, 0.5HP, three phase IM and are tabulated in Table 1.

Table 1. Calculated Values

IM Parameters	Calculated Value
Motor Current	1.736 A
Power Factor	0.926
Efficiency	96 %

4. SIMULATION WORK AND RESULTS

To validate the effectiveness of projected scheme, the Simulink model of 'EPOSLLC adapted V/f control of IM drive' is designed and the simulation is conceded using MATLAB 2012a software. The Simulink model is developed for both Open loop and closed loop V/f controlled IM drive with same arrangement of EPOSLLC in the front end and holds invariable simulation circuit parameters which is shown in Table 2.

Table 2. Simulation Circuit Parameters

Parameter	Rating
Input AC Supply	1 phase, 100V, 50Hz
Induction Motor (IM)	0.5 hp ,3-phase, 50Hz,400V
Stator Resistance of IM	11.1Ω
Stator Inductance of IM	18.8mH
Rotor Resistance of IM	12.3Ω
Rotor Inductance of IM	26.7mH
Mutual Inductance	467mH
Inductor	L_{21} = 2.56mH
Capacitors	C_{21} = 2000μF, C_o = 2200μF

The Simulation results such as output voltage of EPOSLLC and line output voltage of VSI remains same for both the simulated Open loop and closed loop V/f controlled IM drive, because the load disturbance affects only the stator current and speed of IM in proposed scheme. To authenticate the preliminary feature of the developed method, the DC link voltage (i.e.) the output voltage of proposed EPOSLLC is shown in Figure 7.

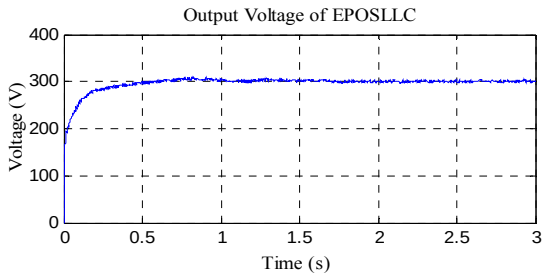


Figure 7. Output Voltage of proposed EPOSLLC

The above result shows that for 100V rectified input, EPOSLLC produce ripple free 300V DC voltage and verifies the effectiveness of PI controlled EPOSLLC ideally. The output line voltage of VSI in the proposed scheme is shown in Figure 8.

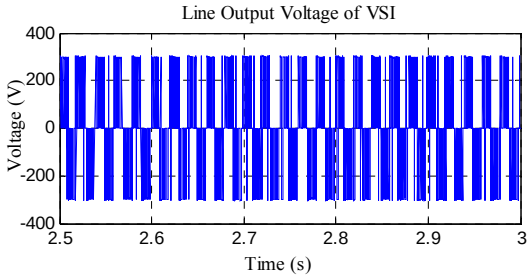


Figure 8. Line Output Voltage of VSI in the proposed scheme

The speed response of IM for proposed open loop and closed loop V/f controlled IM drive is presented in Figure 9.

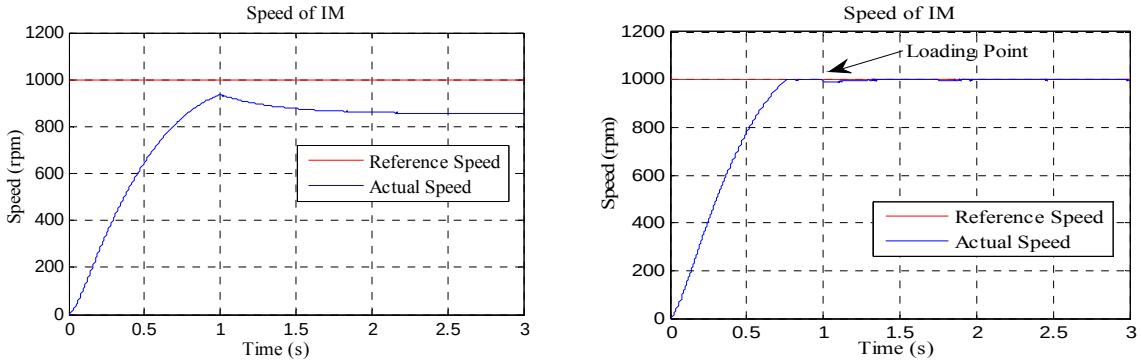


Figure 9. Speed response of IM for 0.5N.m load disturbance at 1s (a) during open loop V/f control (b) during closed loop V/f control

The raise time of speed to attain the reference rpm is very low for closed loop V/f controlled IM drive when compared with open loop V/f controlled IM drive and during the load disturbance, the open loop V/f controlled IM drive fails to attain the speed at least nearby the reference. Whereas, the closed loop V/f control effectively regulates the error in speed during load commotion. Figure 10 shows the stator current of IM in the proposed scheme during load disturbance.

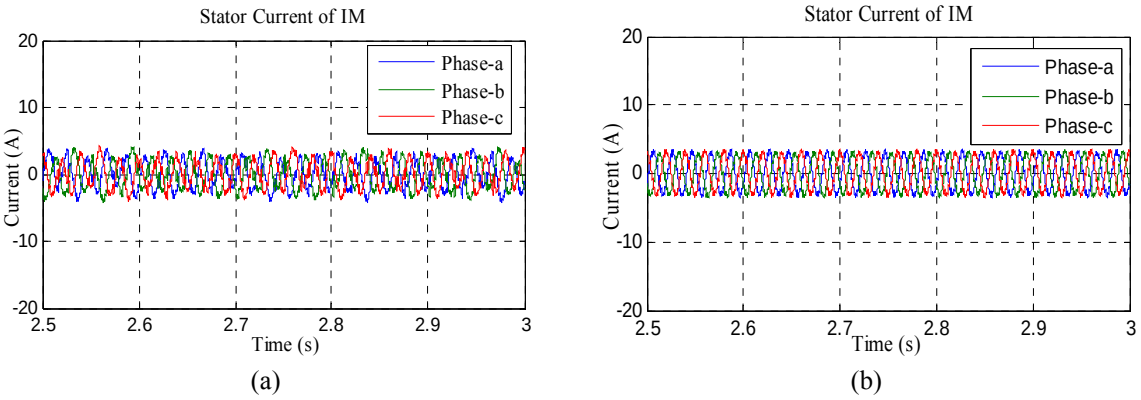
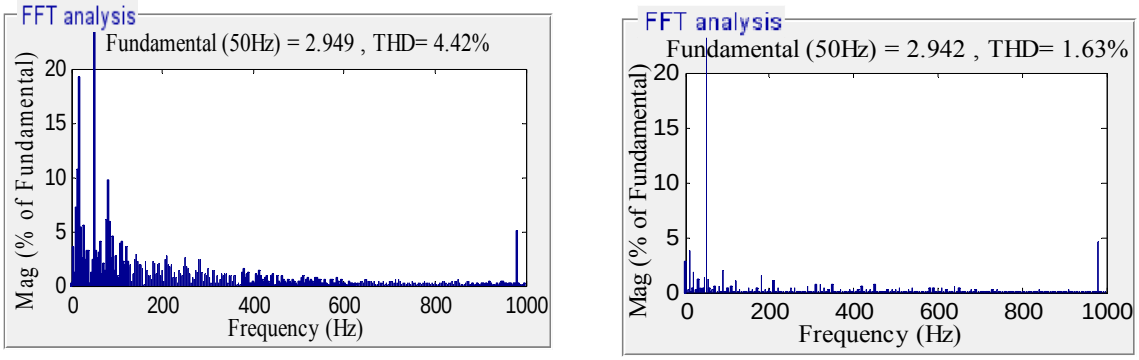


Figure 10. Stator Current of IM (a) Open loop V/f control (b) Closed Loop V/f control

From Figure 10, it is apparent that the undulation in the stator current of IM is high during open loop V/f control when compared with the stator current of IM during closed loop V/f control operation and corresponding THD in stator current for both the schemes were presented in Figure 11.



(a) (b)

Figure 11. THD in stator current of IM (a) during open loop V/f control (b) during closed loop V/f control

5. EXPERIMENTAL WORK AND RESULTS

The Hardware model of the proposed open loop and closed loop V/f controlled IM drive incorporated with PI controlled EPOSLLC is shown in Figure 12 and Table 3 show the experimental parameters used in the proposed configuration. The separate algorithm for open loop and closed loop V/f control topology is developed which is embedded in FPGA spartan-6 processor for generating gate pulse to VSI.

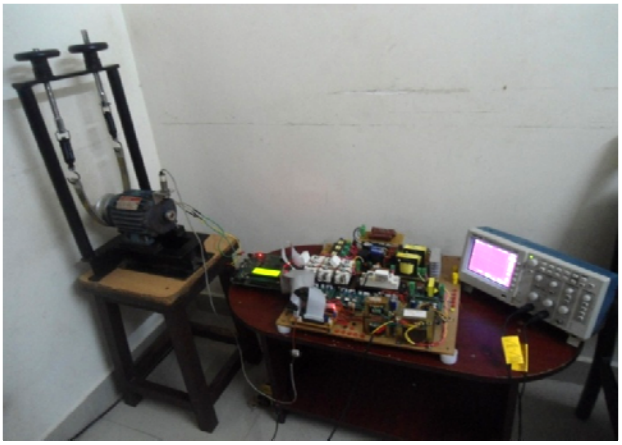
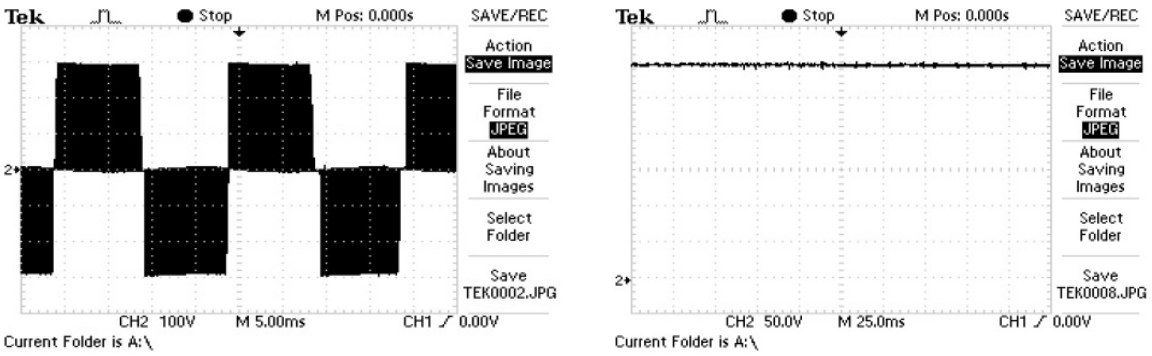


Figure 12. Hardware model composed of 1phase AC supply, Power Electronic converters, FPGA processor, IM and Tektronix Oscilloscope

Tablel 3. Experimental Parameters

Parameter	Rating
Input AC Supply	1 phase, 100V, 50Hz
Inductor	L_{11} = 3mH, L_{21} = 2.56mH
Capacitors	C_{21} = 200μF, C_o = 1320μF
Diodes	MVR3060, 600V, 30A
Voltage Source Inverter	IGBT Inverter
Switches	SKM100GB12T4, 1200V, 100A, 20Khz switching Frequency
Three phase Induction motor	0.5 hp ,3-phase, 50Hz,400V
Processor	FPGA Spartan-6

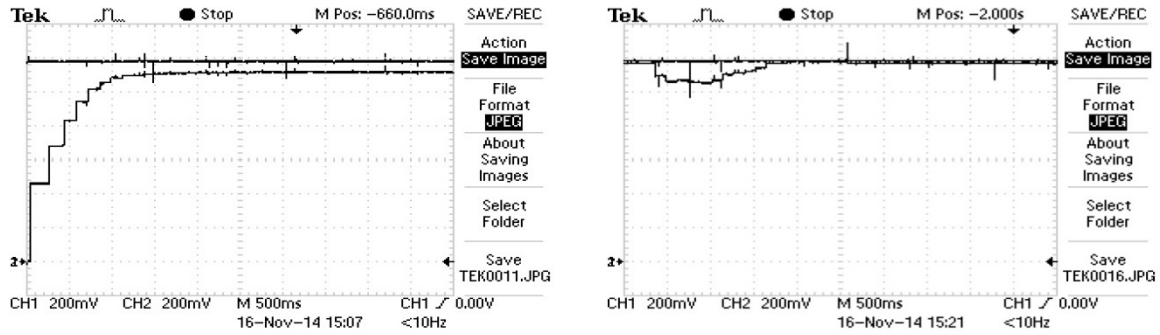
The IM terminal voltage (line voltage of VSI) and DC link voltage is presented in Figure 13.



(a) (b)

Figure 13. (a) Line output voltage of VSI (CH2) with x-axis scale (1div. = 5ms) and y-axis scale (1div. = 100V) (b) DC link Voltage (CH2) with x-axis scale (1div. = 25ms) and y-axis scale (1div. = 50V)

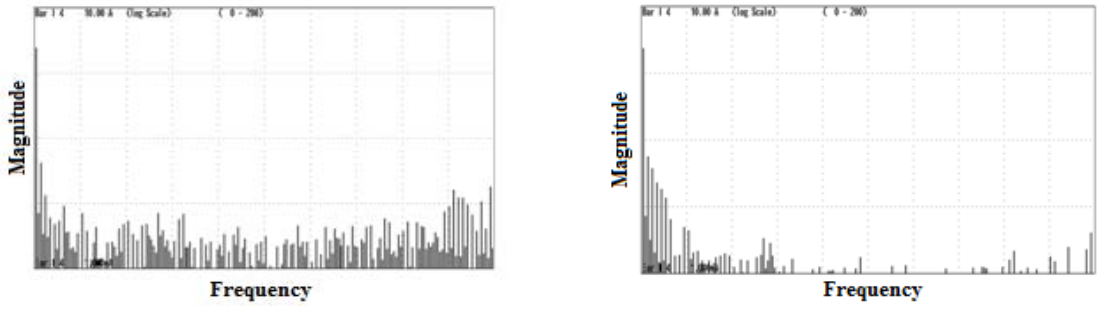
The speed of IM in the experimental setup is measured at the terminals of Spartan-6 processor through a digital to analog convertor and hence the speed response is measured in terms of voltage. Figure 14 shows the speed response (Channel-1) of IM for 1000rpm reference speed (Channel-2) and the load torque of 0.5N.m applied at 400ms. The result of speed response validates the feasibility of closed loop V/f control over open loop V/f control for the proposed model.



(a) (b)

Figure 14. Speed response of IM for load disturbance (a) during open loop V/f control (b) during closed loop V/f control with x-axis scale (1div. = 500ms) and y-axis scale (1div. = 166.66rpm)

The THD in the stator current during the experimental work is measured and is shown in Figure 15.



(a) (b)

Figure 15. THD in Stator current of IM (a) during open loop V/f control (b) during closed loop V/f control

The THD in the stator current of IM during open loop V/f control is around 5% and during closed loop V/f control is around 2% which legalizes the simulation result presented in Figure 11.

6. CONCLUSION

This paper presents the improved PI control of EPOSLLC incorporated in the façade end of open loop and closed loop V/f controlled IM drive. Experimental and Simulation results such as DC link voltage, speed response of IM and THD in the stator current of IM are obtained. On observing the speed response of IM, the regulation time for load disturbance is very low for closed loop V/f control of IM drive in both simulation and hardware test, which validates the effectiveness of closed loop V/f control over open loop V/f control without complex design. On the other hand, the speed response of IM during open loop V/f control suggest that such control technique is accepted only for the applications like water pumping, compressors, etc., where the speed change of IM is not required. The DC link ripple free voltage waveform verifies the usefulness of proposed EPOSLLC in both the arrangements of IM drives. The scheme suggested utilize minimum rectified DC voltage for driving a three phase IM and therefore, the design using renewable energy as a source by eliminating the single phase AC supply cascading diode rectifier is possible. Basis of future work has been left for the alteration and implementations of experimental drives under involvement of some other control techniques.

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