A Novel Approach of Position Estimation and Power Factor Corrector Converter Fed BLDC Motor

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Article Info	ABSTRACT					
Article history:	This paper proposes a Power factor Corrected (PFC) Bridgeless Buck-Boost					
Received Nov 2, 2014 Revised Dec 20, 2015 Accepted Jan 14, 2015	converter fed BLDC motor drive. The Bridgeless configuration eliminates the Diode Bridge Rectifier in order to reduce the number of components and the conduction loss. The position sensors used in BLDC drives have drawbacks of additional cost, mechanical alignment problems. These bottle necks results in sensorless technique. The Sensorless technique mostly relies on measurement of Back EMF to determine relative positions of stator and rotor for the correct coil energising sequence can be implemented. This paper					
Keyword:						
BLDC motor Bridgeless Buck-boost converter Discontinuous inductor current Finite element method Power factor correction Power quality	introduces the offline Finite Element method for sensorless operation. The proposed sensorless scheme estimates the motor position at standstill and running condition. The obtained Power Factor is within the acceptable limits IEC 61000-3-2. The proposed drive is simulated in MATLAB/Simulink the obtained results are validated experimentally on a developed prototype of the drive. <i>Copyright</i> © 2015 Institute of Advanced Engineering and Science. <i>All rights reserved.</i>					
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1. INTRODUCTION

Recently lots of research on sensorless control technique for BLDC motor has been conducted. It has been understood that it has various advantages than conventional motors. The advantages are Elimination of motor neutral voltage, Elimination of fixed phase shift circuit, low starting speed, cost effective [1-8]. Also this motor is becoming famous due to its high efficiency, high flux density per unit volume, low maintenance requirements, low EMI problems. These BLDC motors can be applied in transportation, HVAC, motion control, industrial tools, and medical equipment [9-12]. The proposed system is applied in Lift/elevator application.

The BLDC motor is employed with a position sensor for absolute sensing of the rotor position. This results in more mechanical connections and higher cost. In order to overcome these drawbacks the Sensorless method has been introduced. There are various Sensorless techniques for BLDC motor. This paper introduces the Finite-Element-method (FEM) for absolute sensing of the rotor position using position and speed observer method which determines the rotor position at both standstill and running conditions [1].

This method uses the zero-crossing between the line-to-line PM flux linkage that occurs right in the middle of two commutation points (CP). The position between CPs is obtained by comparing the estimated line-to-line PM flux with the FEM-calculated line-to-line PM flux [1].

The Unity power factor is the aim of every electric utility. Suppose if the power factor is less than 1, then more amount of current has to be supplied for the given power use. Hence, the power factor has to be

adjusted nearly to 1. This paper introduces the Power Factor Corrected (PFC) Bridgeless Buck-Boost converter.

When a BLDC motor is fed by the Diode Bridge Rectifier (DBR) with the DC-link capacitor of high value it draws the peak current which suppress the value of Total Harmonic Distortion (T.H.D) about 65% and power factor nearly 0.82 [6]. Hence, this single stage power conversion is employed for improvement in efficiency and less component count.

Comparing BL SEPIC and Cuk converters, the BL Buck-Boost converters gained more advantage for applications requiring a wide range of dc link voltage control [5]-[11]. i.e., bucking and boosting mode. This provides the voltage buck or voltage boost which limits the operating range of the dc link voltage control.

2. PROPOSED PFC BRIDGELESS BUCK-BOOST CONVERTER

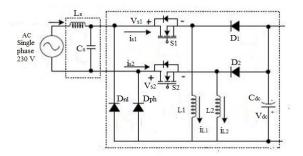


Figure 1. Proposed PFC BL Buck-Boost converter

In the proposed configuration of bridgeless buck-boost converter has the minimum number of components and least number of conduction devices during each half cycle of supply voltage into two parts which include the operation during the positive and negative half cycles of the supply voltage and complete switching cycle [13].

_ r.	- Participant								
	Configuration	Number of Devices				3	1/2 period	Suitability	
		S	С	L	D	Total	conduction		
-	BL- Buck	2	2	2	4	10	5	No	
	BL-Boost	2	1	1	2	6	4	No	
	BL-Cuk	2	3	3	3	11	7	Yes	
	BLSEPIC	2	2	2	3	9	7	Yes	
	Proposed	2	1	2	4	9	5	Yes	

Table 1. Comparison of Number of Components of the Proposed with the Existing Topologies

2.1. Operation of the Proposed Converter in Positive and Negative Half Cycle

In this mode converter switches S_1 and S_2 are operate in positive and negative half cycle of supply voltage respectively. During positive half cycle switch S_1 , inductor L_1 and diodes D_1 and D_2 are operated to transfer energy to DC link capacitor C_{dc} . Similarly in negative half cycle of supply voltage switches S_2 , inductor L_2 and D_2 conducts. In Discontinuous Inductor Current Mode (DICM) operation of converter the current in the inductor L_1 becomes discontinuous for certain duration in a switching period.

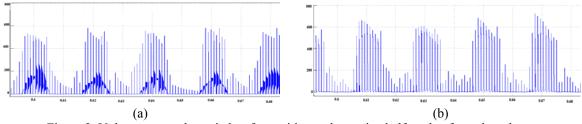
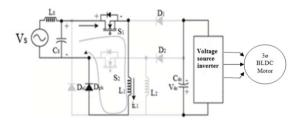


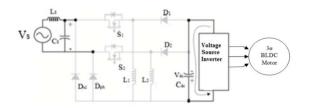
Figure 2. Voltage across the switches for positive and negative half-cycle of supply voltage

2.2. Operation during Switching Cycle

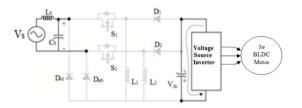
Mode I: In this mode, switch S_1 conducts for charging the inductor L_1 , hence the inductor current iL_1 increases in this mode. Diode D_{ph} completes the input side and the DC link capacitor C_{dc} is discharged by VSI fed BLDC motor.



Mode II: In this mode of operation switch S_1 is turned off and the stored energy from the inductor L_1 is transferred to DC link capacitor C_{dc} till the inductor is fully discharged and current in the inductor is fully reduced to zero.



Mode III: In this mode of operation inductor Li_1 operate in discontinuous conduction mode and diodes and switch are in off condition. At this time DC link capacitor C_{dc} starts discharging. This operation can be continuing up to switch S_1 is turned on again.



3. DESIGN OF PFC BL BUCK-BOOST CONVERTER

A PFC BL buck-boost converter is designed to operate in DICM such that the current in inductors i_{L1} and i_{L2} becomes discontinuous in a switching period. For a supply voltage with an rms value of 200 V, the average voltage appearing at the input side is given as:

$$V_{in} = \frac{2\sqrt{2}V_{s1}}{\pi} = \frac{2\sqrt{2}\times200}{\pi} \cong 180V$$
(1)

The voltage conversion ratio is given by,

$$d = \frac{V_{dc}}{V_{in} + V_{dc}} \tag{2}$$

In the proposed converter the dc link voltage is designed 50 V as the minimum value & 450 V as the maximum voltage with 100 V as the nominal value. Hence, the corresponding duty ratio of $V_{dcmin} \& V_{dcmax}$ is calculated as 0.2 and 0.69 respectively.

3.1. Design of Input Inductors

The value of inductance L_{ic1} , to operate in critical conduction mode in the buck–boost converter is given as:

$$L_{icI} = \frac{R_e (1-d)^2}{2f_s}$$
(3)

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Where R_e is the equivalent resistance, d is the duty ratio and f_s is the switching frequency.

Now, the value of L_{ic1} is calculated at the worst duty ratio of d_{min} such that the converter operates in DICM even at very low duty ratio. At minimum duty ratio, i.e., the BLDC motor operating at 50 V (V_{demin}), the power (P_{min}) is given as 90 W (i.e., for constant torque, the load power is proportional to speed). Hence, the value of inductance L_{iemin} corresponding to V_{demin} is obtained as:

$$L_{icmin} = \frac{V_{dcmin}^2}{P_{min}} \times \frac{(1 - d_{min})^2}{2f_s}$$

= $\frac{50^2}{90} \times \frac{(1 - 0.2016)^2}{2 \times 2000}$
= 442.57 μH (4)

The values of inductances L_{i1} and L_{i2} are taken less than 1/10th of the minimum critical value of inductance to ensure a deep DICM condition. The analysis of supply current at minimum duty ratio (i.e., supply voltage as 200 V and dc link voltage as 50 V) is carried out for different values of the inductor (L_1 and L_2).

3.2. Design of DC Link Capacitor (C_{dc})

The design of the dc link capacitor is governed by the amount of the second-order harmonic (lowest) current flowing in the capacitor and is derived as follows. For the PFC operation, the supply current (Is) is in phase with the supply voltage (Vs). Hence, the input power Pin is given as:

$$P_i = 2\sqrt{2V_{s1}} \sin \omega t * \sqrt{2I_{s1}} \sin \omega t V_{s1}I_{s1}(1 - \cos 2\omega t)$$

Where the latter term corresponds to the second order harmonic, which is reflected in the dc link capacitor as

$$I_s(t) = \frac{V_{s1}I_{s1}}{V_{dc}}\cos 2\omega t \tag{5}$$

The dc link voltage ripple corresponding to this capacitor current is given as:

$$\Delta V_{dc} = -\frac{1}{c_{dc}} \int i_s(t) dt = -\frac{I_{dc}}{2\omega c_{dc}} \sin 2\omega t$$
(6)

For a maximum value of voltage ripple at the dc link capacitor, $Sin(\omega t)$ is taken as 1. Hence, (6) is rewritten as:

$$C_{dc} = \frac{I_{dc}}{2\omega\Delta V_{dc}} \tag{7}$$

Now, the value of the dc link capacitor is calculated for the designed value V_{dcdes} with permitted ripple in the dc link voltage (ΔV_{dc}) taken as 3% as:

$$C_{dc} = \frac{\frac{P_o}{V_{dc\,des}}}{2\omega\Delta V_{dc}} = \frac{\frac{350}{100}}{2\times314\times0.03\times100}$$

= 1857.7 \mu F (8)

Hence, the nearest possible value of dc link capacitor C_{dc} is selected as 2200 $\mu\text{F}.$

3.3. Design of Input Filter (L_s and C_s)

A second-order low-pass LC filter is used at the input side to absorb the higher order harmonics such that it is not reflected in the supply current. The maximum value of filter capacitance is given as:

$$C_{max} = \frac{l_{peak}}{\omega_L v_{peak}} = \frac{350}{220} \frac{1}{314 \times 220\sqrt{2}} \tan 1^{\circ} = 401.98 \, nF$$
(9)

Where I_{peak} , V_{peak} , ω_L , and θ represent the peak value of supply current, peak value of supply voltage, line frequency in radians per second and displacement angle between the supply voltage and supply current, respectively. Hence, a value of C_f is taken as 330 nF.

4. PROPOSED BLOCK DIAGRAM

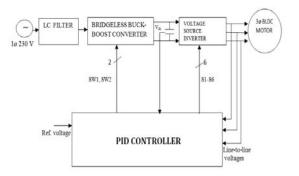


Figure 3. Block Diagram of proposed system

The configuration of bridgeless buck-boost converter has the minimum number of components and least number of conduction devices during each half cycle of supply voltage which governs the choice of BL buck-boost converter for Lift/elevator application.

The inverter does reverse of what ac-to-dc converter does. Even though input to an inverter circuit is a dc source, it is not uncommon to have this dc derived from an ac source such as utility ac supply. Here, the final ac output may be of a different frequency and magnitude than the input ac of the utility supply.

The rotor position is detected using the finite element Method (FEM). This project proposes and investigates a new offline FEM- assisted position and speed observer for BLDC-PM motor drive sensorless control based on the line-to-line PM flux linkage estimation [1]. Using measured phase currents and line-to-line voltages the line-to-line PM flux can be estimated.

5. SENSORLESS OPERATION OF BLDC MOTOR

This paper proposes the FEM assisted sensorless control of BLDC motor done by estimating the line-to-line PM flux linkage. To obtain quasi-square current waveforms, the position of CP's are required. By comparing the line-to-line PM flux linkage with the calculated FEM the position between the CP's is obtained. The line-to-line PM flux linkages can be estimated by direct measurement of line-to-line voltages and phase currents. The another method of calculating the line-to-line voltages by using dc bus voltage and switching status.

5.1. Commutation Approach and Position Estimation

The origin for operation of position and sensorless speed observer is the time period of zero crossing of one CP and the time period of zero crossing of another CP are made equal to each other. In each sector only two modes conduct leaving the third phase open. The voltage in the open phase is equal to the back EMF which is unseen in the controller. In each mode only one line-to-line PM flux linkage is used.

The Voltage model in the stator reference frame is the method employed in Line-to-Line PM flux linkage estimator. To reduce the phase delay a first-order Low-pass filter (LPF) is used as the equivalent integrator with speed adaptive time constant (T_c) to attenuate the output dc offset (equal with $T_c \times$ input dc offset).

Table 2. Line-to-Line PM Flux Linkage				
Rotor Sectors	Estimation of Speed			
Mode a and a	$ ho_{PMab}$			
Mode b and b'	$ ho_{PMbc}$			
Mode c and c'	<i>Р</i> _{РМса}			

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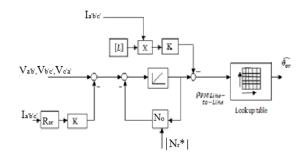


Figure 4. FEM assisted position estimation

$$H(s) = \frac{T_c}{T_c s + 1}, \ T_c = \frac{1}{N_o}$$

Where N_o depends on the reference speed N_{r^*} .

5.2. Speed Estimation

In Sensorless BLDC motor with no position sensors and position estimation, the speed estimation is anticipated by using the information from the commutation controller. The pulses are generated from the estimated position. The 18 pulse edges are formed from every 20° electrical angle. The Speed is considered using the time T between the two pulse edges. At every pulse edge the new speed computation is obtainable. Between two pulses the speed is kept at the old value.

$$N = \frac{2 . \pi}{T - N_{edges}}$$

Where N_{edges} is the number of edges.

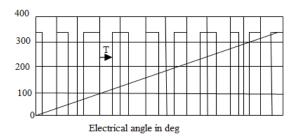


Figure 5. Pulse edges based speed estimation

The required speed can be obtained by keeping the Load torque, T_L value as constant. The Speed varies linearly with time and attains the constant value for the given period of time.

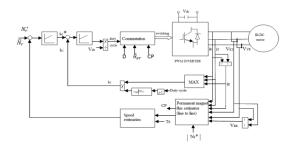


Figure 6. Proposed FEM-assisted PM-BLDC motor drive

6. SIMULATION RESULTS

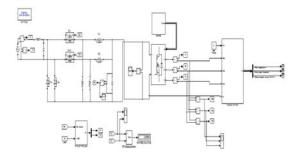


Figure 7. Simulation model of proposed system

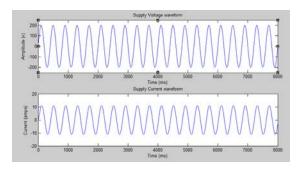


Figure 8. Supply Voltage and Current

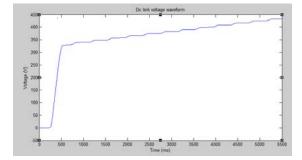


Figure 9. Variation of DC link voltage regulation

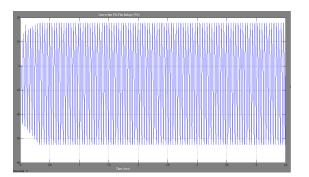


Figure 11. Line-to-Line PM flux linkage (Wb)

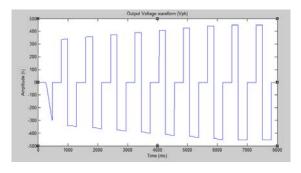


Figure 10. Output of the voltage source inverter

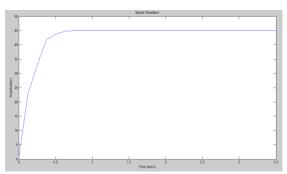


Figure 12. Variation of Speed (rpm)

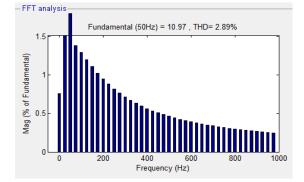


Figure 13. Harmonic spectra of supply current

				- minut j	010 01 0110	1000000	59500111101
	Vs	Is	Vref	V _{dc}	Power	Speed	T.H.D
_					factor		
	80	12	120	175	0.9984	120	2.89 %
	100	12	120	220	0.9984	120	2.89 %
	200	12	120	433	0.9984	120	2.89 %
_	300	12	120	160	0.9984	120	2.89 %

Table 3. THD and Power factor analysis of the Proposed system for $T_L = 3 \text{ NM}$

7. DISCUSSION ON RESULT

The Proposed project is simulated in MATLAB/Simulink. The THD of supply current at ac mains with output power for the proposed scheme of the BL buck–boost converter fed sensorless BLDC motor drive is achieved within the IEC 61000- 3-2 limits. The evaluation is based on the control requirement and losses in the PFC converter and VSI-fed BLDC motor. The speed remains constant in spite of change in voltage. The obtained current Total Harmonic Distortion (T.H.D) is 2.89%. The simulation results the Power Factor in 0.9999 which is nearer to the Unity Power factor, doesn't cause Power Quality issues at ac mains.

8. CONCLUSION

A PFC BL buck-boost converter-based VSI-fed BLDC motor drive has been proposed targeting Lift/elevator application. A new method of speed control has been utilized by controlling the voltage at dc bus. The front-end BL buck-boost converter has been operated in DICM for achieving an inherent power factor correction at ac mains. A satisfactory performance has been achieved for speed control and supply voltage variation with power quality indices within the acceptable limits of IEC 61000-3-2. Moreover, voltage and current stresses on the PFC switch have been evaluated for determining the practical application of the proposed scheme. A FEM assisted position and speed observer for BLDC-PM motor drive sensorless control based on the line-to-line PM flux linkage.

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