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Analysis of Binary DC Source Reduced Switch 7-level Inverter

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ABSTRACT

This paper proposes a binary DC source reduced switch 7-level inverter. Binary DC source reduced switch inverter is triggered by the Unipolar PWM strategy having sinusoidal and trapezoidal reference with triangular carriers. These pulse width modulating (PWM) strategies include phase disposition (PD), alternate phase opposition disposition (APOD), carrier overlapping (CO). Performance factors like total harmonic distortion (THD), VRMS (fundamental) and crest factor are evaluated for various modulation indices. Simulations were performed using MATLAB-SIMULINK. It is observed that UPDPWM strategy with trapezoidal reference provides output with relatively low distortion and UCOPWM strategy with trapezoidal reference provides relatively higher fundamental RMS output voltage.

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1. INTRODUCTION

The main function of a multilevel inverter is to produce a desired ac voltage waveform from several levels of dc voltages. These dc voltages may or may not be equal to one another. The ac voltage produced from these dc voltages approaches a sinusoid. Lai Aghdam et al [1] analyzed various multicarrier PWM methods for asymmetric multilevel inverter. Arif et al [2] proposed a modified cascaded multilevel inverter with reduced switch count employing bypass diode. Bahr Eldin et al [3] developed a new multicarrier based pwm for multilevel converter. Bensraj and Natarajan [4] proposed trapezoidal pwm strategies for a single phase five level cascaded inverter. Ceglia e al [5] developed A new simplified multilevel inverter topology for DC-AC conversion. Ehsan Najafi et al [6] under took a design and implementation of a new multilevel inverter topology. Juan Dixon et al [7] proposed asymmetrical multilevel inverter for traction drives using only one dc supply. Murugesan et al [8] introduced a new multilevel inverter topology using less number of switches. Mondal et al [9] developed a reduced switch-count five-level inverter with common-mode voltage elimination for an open-end winding induction motor drive. Rabiya Rasheed in [10] introduced a reduced switch multilevel topology for drives application. Rokan et al [11] discussed new multilevel inverter topology with reduced number of switches. Sujanarko in [12] introduced advanced carrier based pulse width modulation in asymmetric cascaded multilevel inverter. Murugesan in [13] proposed seven level modified cascaded inverter for induction motor drive applications. Thamizhselvan and Seyezhai [14] discussed a novel pwm hybrid multilevel inverter for fuel cell application. Nakul et al [15] proposed a twenty one level multilevel inverter with reduced switch and source. Gnana Prakash et al [16] developed a new structure multilevel inverter with reduced switch. This paper presents a single phase binary DC source seven level inverter topology for investigation using unipolar PWM control strategies. Simulations were performed using MATLAB-SIMULINK. Harmonic analysis and evaluation of different performance measures for various modulation indices have been carried out and presented.

2. PROPOSED REDUCED SWITCH SEVEN LEVEL INVERTER

The proposed inverter differs from conventional inverter by peculiarity of having binary distribution of voltage sources. The general structure of proposed inverter is shown in Figure 1. This inverter having two conversion cell and One H Bridge. Each conversion cell consists of only one active switching element and one bypass diode and one voltage source. The switches (S1 and S2) and diodes (D1 and D2) produce only unipolar output, H bridge circuit makes output voltage in both the polarity. This type of inverter consist of two unequal DC voltage with R load.

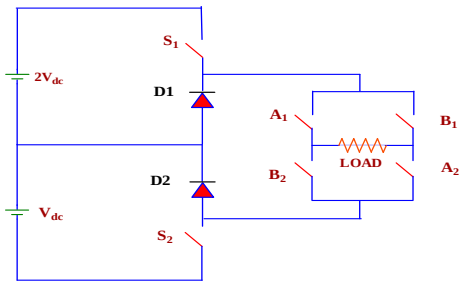

Figure 1. Binary DC source MLI

In binary DC source MLI, output voltage level is seven, if n number of H-bridge module has independent DC sources in sequence of the power of 2, an expected output voltage level is given as:

$$V_n = 2^{n+1} - 1, n = 1, 2.. \quad (1)$$

3. UNIPOLAR PULSE WIDTH MODULATION SCHEME

In this section, it is explained the results of research and at the same time is given the comprehensive discussion. Results can be presented in figures, graphs, tables and others that make the reader understand easily [2], [5]. The discussion can be made in several sub-chapters. The scheme uses a unipolar sine and trapezoidal as modulating signal and triangular as carriers. In this PWM scheme, triangular carriers are compared with rectified sine and trapezoidal reference. The intersection between the unipolar reference signal and the carrier signals defines the switching instant of the PWM pulse. The multiple carriers used are positioned above zero level and the number of carriers is dependent on the output voltage levels. For an m-level inverter, (m-1)/2 carriers with the same frequency f_c and the same amplitude A_c are disposed. The reference waveform has peak-to-peak amplitude A_m and frequency f_m. The reference is continuously compared with each of the carrier signals. If the reference is greater than a carrier signal, then the active device corresponding to that carrier is switched on; and if the reference is less than a carrier signal, then the active device corresponding to that carrier is switched off. There are many alternative strategies are possible, some of them are tried in this paper and they are:

a. Unipolar Phase disposition PWM strategy (UPDPWM).
b. Unipolar Alternate phase opposition disposition PWM strategy (UAPODPWM).
c. Unipolar Carrier overlapping PWM strategy (UCOPWM).

The formulae to find the Amplitude of modulation indices are as follows:

For UPDPWM, UAPODPWM:

$$m_a = 2A_m/(m-1)A_c) \quad (2)$$

For UCOPWM:

$$m_a = A_m / (2 * A_c) \quad (3)$$

The frequency ratio m_f are as follows:

$$m_f = f_c / f_m \quad (4)$$

3.1. Unipolar Phase Disposition PWM (UPDPWM)

The triangular carriers of same amplitude and frequency are disposed such that bands they occupy are contiguous. The carrier arrangement for binary DC source multilevel inverter having Sinusoidal reference and Trapezoidal are illustrated in Figure 2 & 3 respectively.

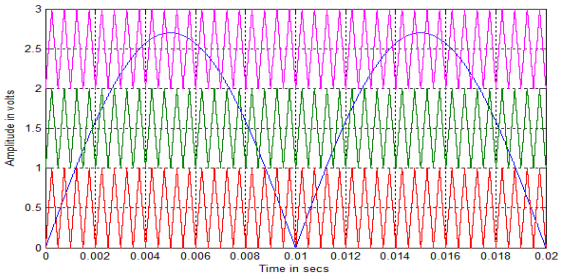

Figure 2. Carrier arrangement for UPDPWM strategy with sinusoidal reference (ma=0.9 and m_f=40)

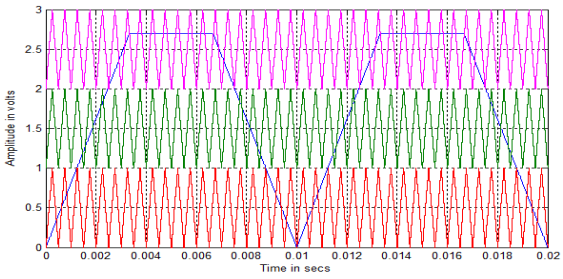

Figure 3. Carrier arrangement for UPDPWM strategy with Trapezoidal reference (m_a=0.9 and m_f=40)

3.2. Unipolar Alternative Phase Opposition Disposition PWM (UAPODPWM)

Carriers for binary DC source multilevel inverter having Sinusoidal reference and Trapezoidal are illustrated in Figure 4 & 5 respectively. The triangular carriers of same amplitude are phase displaced from each other by 180 degrees alternately.

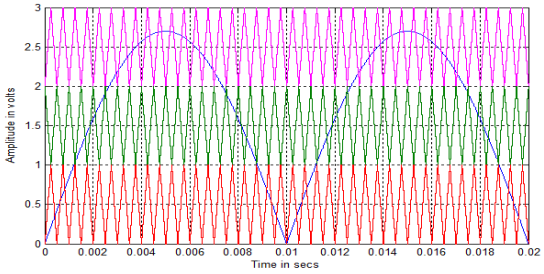

Figure 4. Carrier arrangement for UAPODPWM strategy with sinusoidal reference (m_a=0.9 and m_f=40)

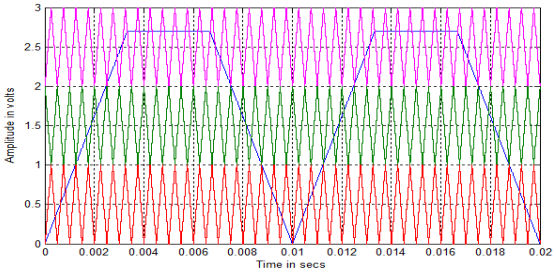

Figure 5. Carrier arrangement for UAPODPWM strategy with Trapezoidal reference (m_a=0.9 and m_f=40)

3.3. Unipolar Carrier Overlapping PWM (UCOPWM)

Carriers for binary DC source multilevel inverter having Sinusoidal reference and Trapezoidal are illustrated in Figure 6 & 7 respectively. In carrier overlapping technique, carriers of same amplitude and frequency are disposed such that the bands they occupy overlap each other; the overlapping vertical distance between each carrier is $A_c/2$.

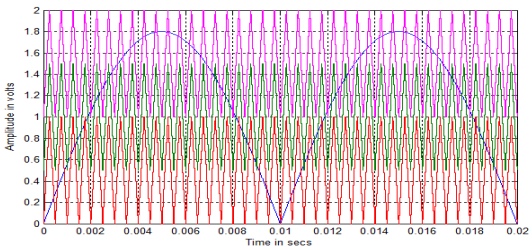

Figure 6. Carrier arrangement for UCOPWM strategy with sinusoidal reference(m_a=0.9 and m_f=40)

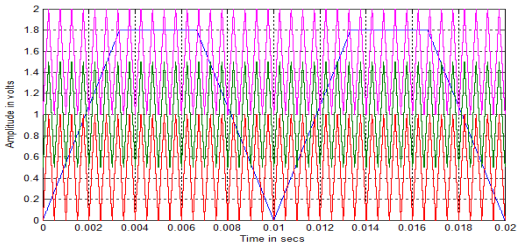

Figure 7. Carrier arrangement for UCOPWM strategy with Trapezoidal reference (ma=0.9 and mf=40)

4. SIMULATION RESULT

The single phase binary DC source seven level inverter is modeled in SIMULINK using power system block set. Switching signals for binary multilevel inverter using UPWM strategies are simulated. Simulations were performed for different values of ma ranging from 0.8 to 1 and the corresponding %THD are measured using the FFT block and their values are shown in Table 1. Next table displays the V_{RMS} of fundamental of inverter output for same modulation indices. Table 3 and 4 display respectively the corresponding Crest Factor (CF) and Distortion Factor (DF) of the output voltage. Figure 8(a) and (b) respectively shows the seven level output voltage generated by UPDPWM strategy with Sinusoidal reference and its FFT plot. Figure 9(a) and (b) respectively shows the seven level output voltage generated by UPDPWM strategy with Trapezoidal reference and its FFT plot. Figure 10(a) and (b) respectively shows the seven level output voltage generated by UAPODPWM strategy with Sinusoidal reference and its FFT plot. Figure 11(a) and (b) respectively shows the seven level output voltage generated by UAPODPWM strategy with Trapezoidal reference and its FFT plot. Figure 12(a) and (b) respectively shows the seven level output voltage generated by UCOPWM strategy with Sinusoidal reference and its FFT plot. Figure 13(a) and (b) respectively shows the seven level output voltage generated by UCOPWM strategy with Trapezoidal reference and its FFT plot.

The following parameter values are used for simulation: V_{DC} =50 V, R (load) = 100 ohms, f_c=2000 Hz and f_m=50Hz.

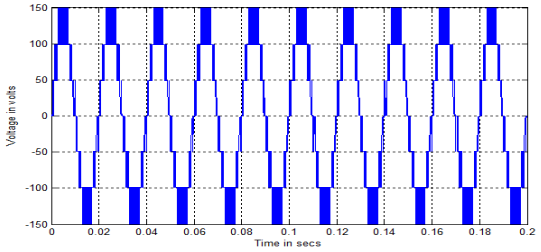

Figure 8(a). Output voltage generated by UPDPWM strategy with Sinusoidal reference

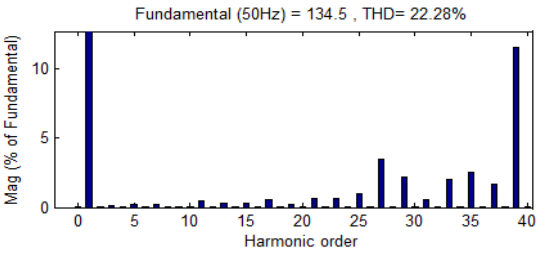

Figure 8(b). FFT plot for output voltage of UPDPWM strategy with Sinusoidal reference

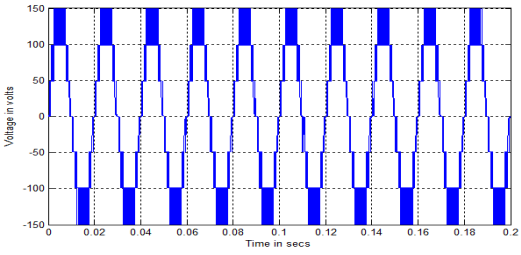

Fig.ure 9(a). Output voltage generated by UPDPWM strategy with Trapezoidal reference

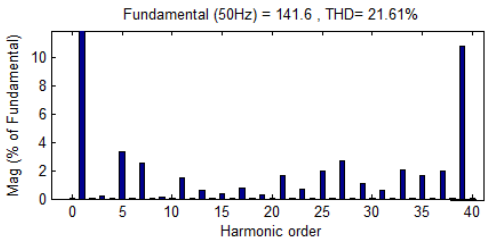

Figure 9(b). FFT plot for output voltage of UPDPWM strategy with Trapezoidal reference

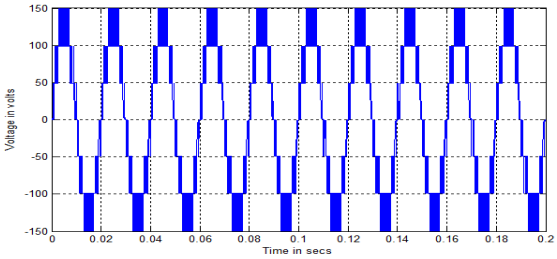

Figure 10(a). Output voltage generated by UAPODPWM strategy Sinusoidal reference

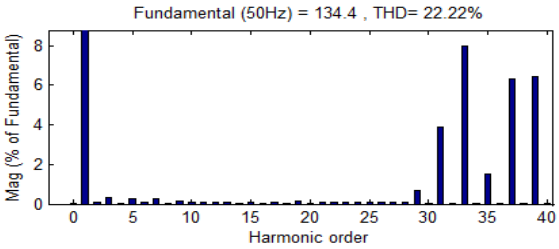

Figure 10(b). FFT plot for output voltage of UAPODPWM strategy with Sinusoidal reference

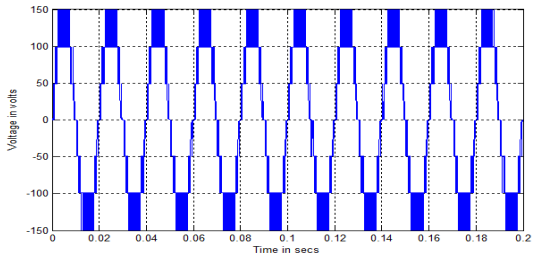

Figure 11(a). Output voltage generated by UAPODPWM strategy Trapezoidal reference

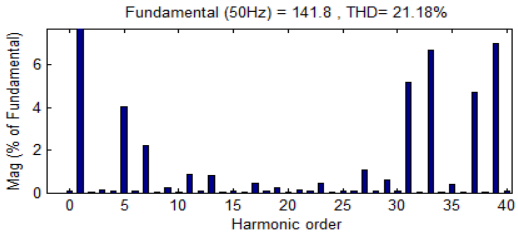

Figure 11(b). FFT plot for output voltage of UAPODPWM strategy with Trapezoidal reference

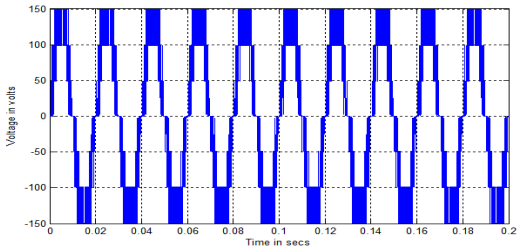

Figure 12(a). Output voltage generated by UCOPWM strategy with Sinusoidal reference

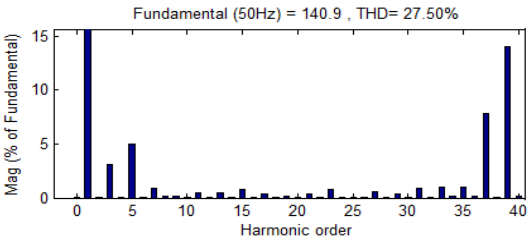

Figure 12(b). FFT plot for output voltage of UCOPWM strategy with Sinusoidal reference

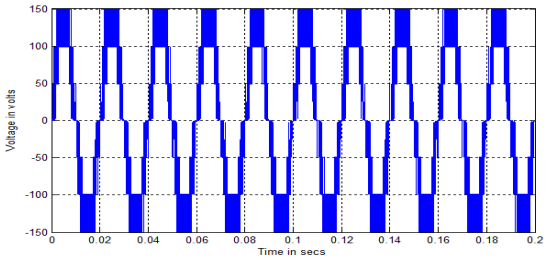

Figure 13(a). Output voltage generated by UCOPWM strategy with Trapezoidal reference

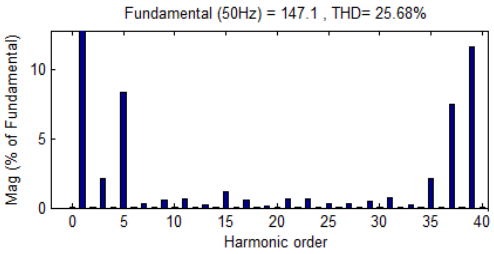

Figure 13(b). FFT plot for output voltage of UCOPWM strategy with Trapezoidal reference

It is observed from Table , that the harmonic content of output voltages is least with UPDPWM strategy with trapezoidal reference provides relatively lower %THD for most of m_a. From Table , it is found that UCOPWM strategy with trapezoidal reference provide higher DC bus utilization. CF is relatively equal for all the strategies (Table 3). % DF relatively low in UPDPWM strategy with sinusoidal reference. (Table 4).

For m_a= 0.9, it is observed from the Figure 8(b), 9(b), 10(b), 11(b), 12(b), and 13(b) the harmonic energy is dominant in: a) 27th and 39th order in UPDPWM with Sinusoidal reference and 5th, 27th, and 39th of Trapezoidal reference. b) 31st, 33rd, 37th and 39th in UAPODPWM with Sinusoidal reference and 5th, 31st, 33rd, 37th and 39th of Trapezoidal reference. c) 3rd, 5th, 37th and 39th in UCOPWM with Sinusoidal reference and 5th, 37th and 39th of Trapezoidal reference.

Table 1. % THD for Different Modulation Indices

m_a	UPDPWM		UAPODPWM		UCOPWM	
	Sinusoidal Ref.	Trapezoidal Ref.	Sinusoidal Ref.	Trapezoidal Ref.	Sinusoidal Ref.	Trapezoidal Ref.
1	18.01	15.06	18.24	15.60	22.88	20.83
0.9	22.28	21.61	22.22	21.18	27.50	25.68
0.8	24.15	24.66	24.13	24.83	32.31	30.26
0.7	24.79	23.66	24.78	23.88	40.26	37.92

Table 2. V_{RMS} for Different Modulation Indices

m_a	UPDPWM		UAPODPWM		UCOPWM	
	Sinusoidal Ref.	Trapezoidal Ref.	Sinusoidal Ref.	Trapezoidal Ref.	Sinusoidal Ref.	Trapezoidal Ref.
1	105.8	111.7	105.8	111.5	109	112.9
0.9	95.13	100.1	95.04	100.2	99.61	104
0.8	84.32	88.95	84.21	88.78	89.59	94.24
0.7	73.45	77.62	73.57	77.52	76.46	81.91

Table 3. Crest Factor For Different Modulation Indices

m_a	UPDPWM		UAPODPWM		UCOPWM	
	Sinusoidal Ref.	Trapezoidal Ref.	Sinusoidal Ref.	Trapezoidal Ref.	Sinusoidal Ref.	Trapezoidal Ref.
1	1.41493	1.41450	1.41398	1.41434	1.41376	1.41452
0.9	1.41385	1.41458	1.41414	1.41516	1.41451	1.41442
0.8	1.41366	1.41427	1.41432	1.41473	1.41422	1.41447
0.7	1.41456	1.41458	1.41361	1.41382	1.41381	1.41374

Table 4. % Distortion Factor for different modulation indices

m_a	UPDPWM		UAPODPWM		UCOPWM	
	Sinusoidal Ref.	Trapezoidal Ref.	Sinusoidal Ref.	Trapezoidal Ref.	Sinusoidal Ref.	Trapezoidal Ref.
1	0.019	0.178	0.041	0.172	0.190	0.302
0.9	0.019	0.146	0.047	0.169	0.396	0.413
0.8	0.031	0.170	0.028	0.160	0.699	0.674
0.7	0.029	0.168	0.023	0.158	0.850	0.843

5. CONCLUSION

This paper has proposed a binary DC source reduced switch 7-level inverter, and has observed that UPDPWM strategy with trapezoidal reference provides output with relatively low distortion and UCOPWM strategy with trapezoidal reference provides relatively higher fundamental RMS output voltage.

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