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Closed Loop Analysis of Bridgeless SEPIC Converter for Drive Application

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ABSTRACT

In this paper closed loop analysis of Single phase AC-DC Bridgeless Single Ended Primary Inductance Converter (SEPIC) for Power Factor Correction (PFC) rectifier is analyzed. In this topology the absence of an input diode bridge and the due to presence of two semiconductor switches in the current flowing path during each switching cycle which will results in lesser conduction losses and improved thermal management compared to the conventional converters. In this paper the operational principles, Frequency analysis, and design equations of the proposed converter are described in detail. Performance of the proposed SEPIC PFC rectifier is carried out using Matlab Simulink software and results are presented.

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1. INTRODUCTION

Due to the increase on high efficiency and low harmonic pollution, the PFC circuits are commonly employed in ac–dc converters and also in switched-mode power supplies. Generally, in these kinds of converters include a full-bridge diode rectifier on an input current path, so that conduction losses will be worse especially at the low line. To overcome this problem, bridgeless converters is introduced to reduce or eliminate the full-bridge rectifier, and hence a conduction losses [1]–[3]. Recently, several bridgeless topology have been introduced to improve the rectifier power density and also to reduce noise emissions via soft-switching techniques or coupled magnetic topologies [4]–[6]. In conventional PFC Buck converters, the output voltage of the converter in [7] and [8] is lower than the peak value of the input voltage. In [9]–[13], several bridgeless single-ended primary inductor converters (SEPICs) were proposed, however in this converter, an input inductor with large inductance should be used in order to reduce the input current ripple. The above literature review does not deal with, a bridgeless SEPIC converter with ripple-free input current, closed loop analysis and Frequency response analysis of the Bridgeless SEPIC PFC converter fed DC drive.

2. BRIDGELESS SEPIC CONVERTER

2.1. Circuit Operation

The proposed bridgeless SEPIC converter is shown in Figure 1, which is contracted by connecting two dc-dc converters. During the positive half-line cycle, the first part of circuit L1- Q1 – L3 – Do is active

through diode Dp, which is connecting the input ac source to the output ground. During the negative half-line cycle, the second part of circuit, L2- Q2- C2- L3- Do, is active through diode Dn, which is connecting the input ac source to the output ground. Generally it is sufficient to analyze the circuit only during the positive half of the input voltage. Apart from that, the operation of the proposed rectifiers will be briefly described by assuming that the three inductors are operating in DCM. Because of this several advantages can be gained. These advantages include the following: there is approximate near-unity power factor, the power switches are turned on at zero current, and the output diode Do is turned off at zero current. Thus, the losses due to the turn-on switching and the reverse recovery of the output diode are considerably reduced. Due to filter circuit across the output DC is ripple free. Coupled inductors are also used to reduce the ripple content in the circuit. Similarly the Efficiency of the proposed converter can be improved.

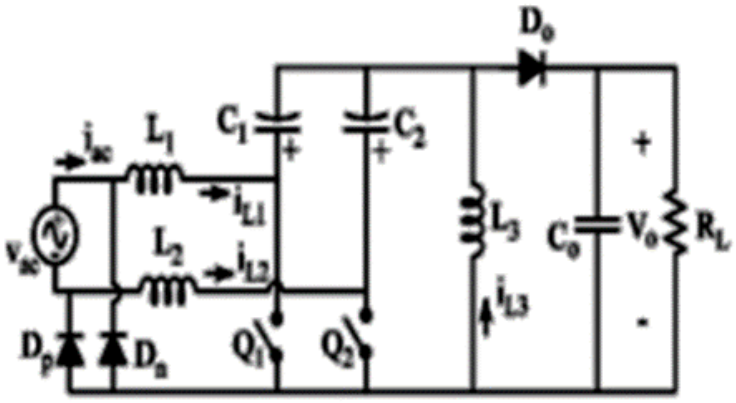

Figure 1. Proposed SEPIC Converter

2.2. Efficiency Improvement

The efficiency of the proposed converter can be improved by i). The voltage drop of a MOSFET is ignored, ii). The power dissipation of the reduced components is theoretically calculated. This is done with the assum ption that the forward voltage drops of all diodes are 0.5 V.

$$Pavg = \frac{1}{T}\int_0^T 2VD\ IDDdt \tag{1}$$

$$\Delta\eta\ Proposed = P\ avg/input \tag{2}$$

In this case when the proposed gate signals are applied to the converter, one diode of a rectifier, including the intrinsic body diode, is omitted in a switching period. So, the efficiency improvement of the proposed converter is obtained.

2.3. Frequency Response Analysis

The power stage specifications of the bridgeless SEPIC PFC converter are designed with following power stage parameters like Input voltage, Output voltage, Output power, Switching frequency, Power Factor. According to the design specification parameters, the state vectors for both switching intervals (in the equation 3 & 4) and a quasi-state assumption, following the numerical expression of the control-to-inductor current transfer function is obtained assuming an input voltage.

$$A1 = \begin{pmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{C1} & 0 & 0 \\ 0 & 0 & 0 & -1/RC0 \end{pmatrix} \tag{3}$$

$$B1 = \begin{bmatrix} \frac{1}{L1} \\ \frac{1}{L2} \\ 0 \\ 0 \end{bmatrix} \quad (4)$$

$$G(s) = \frac{S3 + S2 + S + 3.96}{S4 + S3 + S2 + S1 = 3.49} \quad (5)$$

$$Fr = \sqrt{1 - D/L1C1} \quad (6)$$

Figure 2 shows the frequency response of the derived control-to-inductor model. As there are 2 resonance locations, and one among them has very high Q-factor. In addition, from the state-matrix and the transfer function with the characterized parameters, the locations of resonance points are determined as shown in equation-6. Those locations are related to the main passive components and the duty cycle that presents the relation between the input voltage and the output voltage.

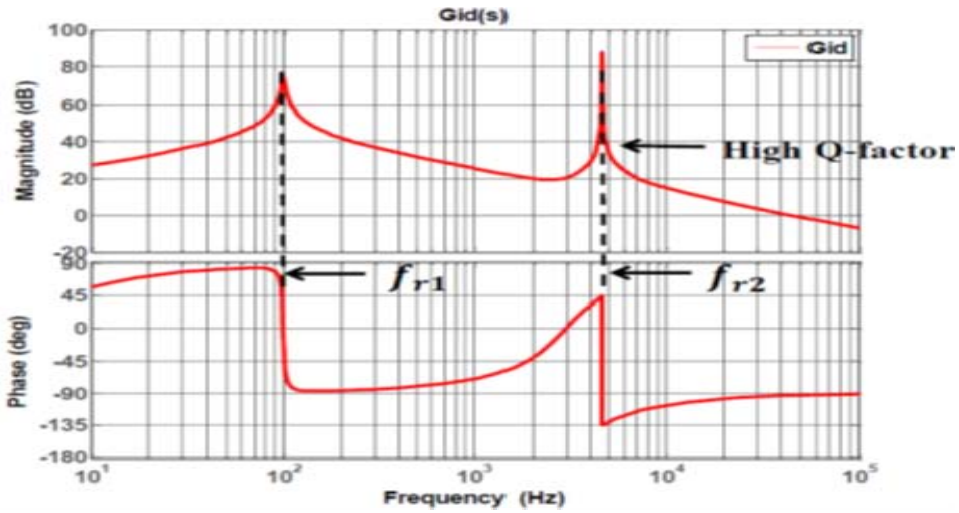

Figure 2. Frequency response of input voltage

3. SIMULATION ANALYSIS

The performance of the proposed modeled is evaluated Using Matlab-Simulink environment, and it is extended to drive applications. The simulation of bridgeless SEPIC converter is shown in Figure 3, which gives a low conduction loss and switching loss during switch turn on and turn off condition. Figure 4 shows the input voltage and current waveform. This circuit also used to improve power factor during conversion of ac-dc. Here three identical inductors are used to reduce the ripple current. The output voltage measures 59 volts and current measures 1.4 amps from the Figure 5

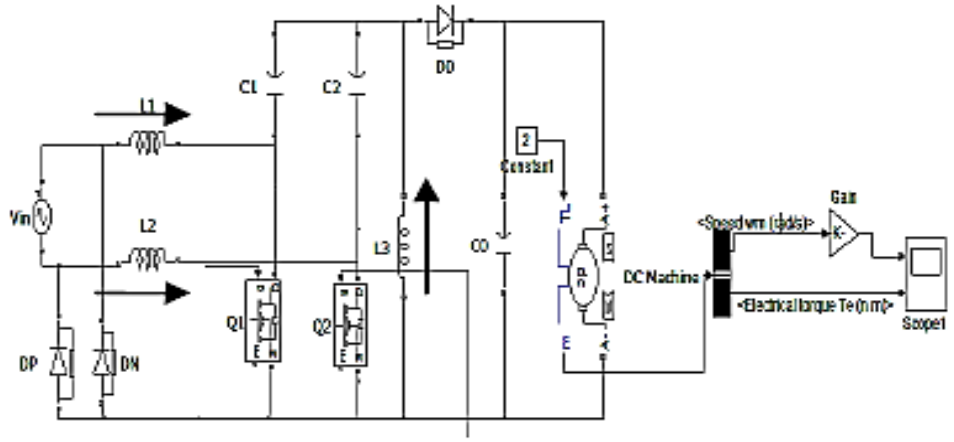

Figure 3. Simulation of Proposed Circuit

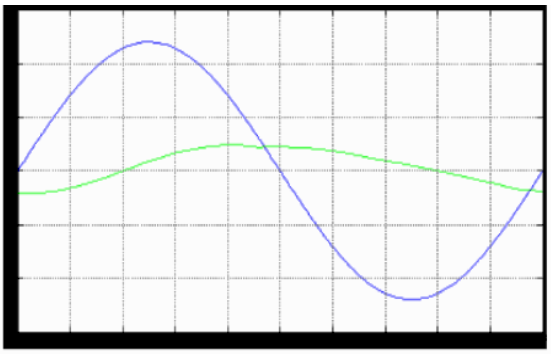

Figure 4. Measured Input Voltage and Current

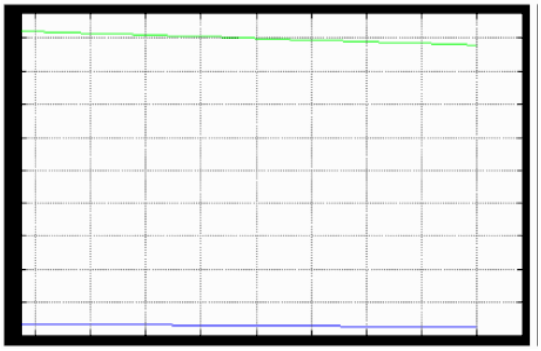

Figure 5. O/P Voltage= 59 v, Current=1.4 A

Figure 6 depicts the closed loop simulation circuit using PI controller, where input side voltage disturbances are created at a specified time. During open loop system output voltage of open loop with disturbance remains constant till the time of disturbance given by PI controller.

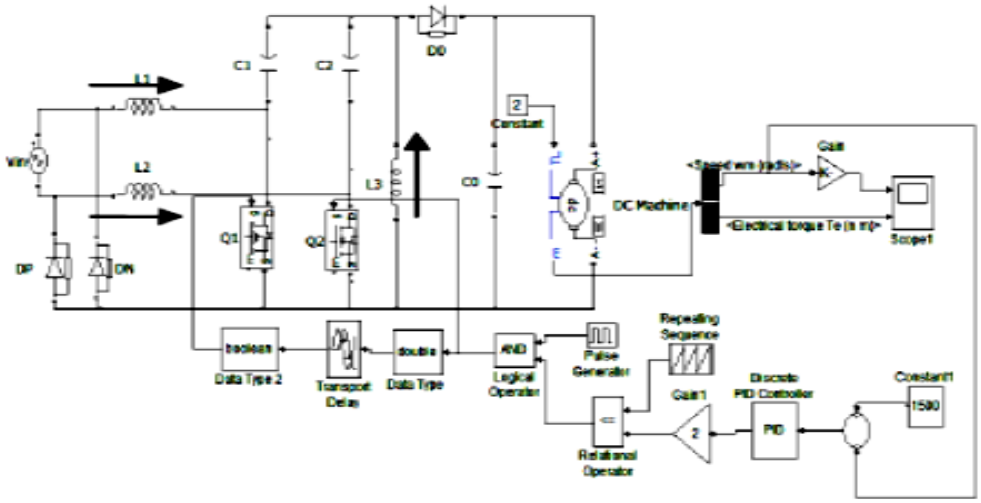

Figure 6. Closed loop Analysis of Proposed Converter

The input voltage disturbance is done using PI controller and it gets reflected in the output side, leading to reduction in the output voltage. During this time the closed loop PI circuit with PWM controller helps in reducing the overshoot caused due to open loop.

The output voltage is continuously compared with a reference voltage using a differential amplifier. The differential signal is amplified and fed to comparator. The comparator output is fed to one of the MOSFET switches. Another triangular wave is phase shifted by 180º is compared with the same differential amplifier output and the output of the second comparator is fed to the other MOSFET. Thus changes in the output voltage are reflected in the differential amplifier output and in turn in the comparator output. Figure 7 gives the output DC voltage of the closed loop circuit. Figure 8 shows the step change in the torque at 1 sec and from Figure 9, the speed attains its steady state instantly after the step change in the load torque.

From Figure 10, the THD mains current of the proposed PFC SEPIC converter fed DC drive is observed under 5%, which is the requirement of power quality.

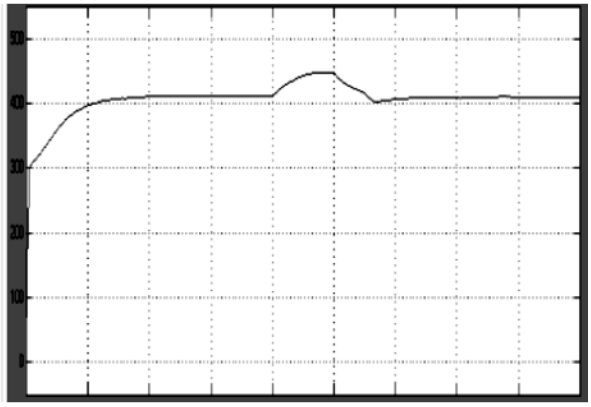

Figure 7. DC Output Voltage

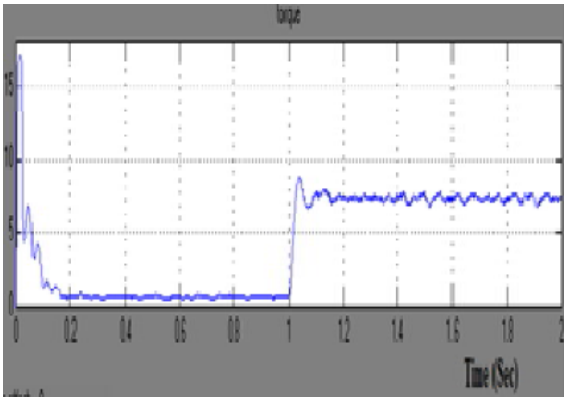

Figure 8. Change in load torque at time t= 1 sec

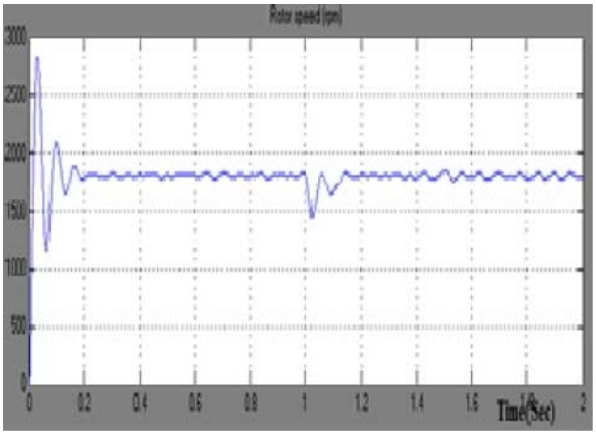

Figure 9. Speed response of close loop system

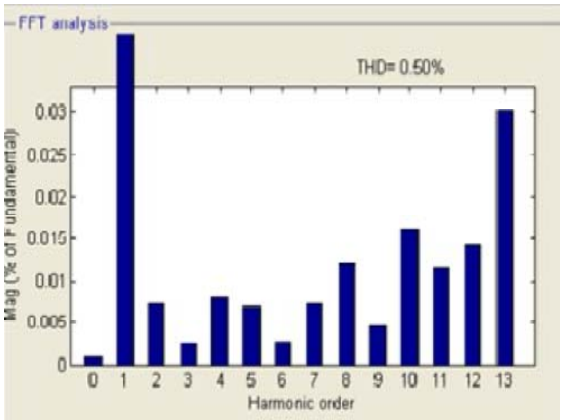

Figure 10. THD Value of Proposed Converter

4. EXPERIMENTAL ANALYSIS OF SEPIC CONVERTER

Figure 11 shows the hardware board with top side for main switches and bottom side for controller. The output voltage is regulated and the input current tracks the input voltage. Under full-load condition, the power factor and the harmonic distortion result can be analyzed from Figure 12. Harmonic components are shown in Table 1. The major objective of the analysis is to compensate the power stage with proper damping and to ensure the stable operation of converter. Bridgeless SEPIC PFC topologies can further improve the conversion efficiency. To maintain same efficiency, the improved circuits could operate with higher switching frequency.

Figure 11. Hardware of Proposed Converter

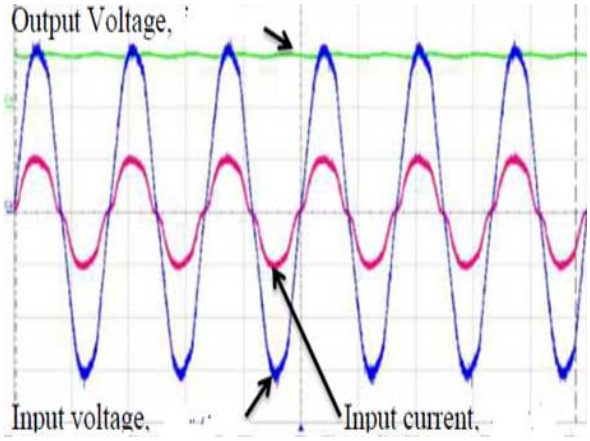

Figure 12. Input AC and output DC signals of proposed converter

Table 1. Harmonic components

Fundamental	3	5	7	9
1.448A	0.067A	0.097A	0.044A	0.009A

5. CONCLUSION

In order to improve the efficiency, bridgeless SEPIC converter has been proposed. Performance of the proposed SEPIC PFC rectifier is carried out using Matlab Simulink software. The frequency response of the derived control-to-inductor model is analyzed for the proposed converter. In our analysis Bridgeless SEPIC PFC rectifier suffers a step input voltage change and thereby it attains the steady state. Besides in improving the circuit topology the performance can be further reduce in rectifier size could be realized by integrating the three inductors. The simulation results are presented to verify the controller design. The experiment results indicate that the harmonic contents are well below the limits. It is verified that a well-designed damping circuit reduces the high risk of system instability. Simulation and hardware results show high performance in terms of high power factor and efficiency.

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